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Characterizing the VFAT3 chip for the DAQ electronics of the CMS detector

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Master thesis submitted under the supervision of
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Abstract

As part of the next long shutdown of the Large Hadron Collider (LHC) from 2018 to 2020, the Compact Muon Solenoid (CMS) experiment is planned to be upgraded, namely by means of the GE1/1 project implementing a new gas detector technology. This master thesis contributes to characterizing the newest version of the VFAT chip which is the first element in the acquisition (DAQ) electronics of the detector. After briefly describing the LHC and CMS, the GE1/1 project and its detector are presented. Then a description of the VFAT and a detailed overview of the new features in the VFAT3 version are provided in order to define and develop a test bench of the chip in terms of firmware and software. Finally, a characterization of the VFAT3 is carried out in order to validate its design for the next detector prototype.

Keywords: CERN, CMS, LHC, GE1/1 Project, VFAT, DAQ.

Acknowledgments

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Contents

Introduction

In 2013, the Nobel prize in Physics was awarded to François Englert and Peter W. Higgs for the Higgs boson's discovery highlighted by the ATLAS and CMS experiments in the LHC at CERN. [1]

Since the beginning of its operation in 2009, the LHC is regularly improved in order to reach higher operating energies and intensities to hopefully bring out new breakthroughs in the understanding of the universe.

In this project, Belgian universities are strongly involved in CMS and its upgrades as attested by the amount of existing PhD and master theses on this subject. [2]

In the next upgrade of CMS, a new detector will be implemented in its endcaps as an additional muon tracker, namely the GE1/1 project. Besides the detector technology, the DAQ electronics which has to carry the data to the control room is crucial. In particular the VFAT chips are the first element in the chain and need to be carefully designed.

The latest version of that chip – the VFAT3 – has newly been released and its arrival raises several questions. Is the chip working properly ? Does it meet the design requirements, namely in terms of timing and spatial resolution ? The chip has to be verified and a full process of debugging and characterization needs to be performed to determine whether the VFAT3 chip is ready for production and integration to the DAQ electronics. Therefore, what testing methodology must be adopted ? The purpose of this master thesis is thus to take charge of this new chip by first considering a new firmware architecture to communicate and transfer data with the VFATs for finally performing series of tests to characterize the chip's behaviour.

In this thesis, the context will first be settled in more details (chapter 1) then the VFAT3 and its differences with the VFAT2 will be exposed (chapter 2). Next, the test bench set-up of the chip will be exposed, including a rethought of the software and firmware architecture communicating with the VFAT (chapter 3). Finally, the VFAT3 will be characterized to check if it is in accordance with preliminary simulations and expected results (chapters 4 and 5). Before concluding, the organization and the planning of the project are presented, as well as the issues encountered and how I managed them (chapter 6).

Chapter 1

The GE1/1 project

This chapter will first detail the context in which the GE1/1 project is framed before emphasizing the project itself and its detector.

1.1 The LHC

In 2008, CERN has ended to build the world's largest particle accelerator, the Large Hadron Collider (LHC). Its principle is to send in a 27km-ring two bunches of protons in opposite directions to collide them and create unstable particles to be observed and studied. More recently, it is that experiment which led to the discovery of the Higgs Boson.

Powerful detectors are therefore needed to register each resulting particle. To this end, four experimental devices have been built along the LHC : ALICE, ATLAS, LHCb and CMS, as presented on figure 1.1.

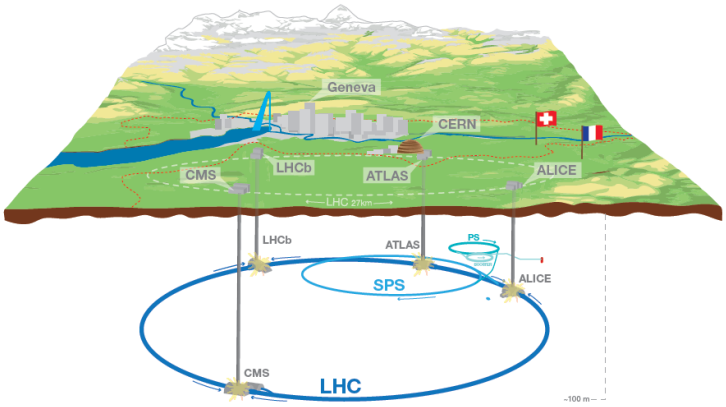

Figure 1.1: Schematic of the LHC with its four experiments' positions. [3]

1.1.1 LHC calendar

The LHC is experiencing different Long Shutdowns (LS) during its life time allowing to upgrade and add new features to the machine. Figure 1.2 shows the time line of the expected LHC upgrades in the coming years. The LS3 will allow a crossover of the peak luminosity from $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ to $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Looking towards this so-called *high luminosity* phase of the LHC, the GE1/1 project is planned to be added to CMS during the next Long Shutdown – LS2 – between 2018 and 2020.

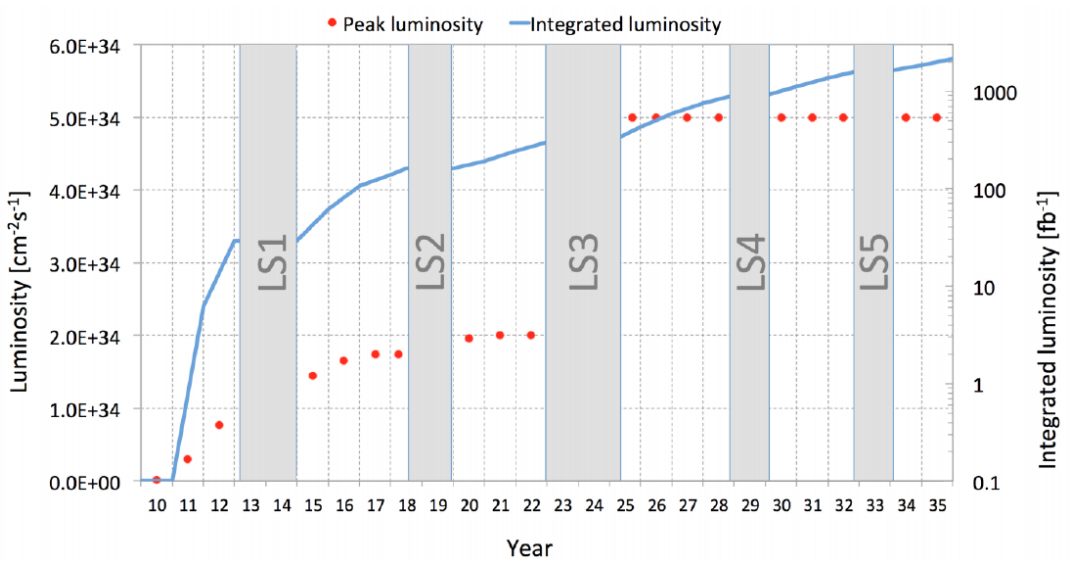

Figure 1.2: Time line of the LHC upgrades with respect to the luminosity evolution. The luminosity is an indicator of the performance of the particle collider. The peak luminosity measures the ability to produce a given number of interactions while the integrated luminosity directly relates to the number of observed events of interest. [4], [5]

1.2 The CMS experiment

CMS stands for the Compact Muon Solenoid and is one of the four main experiments around the LHC. Its primary function is the detection and study of the muons resulting from collisions.

From the figure 1.3, CMS can be depicted as a huge barrel of 28.7 m length and 15 m diameter. It is closed by two endcaps in order to ensure a full coverage of the collision point, located in the center of CMS.

CMS contains of course many sub-detectors. They are split in the two following categories.

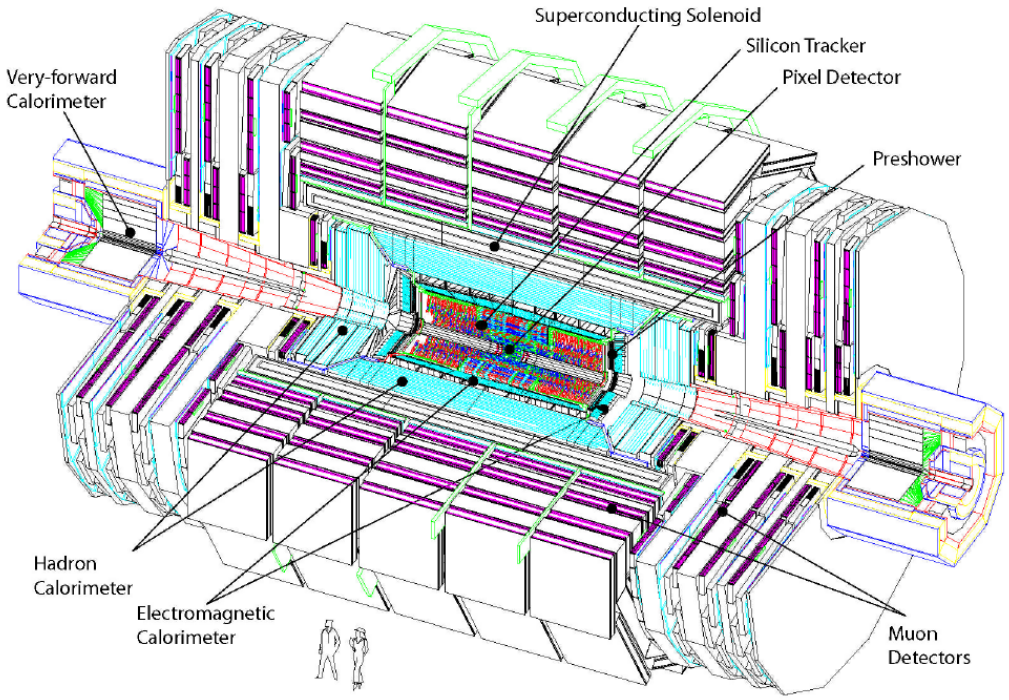

Figure 1.3: The CMS experiment and its different layers [6]

1.2.1 The calorimeters

Calorimeter detectors produce a signal proportional to the energy of the particle hit. Inside CMS, electromagnetic calorimeters (ECALs) and hadronic calorimeters (HCALs) are used which respectively detect the high energy electrons (or positrons) as well as photons and hadrons.

1.2.2 The trackers

Aside from the particle's energy, it is also necessary to evaluate its momentum and determine its trajectory. To this end, the trackers are made of several layers each calculating the collision point of the particle with the detector. Gathering these data allows to estimate its trajectory. As the tracker needs to interfere as less as possible with the particles, gaseous or silicon detectors are generally preferred.

1.2.3 Setting of the sub-detectors inside CMS

On figure 1.4, a cross section of CMS details the different operating sub-detectors.

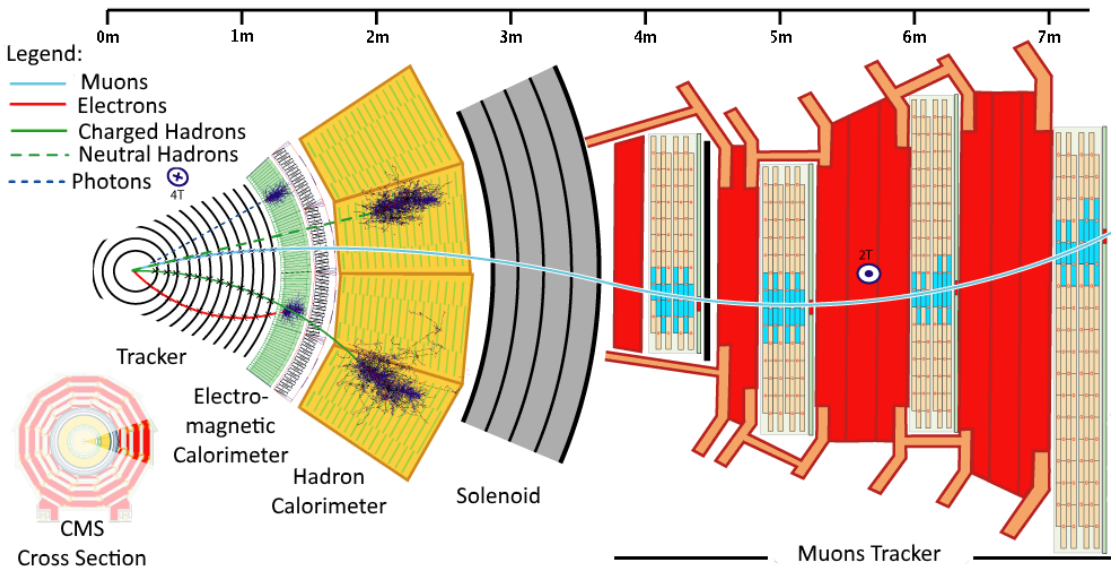

Figure 1.4: Schematic view of a slice of the CMS showing the interaction of particles in the different detection layers.[3]

Starting from the collision point and going outward, the particle will cross [7], [8] :

Silicon tracker It allows to follow the precise path of charged particles through a magnetic field and determine their momentum.

Electromagnetic calorimeter (ECAL) ECAL measures the energy of emerging particles, in particular electrons and photons. The latter are neutral particles and thus invisible to silicon tracker. Their detection via the ECAL is consequently essential.

Hadron Calorimeter (HCAL) This calorimeter measures the energy of hadrons (neutrons, protons, pions, kaons, ...).

Solenoid The solenoid is the world's largest superconducting magnet built and it generates a magnetic field of 4 T. It allows to sufficiently bend the trajectory of the high energy (> 10 GeV) charged particles to measure precisely enough their momentum.

Muon tracker It consists of the four last layers of CMS and takes care of detecting muons, the only particles able to pass through the previous layers. The particle trajectory is reconstructed by fitting a curved path to the hits registered in the four layers and it allows to determine its momentum.

Oppositely to silicon tracker, muon trackers cover a much larger surface (several hundreds of square metre) therefore using gas detectors in place of silicon due to a better covered-area-to-cost ratio.

Of course, those detectors are also found in the endcaps of CMS. That is precisely where the GE1/1 project takes place.

1.2.4 The trigger system

The LHC is running at a nominal frequency of 40 MHz. This means that every 25 ns there is a collision of two bunches of protons. This high rate needs to be reduced in order to collect all the particles data before the next collision.

A real-time selection is therefore applied to determine if an event is relevant based on the energy, the mass and the charge of the reconstructed particles. This is the so-called trigger system of CMS and has two levels. [9], [8]

Level-1 trigger (LV1) LV1 takes place in the electronics of the detectors and its aim is to reduce the event rate from 40 MHz to 100 kHz. As the time constraint is severe (3.2 µs), it uses low-granularity data to determine if a collision is relevant. During this process, the full granularity data are stored in a FIFO memory. If a collision is judged relevant, a *Level-1 Accept* signal will be sent back to extract its full tracking data to the next trigger level. If the collision is judged non-relevant, its data will be later erased from FIFO by new data.

High-Level trigger (HLT) The time constraint being less restrictive (around 1 ms), HLT can use more powerful algorithms on processors to reduce the event rate even further to 100 Hz.

1.3 The GE1/1 project

The CMS muon tracker is currently composed of three technologies of gaseous detectors. Figure 1.5 shows a longitudinal view of a quarter of CMS highlighting with colors these different technologies:

- the Drift Tubes (DTs) are present in the barrel of CMS,
- the Cathode Strip Chambers (CSCs) are in the endcaps and
- the Resistive Plate Chambers (RPCs) are found in both regions, complementing the DTs and CSCs.

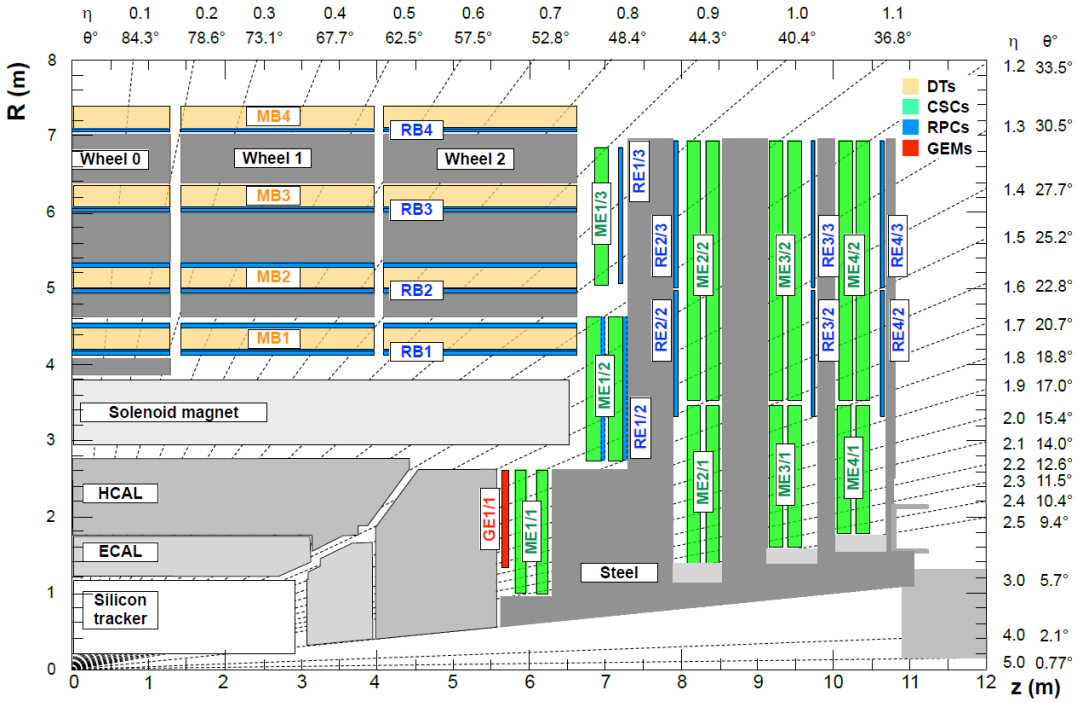

Figure 1.5: Cut of the CMS highlighting the different detectors in the endcaps [10]

To withstand LHC performance during its high luminosity phase, a region in the CMS endcap which was reserved for RPCs will be equipped with a more suitable technology thanks to the GE1/1 project. [9], [10]

The aim of the GE1/1 [1] project is to implement a new technology of gaseous detector for muon tracking and is expected to be added to the CMS endcaps during the next Long Shutdown of the LHC between 2018 and 2020. [10]

As a matter of fact, this project had to meet major constraints, in particular in terms of [10]:

Geometry The space available in the endcaps is very small, only a few centimetre along z-axis and the detector has to cover the whole area to ensure hermeticity for the muon detector. .

Hit rate The detector needs to support rates of up to $10\,\mathrm{kHz\,cm^{-2}}$.

Efficiency A detection efficiency of at least $97\,\%$ is required to detect a maximum of particles.

[1] GE1/1 is a conventional name to indicate the type of detector (G – GEM technology), its corresponding region in CMS (E – endcap) and its precise position in the CMS (the two last numbers).

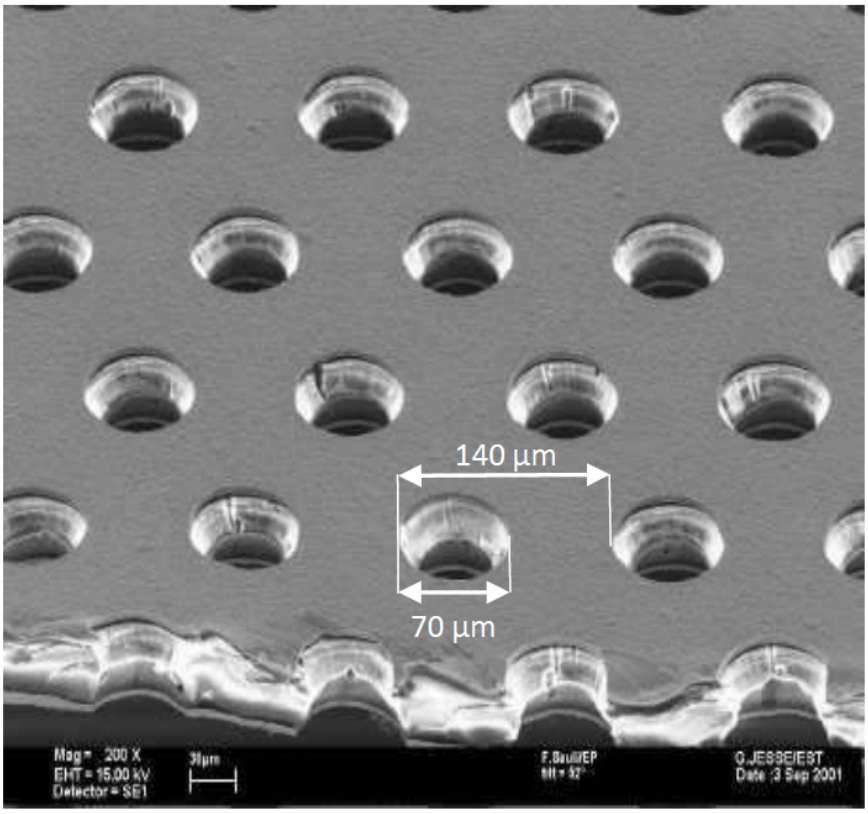

Figure 1.6: Zoom on a GEM foil [10]

Angular resolution At least 300 µrad resolution is needed to precisely determine the angular muon positions.

Time resolution To participate to the LV1 trigger, a time resolution of 10 ns or better is requested.

To fulfill those constraints, triple-GEM technology has been chosen for the detector.

1.3.1 The triple-GEM dectector

This detector is composed of a set of three GEM (Gas Electron Multiplier) foils surrounded by gas. One foil and its typical dimensions are depicted on figure 1.6.

When a muon passes through the detector, it ionizes the gas and create electrons. Each foil is drilled with holes all over the surface and is formed by two thin copper sheets isolated by a dielectric layer and a high electric field (order of 10 kV cm^{-1}) is created between those two surfaces, as presented on figure 1.7. So the resulting electrons are attracted and accelerated by this electric field in the holes, ionizing other gas molecules and creating an avalanche.

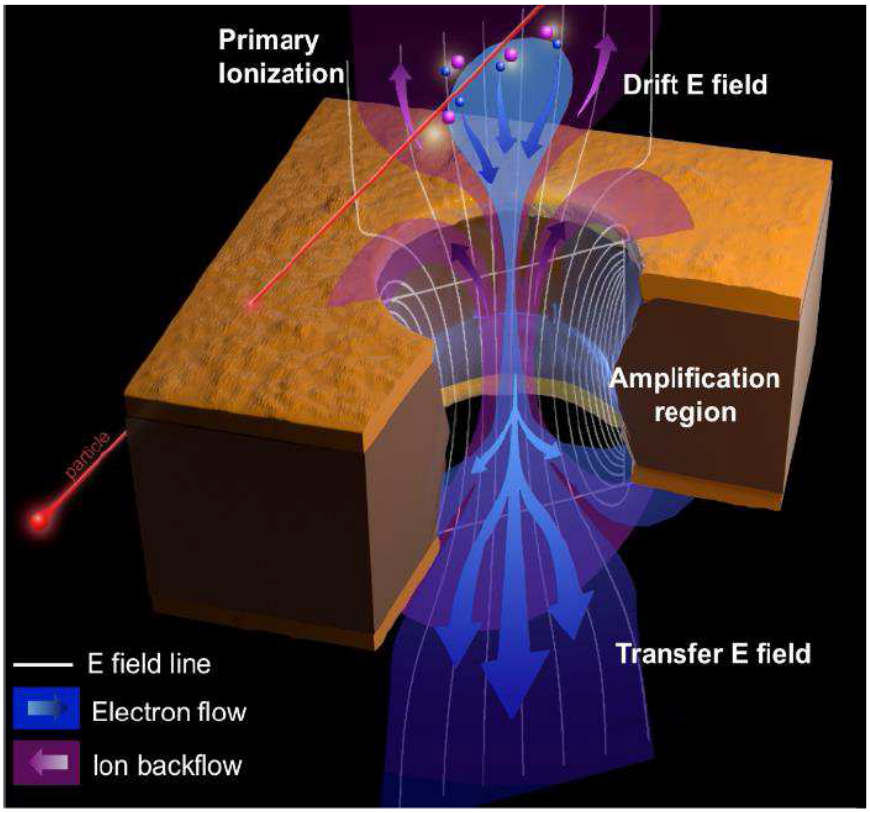

Figure 1.7: The GEM technology principle. [10]

By triplicating this phenomenon, the gas gain, which is typically defined as the ratio between the number of electrons exiting the GEM hole and the number of electrons entering it, goes from about 20 for one foil up to 8000 for the triple-GEM configuration. As shown on figure 1.8, a particle passing through the detector ionizes the gas and the three GEM foils provoke an avalanche process multiplying the number of electrons until the readout board, collecting a readable electric signal.

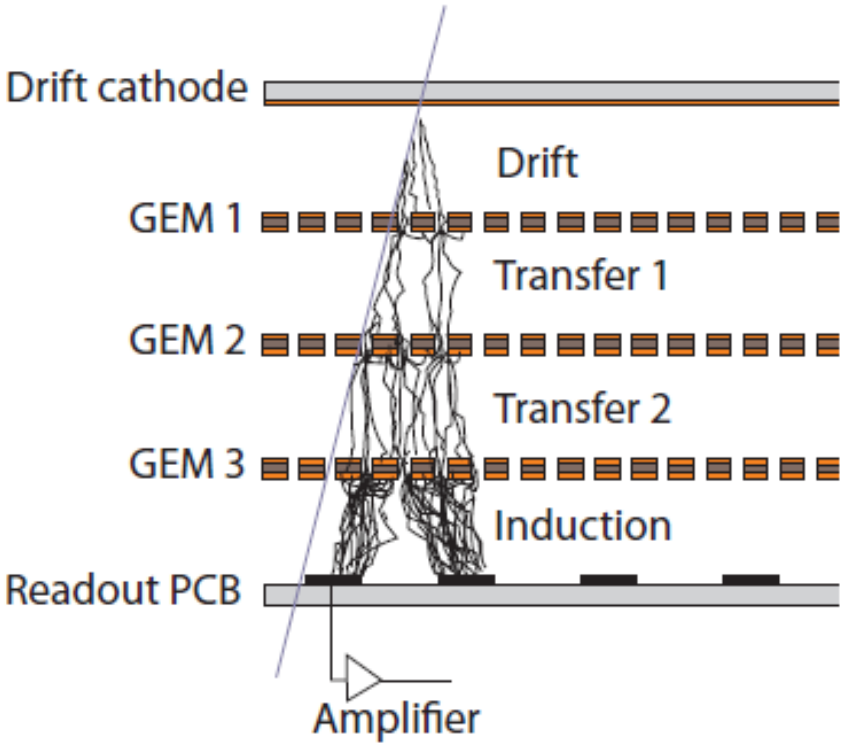

Figure 1.8: The three GEM foils increase the gain of electrons by a power of 3 [10]

1.3.2 Set-up of the detector

Figure 1.9 shows a CMS endcap and the position of the GEM detectors, highlighted in red and blue. Each detector covers 10° in azimuthal angle; it has a trapezoidal shape with a length of 100 cm, a wide edge of 45 cm and a narrow edge of 22 cm.

An exploded view of a complete GE1/1 detector is shown on figure 1.10. In the CMS endcap, the GE1/1 detectors are mounted by pair, back-to-back, to form a so-called super-chamber. In total, 72 super-chamber, that is 144 triple-GEM detectors, will be placed in CMS. [10]

Knowing the configuration of the detectors inside CMS, more emphasis can now be put on the different parts forming a complete detector.

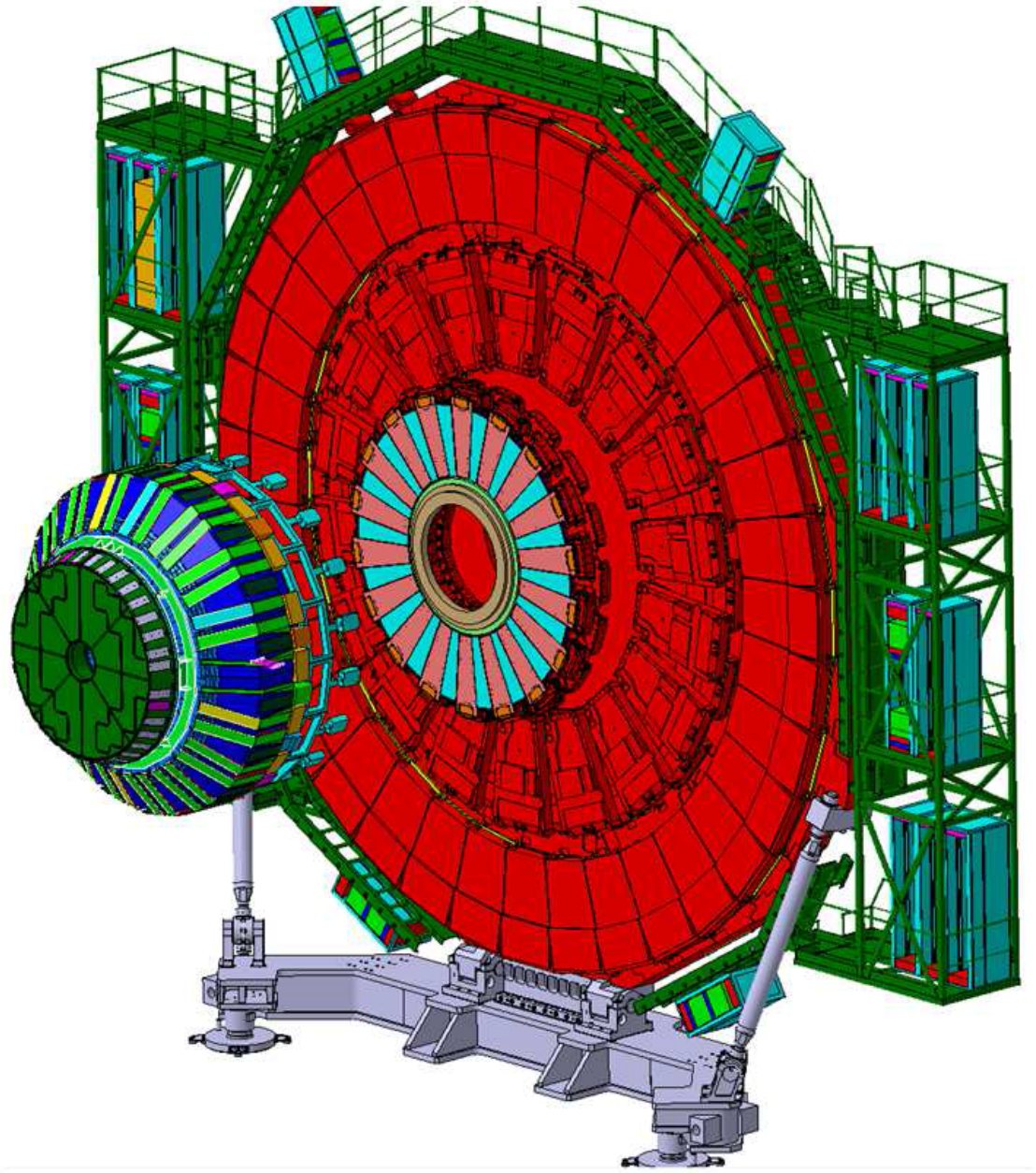

Figure 1.9: The CMS endcap with the triple-GEM super-chambers highlighted in light red and blue.[10]

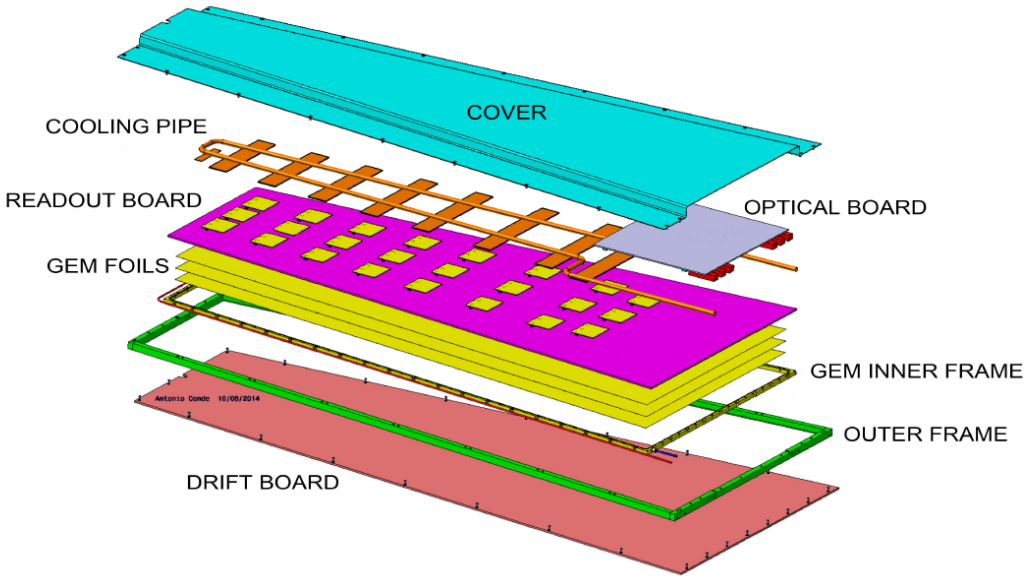

Figure 1.10: The triple-GEM detector. Here the *optical board* is the Opto-Hybrid and the *readout board* groups the actual readout board and the GEB. [4]

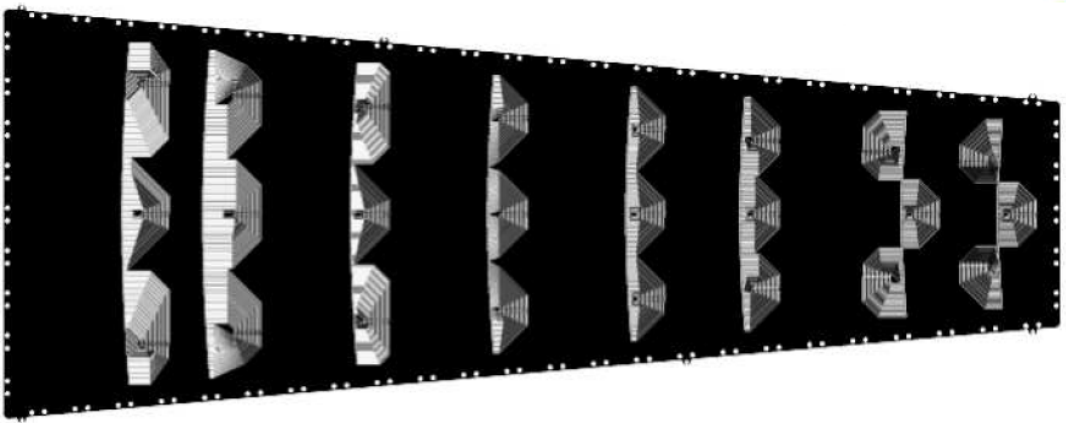

Figure 1.11: The readout board [10]

1.3.3 The readout board and the GEB (GEM Electronic Board)

The readout board is a PCB (Printed Circuit Board) covered of readout strips. These strips are the anodes which the electrons from the avalanche will drift to. The drift of the electrons in the gas will create a current that will be amplified by a preamplifier (recalling the bottom part of figure 1.8).

As illustrated by the figure 1.11, the board is divided in 24 sections gathering 128 strips each so that the signals are concentrated on a connector.

On top of that readout board comes the GEB. Both are connected to each other thanks to a chip called the VFAT which will concentrate the 128 signals and send them to the rest of the acquisition chain through the GEB. The VFAT will be deeply detailed in chapter 2. A picture of the GEB is provided on figure 1.12.

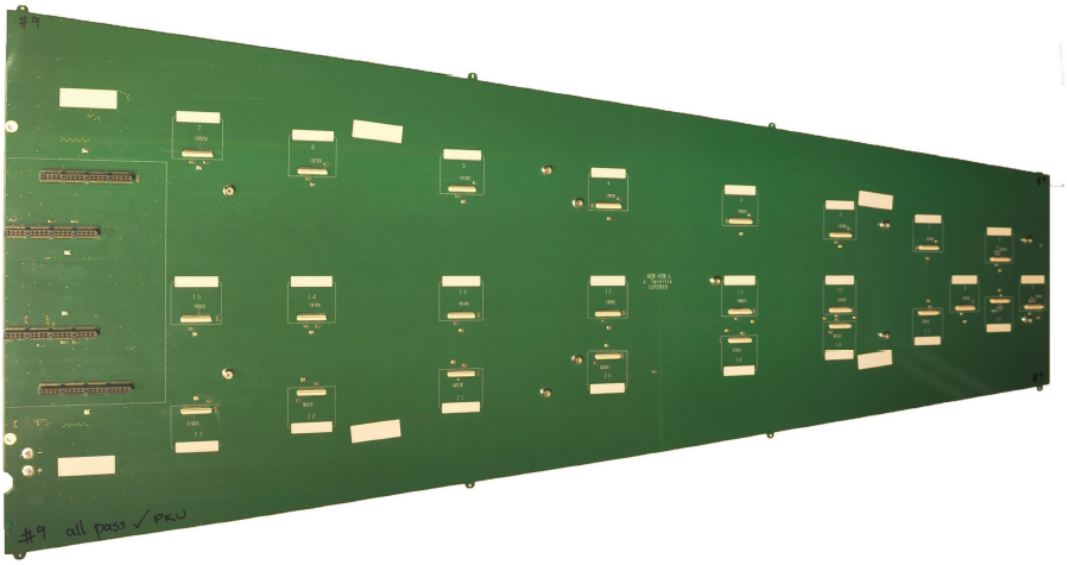

Figure 1.12: The GEB [11]

1.3.4 The Opto-Hybrid

The Opto-Hybrid is a board placed on the wide edge of the GEB and has to communicate with the VFATs. It sends to the latter commands and it gets back the data read by the different VFATs. Those data are centralized and synchronized in order to transmit them to the off-detector electronics for further analysis. The Opto-Hybrid is depicted on figure 1.13.

To fulfil these functionalities, the Opto-Hybrid is based on an FPGA (see chapter 3.

Conclusion To conclude this chapter, figure 1.14 shows CMS opened at the beginning of 2017 allowing, among others, to install a first version of GEM-detectors to perform tests in the real CMS environment. The installed devices are still prototypes, not using the final VFAT chip. However, this installation is essential to prepare the full deployment of GE1/1 during the next Long Shutdown. This thesis is a contribution to the development of the final GE1/1 electronics, in particular its front-end chip, the VFAT, described in the next chapter. For the sake of completeness, extra pictures are available in appendix A.

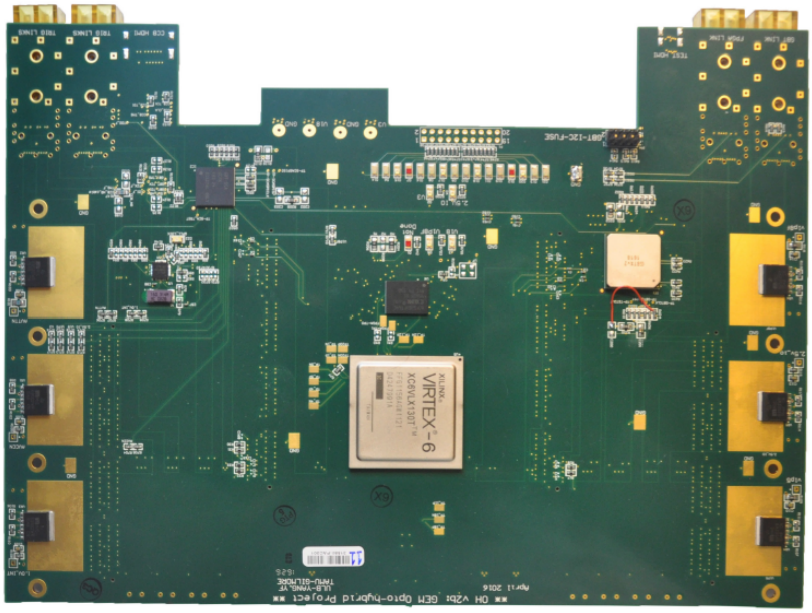

Figure 1.13: The Opto-Hybrid [11]

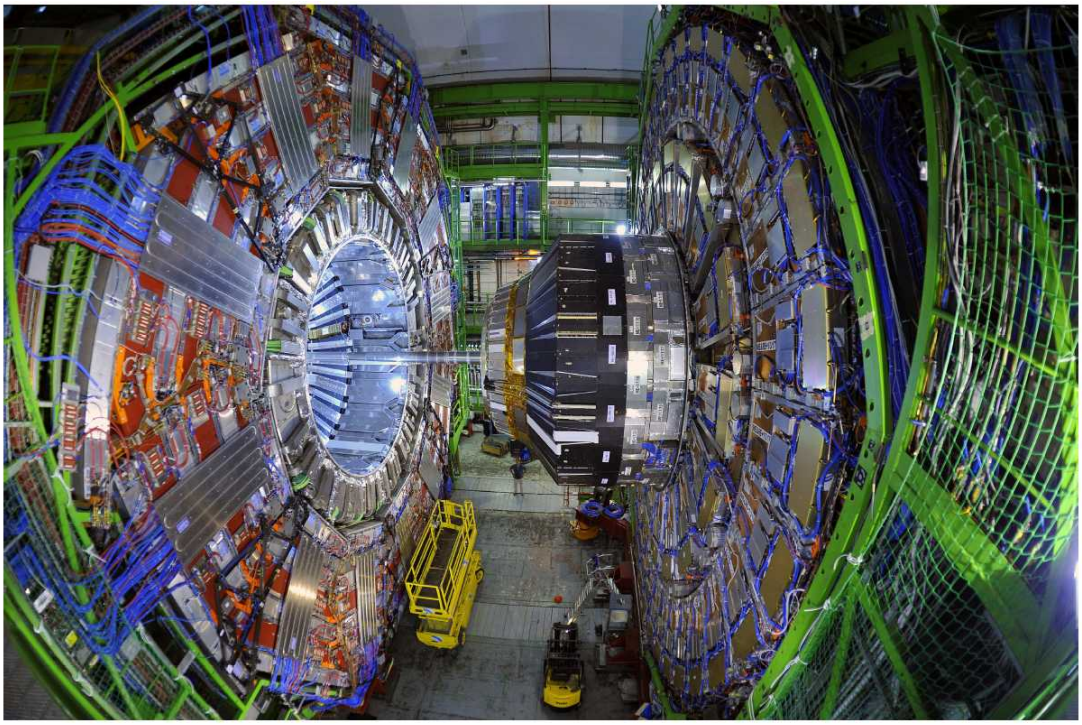

Figure 1.14: The opened CMS. The left side is the barrel while the right side is the endcap. [10]

Chapter 2

The VFAT chips

This chapter presents first the VFAT chip and its features based on the previous version, the VFAT2. Then the changes made in the last release of the VFAT, the VFAT3, will be detailed.

2.1 The VFAT2

The VFAT2 is a trigger and tracking front-end ASIC device designed in 0.25 µm CMOS technology handling two main functions: the first is the *trigger* in order to give fast low granularity data about the muon hit position at the LHC frequency of 40 MHz. These data should be used at the first trigger level LV1 as explained in section 1.2.4. The second is the *tracking* which provides high granularity data for the corresponding triggered event.[12]

2.1.1 Block diagram

The block diagram of the VFAT2 is shown on the figure 2.1.

The VFAT2 has 128 input channels. That is why the readout board has been shaped accordingly by gathering 128 strips in 24 different sections (recall figure 1.11). Each channel has a preamplifier, a shaper and a comparator to digitize the information. The comparator has a programmable threshold in order to determine if a signal should be considered as relevant (1) or not (0). A monostable synchronizes the output at 40 MHz, the LHC running frequency.

After the monostable, two different paths can be distinguished.

The trigger path In this path, a fast OR operation proceeds on the different channels (up to 8 groups of 16 channels). The 8 resulting bits are set on LVDS outputs named S1 to S8 and are transmitted to the off-detector electronics.

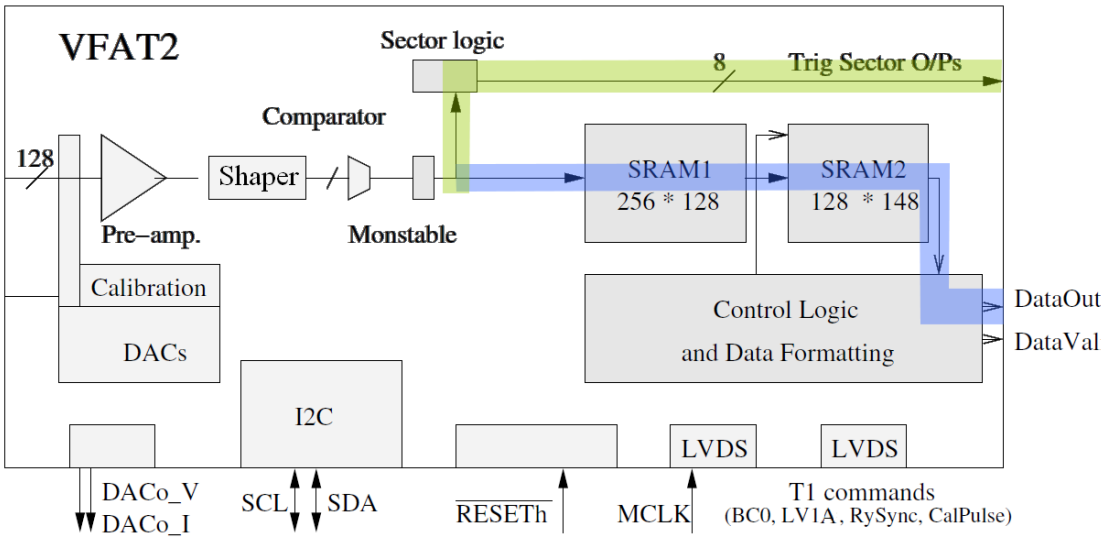

Figure 2.1: Block diagram of the VFAT2. The trigger path is highlighted in green while the tracking path is in blue. [12]

The tracking path Once the monostables provide the data, the 128 bits are immediately stored in parallel in an SRAM memory called SRAM1. Once the off-detector electronics receive the LV1 signal from the trigger path, it will send an LV1A signal (LV1 Accept) back to the VFAT2 if the event is judged relevant in order to extract the tracking data and move it to SRAM2.

In the specifications, the LV1A signal arrival will not exceed 6.4 µs or 256 clock cycles hence the size of SRAM1 (see figure 2.1). About SRAM2, it can store up to 128 triggered events, each sized to 148 bits considering the actual tracking data width plus headers.

As soon as the SRAM2 is filled with data, a read operation is performed and the Data Formatting block streams out the adequate bit stream to the rest of the DAQ chain.[12]

2.1.2 VFAT2 commands

Looking at figure 2.1 again, aside the 40 MHz clock MCLK, the VFAT also gets as inputs the so-called T1 commands, as presented on the figure with the LVDS port on the right.

The VFAT can therefore receive four different commands:

LV1A is the Level 1 trigger Acceptance signal.

CalPulse is a Calibration Pulse.

ReSync resynchronizes all the state machines.

BC0 is the Bunch Crossing[1] identifier.[12]

2.1.3 Inter-Integrated Circuit (I^2C) bus

Finally, the configuration and transmission of data with VFAT2 is done via an I^2C bus. This serial protocol developped by Philips Semiconductors is well-known and allows to communicate easily between multiple electronics circuits.

It uses two bidirectional lines: Serial Clock Line (SCL) and Serial Data Line (SDA) which are self-explanatory. The bus nodes can either be master or slave. The first one starts communication and provides the clock while the slave responds when he is addressed by the master.

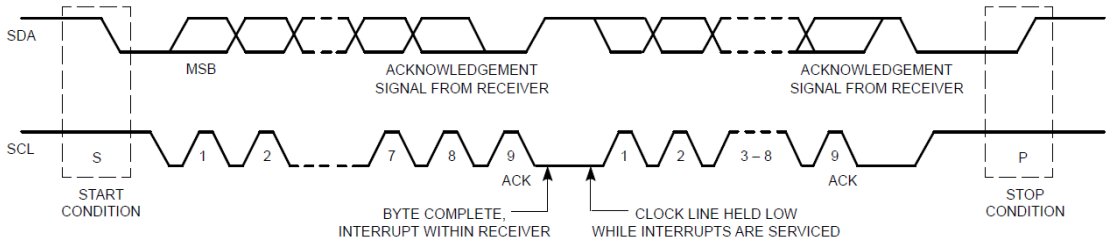

Figure 2.2: Typical example of an I^2C transmission. [13]

A typical transmission is shown on figure 2.2. First, the master initiates communication with a start bit by pulling down SDA while SCL is kept high. Then the data is provided on SDA when SCL is low and read by the slave when SCL is high. The transmission is finished with a stop bit when SDA is pulled high while SCL is high.

2.2 The VFAT3

The concept of the VFAT3 is similar to the VFAT2 (it also has a trigger and a tracking data path). However, this chip has been especially designed to accommodate the future operation conditions of the high luminosity LHC as well as the new constraints of the upgraded CMS detector. The main differences are the increase of performance, the communication protocol and the data formatting block.[14]

[1] A bunch crossing is a commonly used unit at CERN for a clock cycle in the LHC given that two bunches of particles meet each other every 25 ns so it corresponds to the 40 MHz clock

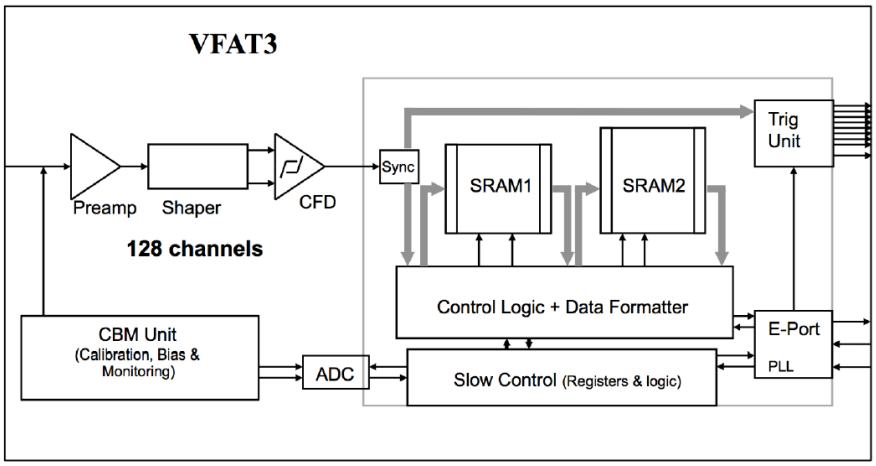

Figure 2.3: Block diagram of the VFAT3.[10]

2.2.1 The performance

Granularity The VFAT3 can provide 64 trigger bits resulting from fast OR operations instead of 8 bits for the VFAT2. It implies an improvement in spatial resolution of a factor 8 at the LV1 trigger.

Time resolution and signal-to-noise ratio (SNR) In triple-GEM detectors, an incoming signal charge can last approximately 60 ns. The preamplifier has to amplify this charge. The latter is similar to a pulsed current source, therefore using a charge-integrating amplifier is suitable for this function (see figure 2.4a). However, this pulse can last very long and deteriorate the time resolution, hence the use of a shaper which is structured by low- and high-pass filters in order to define an adequate *shaping time* (figure 2.4b).[15]

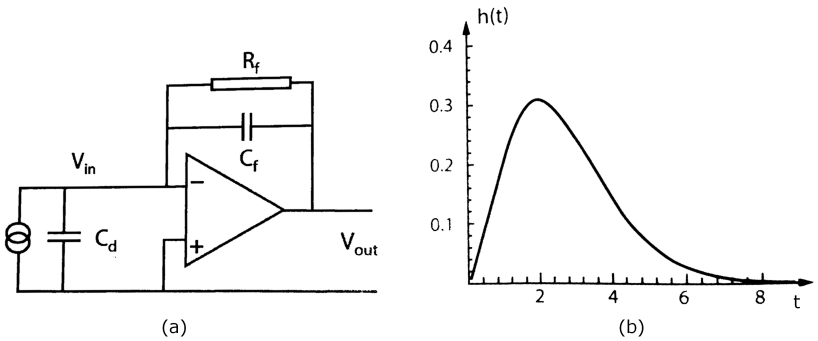

Figure 2.4: (a) Charge-integrating amplifier. (b) Shaping time resulting from a preamplifier and shaper stage. [15]

To get good timing resolution (better than 10 ns), fast shaping time of the signal is needed but it induces a loss of SNR. Indeed, if the shaping time is too fast, *ballistic deficit* can be observed which results in the SNR drop. This is depicted on figure 2.5 with the green curve having a shaping time too short compared to the blue one. This problem is overcome in VFAT3 by using a programmable shaping time (that is 25 ns, 50 ns, 75 ns or 100 ns). [3]

In addition to that, the VFAT2 used a simple *time over threshold* (meaning the time was taken by comparing the signal's amplitude to a given threshold). The drawback is that the time corresponding to the crossover of the signal with the threshold depends a lot on the signal's amplitude. This is called *time walk* as highlighted by figure 2.5 with the red curve having a lower amplitude than the blue one. To get rid of this defect, the VFAT3 implements the Constant Fraction Discriminator (CFD) in its analog front-end which has the property of providing a precise arrival time of the signal independently from its amplitude.

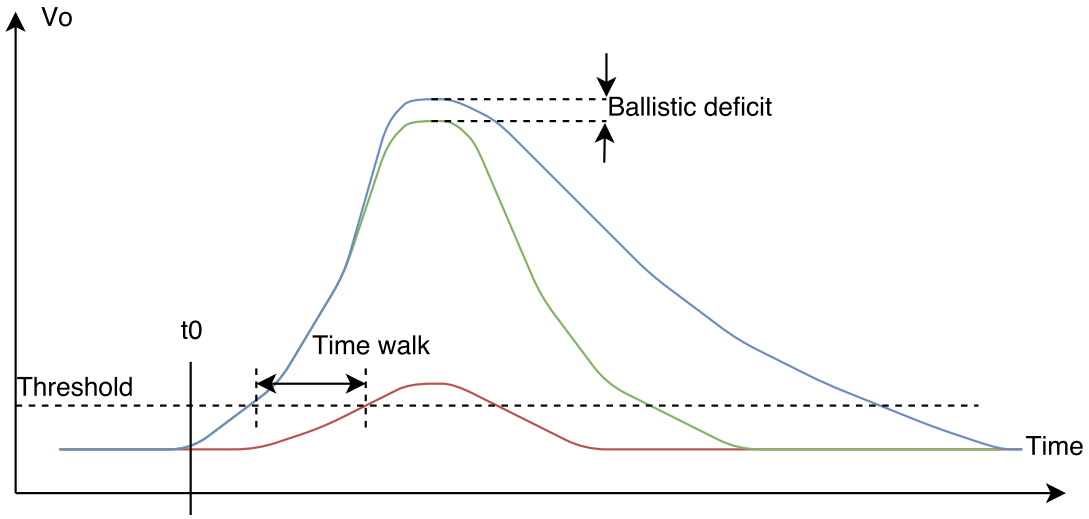

Figure 2.5: Illustration of ballistic deficit (loss of SNR) and time walk (time resolution drop) depending on the shaping time and the signal's amplitude.

The CFD actually takes a first copy of the signal delayed by a time t_{dalay}.

$$t_{delay} = t_{max} - t_k \tag{2.1}$$

t_{max} being the time corresponding to the maximum amplitude of the signal and t_k, the time when the signal has an amplitude equal to its maximum divided by a constant k. [3]

A second signal is taken by dividing the original one by $-k$. The CFD then sums up those both signals. Therefore, this operation has the feature to have its time

zero-crossing independent from the signal's amplitude. The resulting signal can finally be digitized thanks to a Zero Crossing Comparator (ZCC). The principle of the CFD is illustrated on figure 2.6 and 2.7. [3],[14]

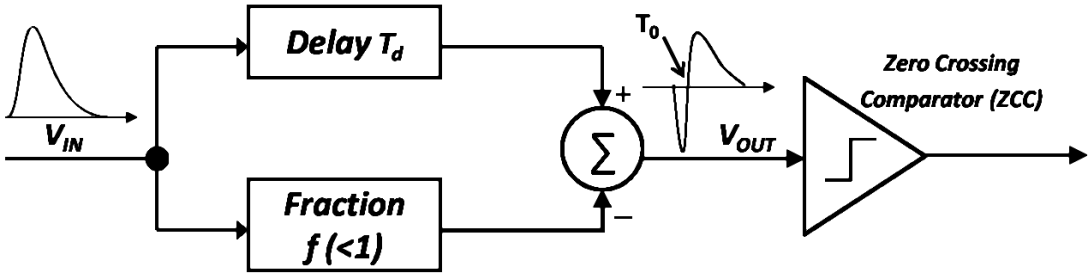

Figure 2.6: Scheme of CFD principle of operation. [14]

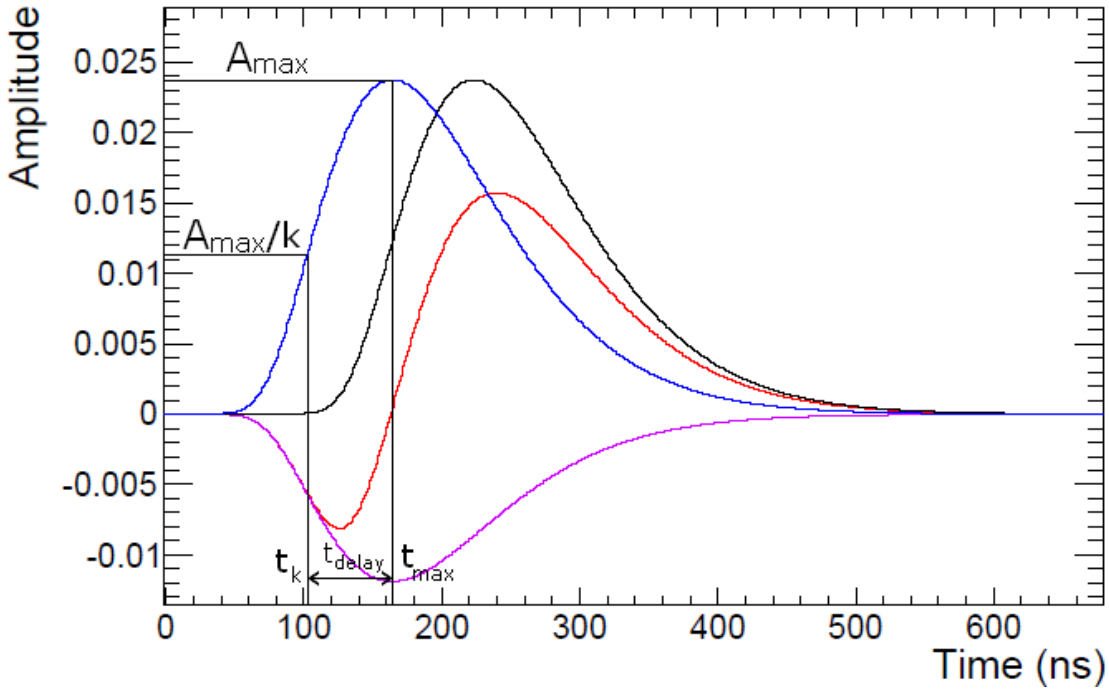

Figure 2.7: CFD principle. The blue curve is the original signal. The black one is the t_k delayed version, the violet is the signal divided by $-k$ and the red one is resulting from the sum of the black and violet curves. [3]

2.2.2 The communication port

Until now, CMS was processing the data and the control commands to each subdetector separately using dedicated optical links. They moved to a new protocol gathering both

links, called the Gigabit Bidirectional Transceiver (GBT) such that each subdetector communicate with this GBT link to a single off-detector electronic system.

To use this protocol, every subdetector needs to comply with the so-called GBTx interface. This is described on figure 2.8. This is why the I^2C protocol is no more used in the VFAT3 and the communication port has been designed instead, in order to take care of the full communication with the VFAT3, including fast control commands, data transactions and bidirectional communication with Slow Control (see next page and later section 3.2.2).

Therefore, the communication port complies with the following functionalities: [16]

- Reception of 320 Mbps serial data and synchronization to the 40MHz LHC clock.
- Detection and decoding of synchronous control commands.
- Separation and prioritized interleaving of data types, detector data and slow control data.
- Transmission of data to the GBTx.

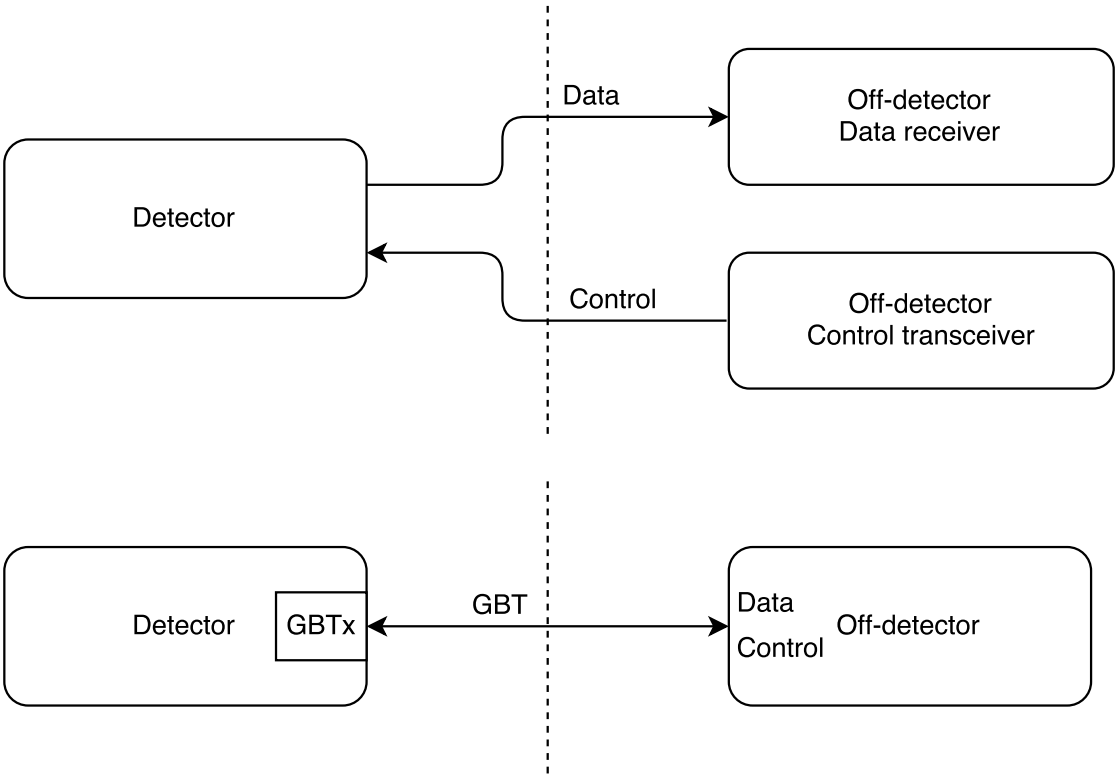

Figure 2.8: Above, data and control packets are dealt independently. Below, GBT protocol handles the bidirectional transmission in a single bus.

It internally uses the Ipbus protocol, which has been designed by the CERN and describes basic transactions for controlling IP-aware hardware devices on a virtual bus.[17]

Reception of data synchronization

The communication port has a 320 Mbps serial data stream which is deserialized in 8-bit packets. Furthermore, a 40 MHz internal clock is derived from the input clock running at 320 MHz.

The phase of that internal clock has to match with the 40 MHz LHC clock. This process starts once the syncronization pattern of three consecutive so-called *comma characters* CC-A is detected (see section 3.2.3). The communication port allows to verify that the internal clock is properly synchronized by detecting another comma character, CC-B. If so, a synchronization acknowledgement is sent back.[16]

Slow Control and Data Formatter communication

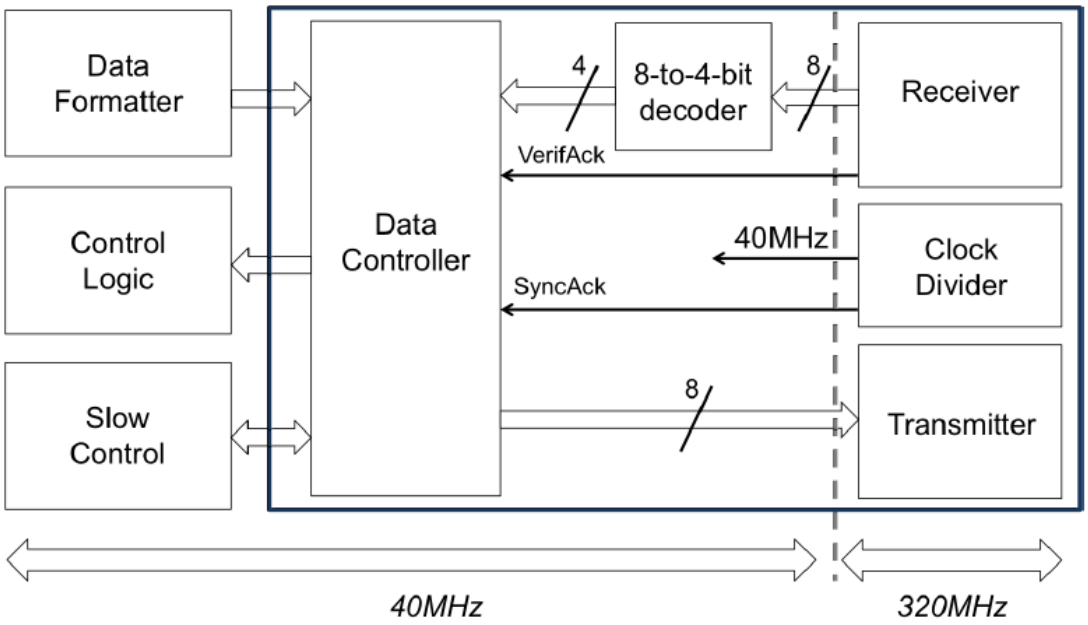

Figure 2.9: Architecture of the communication port [16]

The architecture of the communication port is shown on figure 2.9. The Data Controller block takes care of the communication with the Slow Control and the Data Formatter of the VFAT3 chip. The transmission side of the VFAT3 operates at 320 MHz and a clock divider provides a 40 MHz clock to the chip. A 8-to-4-bit decoder is also implemented for the incoming data (see section 3.2.3).[16]

For communicating with the Slow Control, the High-level Data Link Control (HDLC) protocol is used. Each 0 and 1 of this protocol is encoded in 8-bit words called SC0 and SC1 in the Data Controller before being transmitted to the Slow Control. Therefore, this is, as its name suggests, a high-level encoder/decoder of the data exchanged with the Slow Control. This coding allows an effective bandwidth of 40 MHz with the Slow Control; the I^2C protocol could not afford such a communication speed. Each HDLC packet can encapsulate several Ipbus requests for the VFAT3. Figure 2.10 shows the interface of the Slow Control block and the type of data packet it expects. For the sake of completeness, this interface also provides a Serial Peripheral Interface (SPI) connection in case the communication port would not work so that VFAT3 configuration can still be done.

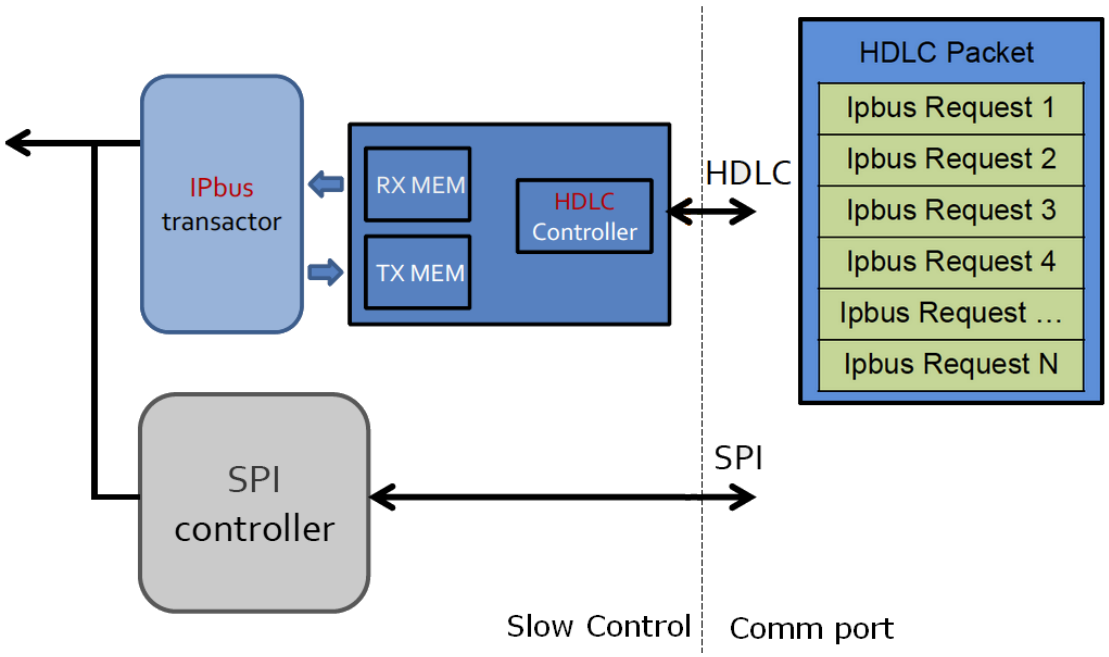

Figure 2.10: Slow Control communication interface and its data packet.

The communication port also interacts with the Data Formatter which provides the high priority tracking data. Therefore, The communication port allows to prioritize the tracking data transmission by interrupting the Slow Control data and resuming it seamlessly. This feature is fully supported by the HDLC protocol.[16]

2.2.3 The data format

Two data formats are available: the first is *lossless* and the second is *Sequential Partition Zero Suppression* (SPZS).

Lossless

The lossless data format was already used in VFAT2 and has been optimized in terms of content: a single header defines the start of packet, a timestamp is given in the form of the Event Counter(EC) or Bunch Crossing Counter(BC) then the data declaring a hit(1) or not (0) for each channel. Finally, a CRC confirms the integrity of the packet (see figure 2.11). [16], [14]

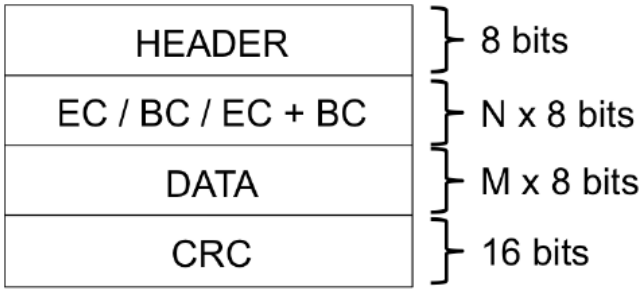

Figure 2.11: Data packet composed of a header, a timestamp, the tracking data and the CRC code. N and M depends on internal chip's settings. [16]

It is possible to only send data when there is a *hit* which allows to use the bandwidth far more efficiently since the chips will register no *hit* most of the time.[14]

Sequential Partition Zero Suppression (SPZS)

By using SPZS data format, the size of the packet is a function of the number of hits. This gives access to the highest possible data transmission rate to the risk of having losses at high occupancy. The 128 channels are divided in 16 partitions of 8 channels. Only the partition corresponding to a given hit will be sent, hence the bandwidth saving when the occupancy is low. In the opposite, the maximum number of partitions per data packet being limited, an overflow may occur therefore causing losses.[14]

Conclusion To summarize, this chapter has thus presented the VFAT chip and detailed the different new features brought to the new VFAT3, namely:

- The VFAT3 uses a a single dedicated communication port for data transactions and slow control commands, at 320 MHz.
- Granularity of trigger bits has been multiplied by a factor 8.
- The chip complies with the requirements of the CMS upgrade, in particular for time resolution and conformity with GBT protocol.

Chapter 3

The VFAT3 test bench

Now that the context of the GE1/1 project and the VFAT3 has been described, we can focus on the work carried out in this thesis and discuss the following points: what is the testing set-up of the chip ? How the VFAT3 will be tested in terms of software and firmware ? What are the tests to realize in order to effectively characterize the chip ? What are the results and what is the outcome for integrating the VFAT3 in the DAQ electronics of the GE1/1 project ?

This chapter will detail the steps which led to an operational test bench of the VFAT3 on a hardware, software and firmware point of view.

As a matter of fact, to characterize the new VFAT3 chip, a dedicated test bench had to be developed, instead of testing the chip on the actual detector as presented in section 1.3.2.

3.1 Hardware testing set-up

The test bench is based around an FPGA development kit and uses several custom boards which have been designed for the project. Figure 3.1 shows a block diagram of the system.

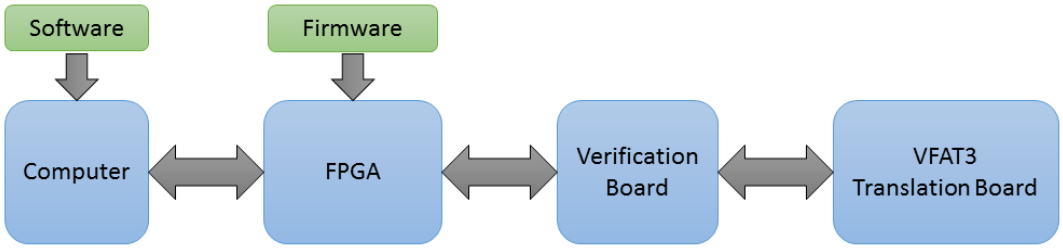

Figure 3.1: Overview of the testing set-up.

The VFAT3 is placed on the so-called translation board providing useful testing points for the chip characterization. Follows the verification board, simulating the tracks on the GEB between the VFAT3 and the FPGA and providing the necessary power supplies to the translation board. Finally, the FPGA board is a Kintex-7 evaluation kit from Xilinx on which the communication firmware detailed in next chapter will be implemented. The set of data to send through the firmware will be generated via software on a regular computer. For more details about the custom boards of the test bench, please refer to appendix B.

The testing set-up is depicted on figure 3.2.

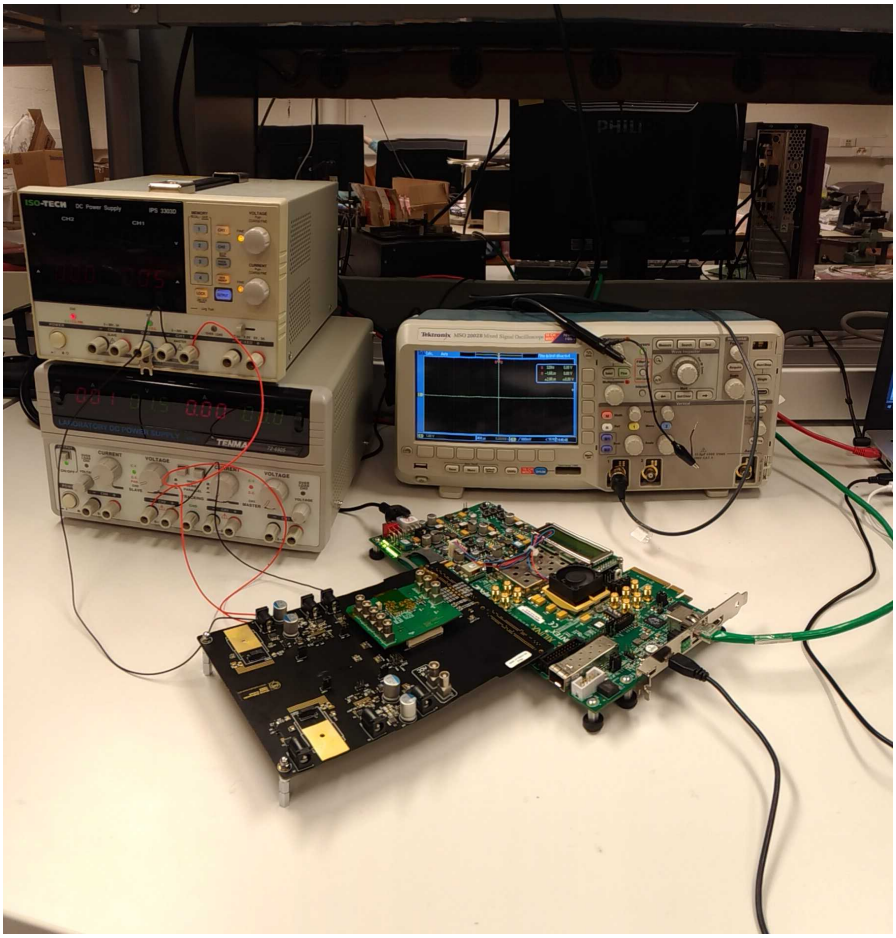

Figure 3.2: Picture of the testing set-up. The small green board is the translation board equipped with the VFAT3 and is supported by the black board (in front), the verification board. This custom board is connected to a green board (behind), the Kintex-7 development kit. Two separate 1.5 V power supplies are used for digital and analog networks. An zoomed in picture is available in figure B.7.

Now, to interact with the chip, it is necessary to implement a firmware and software

interface.

3.2 VFAT3 Firmware

We have seen in section 2.2 that although the VFAT3 and VFAT2 have some common features like the double data path, all the communication from and to the chip is very different. These differences will obviously impact the firmware.

There are also other reasons why the firmware currently used with the VAT2 cannot serve for the new VFAT3. To emphasize the difference, the VFAT2 firmware is briefly described before detailing the VFAT3 firmware which has been developed in this thesis.

3.2.1 Architecture for VFAT2

In early 2017, a prototype of the triple-GEM detector designed with VFAT2 has been implemented in the CMS detector in order to bring a first proof-of-concept of the GE1/1 project. The communication architecture with the VFAT2 was optimized by bringing most of the processing steps on the firmware side, in the FPGA standing on the opto-hybrid, allowing to improve operation timing. [4] This is well depicted on figure 3.3 where we see on the right side, that one single request is sent by the software but every step it implies is processed on the firmware side. Therefore the system's operation is optimized and, only once the process has ended, the resulting data are sent back to the software. This approach is time-efficient and transparent to the software but any transient data will be lost. Unfortunately, such an architecture is not suitable for the characterization of the VFAT3 chips as this leaves few room for debugging the system. This architecture had therefore to be redesigned from scratch to circumvent this loss of flexibility during the chip characterization and to be able to check how the chip is operating between each step, as suggested by the left part of the figure 3.3.

Considering this inadequate architecture and the changes in the VFAT3 presented in section 2.2, the communication and the firmware architecture for the testing set-up has thus been engineered accordingly.

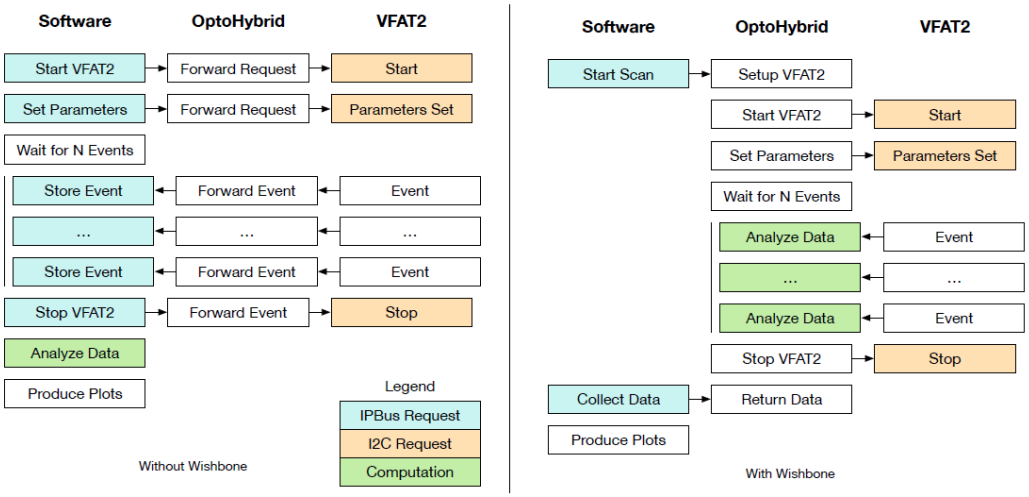

Figure 3.3: Flow of operations on the system with the processing steps concentrated on the software side (left) or on the firmware side (right). [4]

3.2.2 Software command generation

As a consequence, most of the processing steps will be initiated in the software. Therefore, the FPGA firmware will have to transmit the commands and correctly interface with the new communication port of the VFAT3.

The series of commands called Fast Control Commands (FCCs) understandable by the VFAT3 are listed in the table 3.1.

For any request to send to the chip, the software will generate the corresponding set of FCCs. In particular, if we need to communicate with the Slow Control, it will generate a set of SC0 and SC1 forming the entire HDLC packet, as described in section 2.2.2.

To transmit each FCC to the firmware, it has been decided to use an Ipbus interface between the software and the firmware. Each Ipbus packet being 32-bit width, 4 bits are used for the given FCC while the 28 others are used as a time counter called Bunch Crossing difference (BCd). The value of this counter provides the amount of clock cycles to wait before sending the FCC to the VFAT.

The next section will detail how the firmware operates. Then an example of Slow Control transaction will be given to illustrate the communication flow.

Name	Function
CC-A	Synchronization character
EC0	Reset of the Event Counter
BC0	Reset of the Bunch Crossing counter
CalPulse	Injection of a calibration pulse
ReSync	Resets all VFAT3 state machines
SCOnly	Force the *Slow Control only* mode
RunMode	Return from *Slow Control only* mode
LV1A	First level trigger accept
SC0	0 to Slow Control
SC1	1 to Slow Control
ReSC	Reset of Slow Control
CC-B	Synchronization verification

Table 3.1: List of the FCCs

3.2.3 Firmware transmission

The VFAT3 firmware architecture is presented on figure 3.4 and each block is going to be explained below.

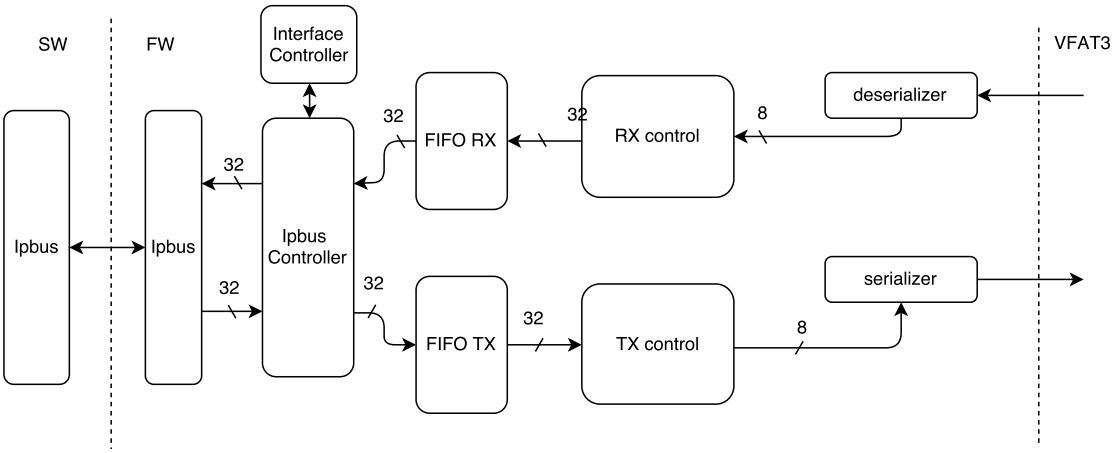

Figure 3.4: Block diagram of the VFAT3 firmware.

Ipbus interface

Software and firmware are interfaced with the Ipbus protocol, the same used for encapsulating Slow Control packets (section 2.2.2). This protocol is developed by CERN and they therefore provide piece of software and firmware interface on which we can base our work. It also has the advantage to contain several transactions in a single packet

and simplify its employment: complexity is kept away from the users (no dealing with resource locks, threading nor even drivers).

Interface controller

The software and firmware interface is dictated by a *control register* which follows a finite state machine as described in table 3.2.

State	**Description**	**Next state**
Idle(00)	Firmware is in stand-by, software can write a series of command in the input FIFO.	Start
Start(01)	Software tells the firmware to start transmitting the commands to the VFAT	Ack
Ack(10)	The firmware acknowledge the request and waits for the output FIFO to be filled in	Send
Send(11)	Tells the software there is data to read, until the FIFO is empty	Idle

Table 3.2: Finite state machine of software and firmware interface control register

Ipbus Controller

This block handles data flow from and to the Ipbus interface using a finite state machine for writing and reading data packets, as detailed in table 3.3 and illustrated by the flowchart available on figure 3.5.

State	**Description**	**Next state**
Idle	Waits for *write* or *read* request	Write or Read
Write	Transmits directly the data to the output	Reset
Read	Request to the firmware data to be read	Ack or Error
Ack	Gives back the data to read	Reset
Error	If there is no data to read available, request is ignored	Reset
Reset	Resets the registers to Idle state	Idle

Table 3.3: Finite state machine of the Ipbus controller

FIFOs

FIFOs are used to store and buffer data coming from the Ipbus towards the VFAT3 and the other way around from the VFAT3 to the software.

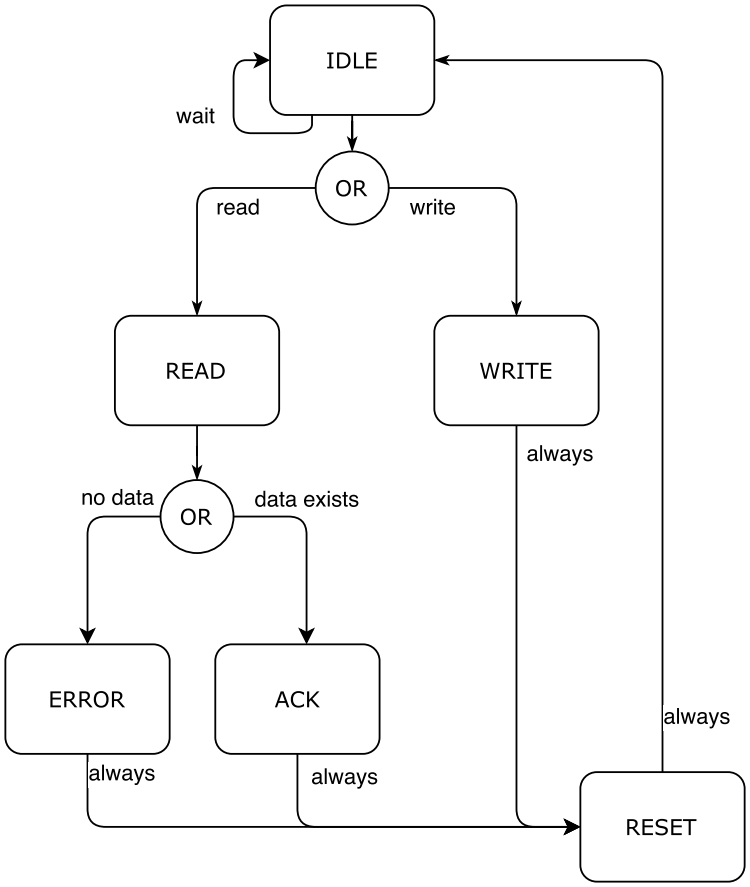

Figure 3.5: Flowchart of the Ipbus controller state machine.

Transmission (TX) controller

As soon as the control register triggers the firmware, the filled FIFO will latch the data packets one after the other at 40 MHz to the TX controller block by respecting their BCd. Each packet is composed as shown in table 3.4. The controller will decrement the BCd until 0 before sending the corresponding FCC to the rest of the chain.

BCd counter	FCC command
28 bits	4 bits

Table 3.4: Composition of the 32-bits data packet coming to the TX controller.

The 4-bits FCC is converted before sending into 8-bits commands following a look-up table, as detailed in table 3.5. When there is no command to transmit, the block sends fillers FCC-A (0x00) and FCC-P (0xFF) alternately to ensure DC balance. In addition to this DC balancing, the conversion provides Single Error Correction (SEC)

and Double Error Detection (DED). [16]

Name	4-bit word	8-bit representation
CC-A	0000	00000000
EC0	0001	00001111
BC0	0010	00110011
CalPulse	0011	00111100
ReSync	0100	01010101
SCOnly	0101	01011010
RunMode	0110	01100110
LV1A	0111	01101001
SC0	1000	10010110
SC1	1001	10011001
ReSC	1010	10100101
LV1A+EC0	1011	10101010
LV1A+BC0	1100	11000011
LV1A+EC0+BC0	1101	11001100
EC0+BC0	1110	11110000
CC-B	1111	11111111
FCC-A	-	00000000
FCC-P	-	11111111

Table 3.5: Transmission codes provided by the 4-to-8 bit converter

Serializer and deserializer

The 8-bit command is then serialized and sent to the VFAT3 at 320 MHz.

The deserializer does the reverse process. As highlighted in figure 3.4, a synchronizer block exists for the deserializer. To make sure the deserialization is sampled correctly, a *bitslip* parameter allows to shift the output data if necessary. As the VFAT3 sends fillers character when there is no data, the synchronizer will use the bitslip until recognizing the fillers once the system is turned on.

Reception (RX) Controller

The readout is completed by a filter block which drops the filler characters from the VFAT3 in order to only retain the meaningful data to the output FIFO. The data coming from the VFAT3 contain a header described in table 3.6.

FCC	8-bit representation	Function
SC0	10010110	Slow Control 0
SC1	10011001	Slow Control 1
F1	01111110	Filler 1
F2	10000001	Filler 2
SyncAck	00111010	Synchronization acknowledge
VerifAck	11111110	Verification acknowledge

Table 3.6: List of the headers from the chip

3.2.4 Slow Control transaction illustration

Let us illustrate with an example.

Let us imagine the user wants to configure a register in the Slow Control. As depicted on figure 3.6, the software will generate the data by packing it in an ipbus request, itself encapsulated in an HDLC packet. Each bit of that packet is encoded as a SC0 or SC1. To send the data to the firmware, a second Ipbus encapsulation is applied for the transmission and directly decapsulated while entering the firmware. Each FCC (SC0 or SC1) will then simply be converted in 8-bits commands and serialized to the VFAT3. Finally, the HDLC and Ipbus layer will be decoded by the Slow Control interface.

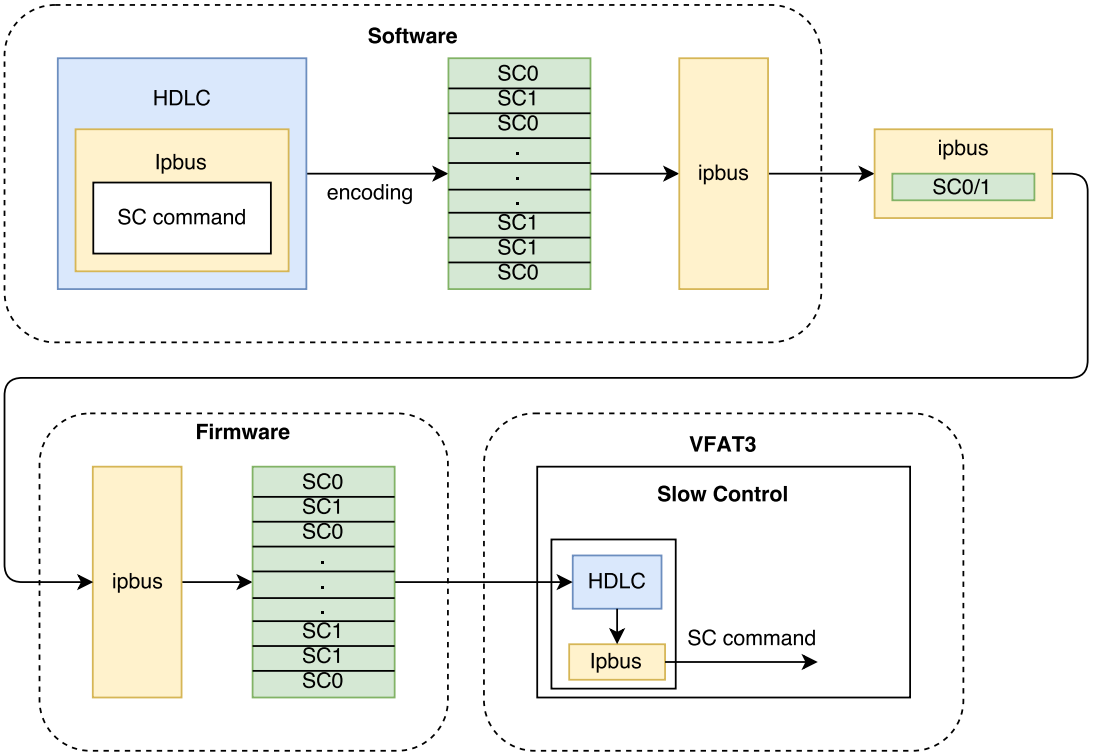

Figure 3.6: Example of a Slow Control transaction.

Conclusion To conclude this chapter, the VFAT3 test bench has been defined on a hardware point of view with the different custom boards and the FPGA development kit around the VFAT3 chip but also in terms of software and firmware where a new architecture has been defined and developed from scratch in order to have a system convenient for debugging the chip.

Chapter 4

Digital functional testing

Now that the test bench has been developed, a series of tests has to be performed in order to characterize the VFAT3 chip. This chapter focuses on the digital features of the chip by stating each test achieved and their results.

4.1 Powering the chip

Although straightforward, the chip first has to be powered on and we must verify if it is running in a normal state, namely the *SLEEP mode*, by checking for instance if the VFAT3 is sending filler characters as it is supposed to.

Results Unfortunately, once the chip was powered on, it was not sending anything. After investigation, it has been found out that the chip was stuck in resetting itself. The problem was coming from the Power-On-Reset circuit which provides the reset pulse to the chip. The only way to circumvent this issue was to force disabling signals available in the chip and feeding this circuit (namely $POR\_DISABLE$ and $BOR\_DISABLE$). Afterwards, the chip worked properly as proved in next sections.

4.2 The communication port

The communication port is the interface in charge of sending and receiving data between the FPGA and the chip. It is therefore, for sure, the first module to test as, without it working, the chip simply could not be used at all.

In order to verify the communication port, a synchronization pattern corresponding to three consecutive CC-A has been sent to the VFAT3 to synchronize its internal clock with the one provided by the firmware. It will respond with an acknowledgement signal

which must be verified. It is also possible to verify this synchronization by sending one CC-B and checking back the response again.

Results Relying on section 3.2.3, after writing 3 CC-A in the TX FIFO, the user asks the firmware to start the transmission by editing the control register (table 3.2). The resulting data flow is illustrated on figure 4.1. After 3 clock cycles, the VFAT3 receives 3 consecutive 0x17, corresponding to the 8-bits conversion of the CCA command (table 3.5). As expected soon after, after 14 clock cycles, the VFAT3 responds with the SyncAck packet (0x3a – table 3.6).

Apart from the synchronization transmission, we also see, as intended, the fillers sent alternately by the firmware (0x00 and 0xff). The same applies from the VFAT3 to the firmware (0x7e and 0x81).

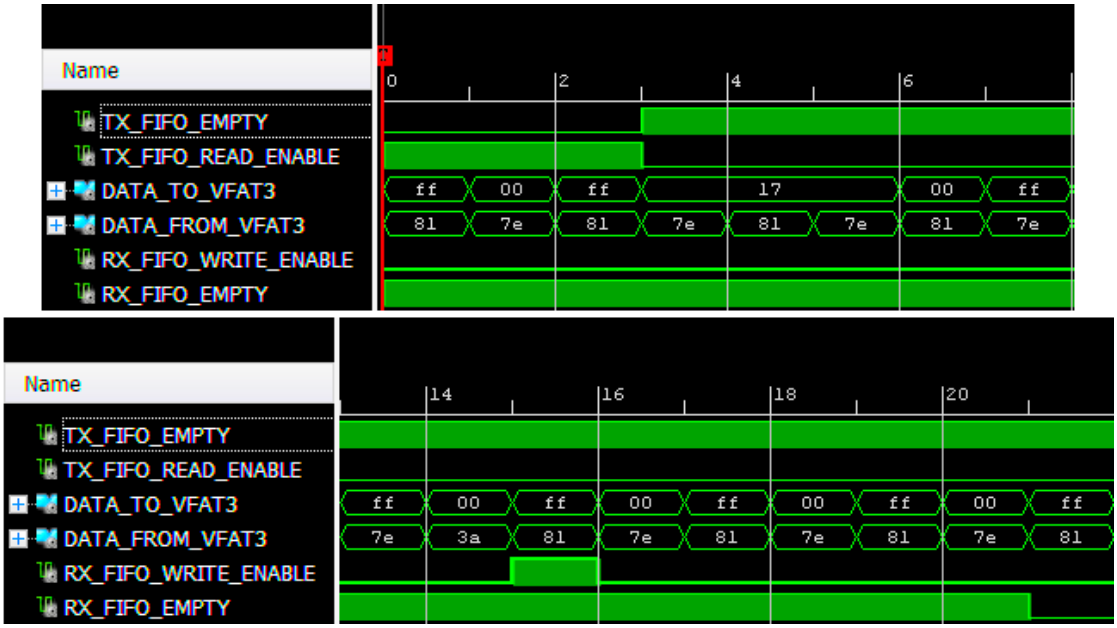

Figure 4.1: Illustration of the VFAT3 synchronization.

The verification of the synchronization has also been established by sending a CC-B command. Figure 4.2 shows its 8-bit equivalent (0xe8 – table 3.5) sent to the VFAT3 and the expected response of the latter (0xfe – table 3.6).

The communication port has therefore been verified and operates as desired.

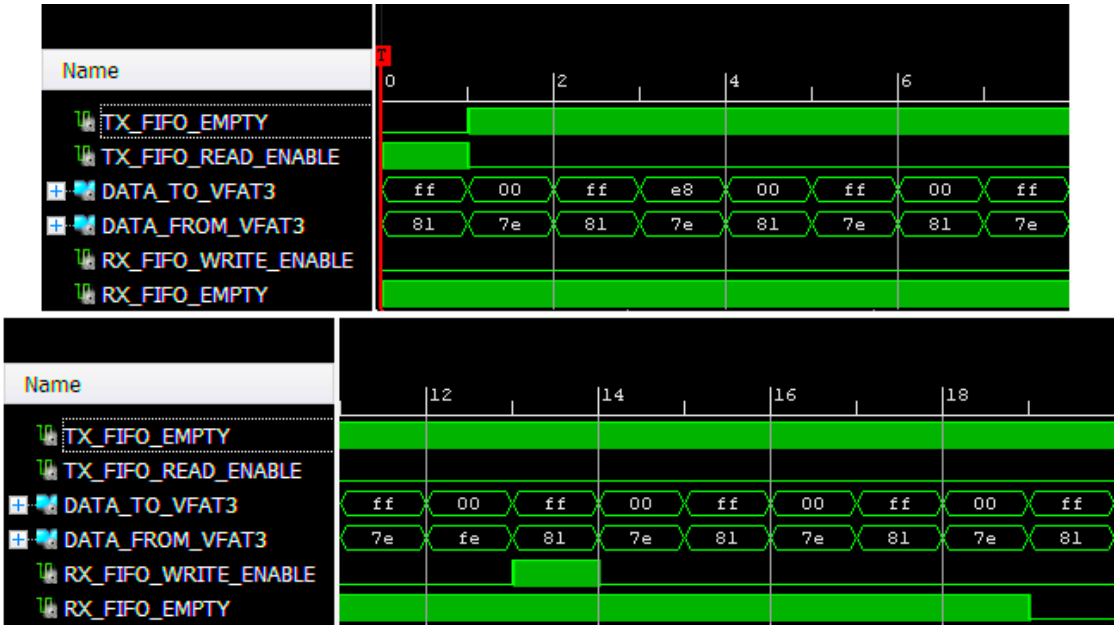

Figure 4.2: Illustration of the synchronization verification.

4.3 Slow Control communication

Once the communication with the chip is established, the next step is to configure its front-end using the Slow Control. This can be done in *SLEEP mode*: in this state, only the Communication port is awake and Slow Control registers can be configured but the changes are not applied yet. Once this is achieved, turning the *SLEEP bit* off to move the VFAT3 in *RUN mode* will start the internal state machines and apply the configured biasing to the analog front-end.

For testing this module, an idle Slow Control transaction can be sent and the response given back from the VFAT3 will confirm it is operating properly.

Results The idle request and response are defined by the Ipbus protocol [18] and the VFAT3 has proved to be able to understand the idle request and give back the expected response.

4.3.1 Priority System

As explained in section 2.2.2, the chip features a priority system allowing to suspend Slow Control transactions to give priority to the tracking data once available. This operating mode is defined by the fast command RunMode. Initially, the chip has to be configured and is therefore only taking care of Slow Control transactions as set by the fast command SCOnly, ignoring the tracking data.

Results These modes have been proved to work properly and were used extensively during the self-trigger testing, for instance (section 4.3.3).

4.3.2 Power Consumption

Once the VFAT3 is turned on, it remains in *SLEEP mode* in order to let the user configure it before going into *RUN mode*, as explained above. In this state, Slow Control transactions can operate and the VFAT3 will send fillers F1 and F2 alternately. This has already been verified with the Communication port synchronization but as the *SLEEP mode* is a minimum power consuming state while the *RUN mode* implies the full chip starts working, it is appropriate to evaluate the power consumption of both states. Table 4.1 shows the current consumption of the chip in both mode for the digital and the analog networks, each supplied with a 1.5 V voltage source.

Mode	SLEEP bit	Digital current	Analog current
SLEEP	1	45 mA	50 mA
RUN	0	60 mA	150 mA

Table 4.1: Power consumption of the VFAT3 chip in *SLEEP* and *RUN mode*.

The power consumption on the analog front-end was bounded to 2.5 mW per channel, that is 320 mW in total while we actually have here 225 mW in RUN mode.

4.3.3 Self-triggering and Event Counter

The VFAT3 chip has the capability to send a calibration pulse (CalPulse) to itself in order to trigger its channels by its own for calibration purpose. As explained in section 2.1, once a hit is detected, the tracking data is stored in SRAMs and a LV1 trigger is sent. If the hit is relevant, knowing the latency between the hit and the reception of the LV1A, the corresponding tracking data will be delivered out of the chip. Each time a LV1A is received, the Event Counter (EC) will increment. Testing this functionality means we can self-trigger the channels and execute more complex scan routines on the chip.

Results CalPulse have been sent repeatedly on one channel of the VFAT3 with LV1A separated with a latency of 3 BC. Note that this latency is particularly low because of the testing setup; it will be higher in real situation on the GEB. The VFAT3 was therefore sending back the EC incrementing and the corresponding data, as shown on figure 4.3. This test has been successful for every channel. The chip was therefore ready for any more complex scan routines using self-triggering.

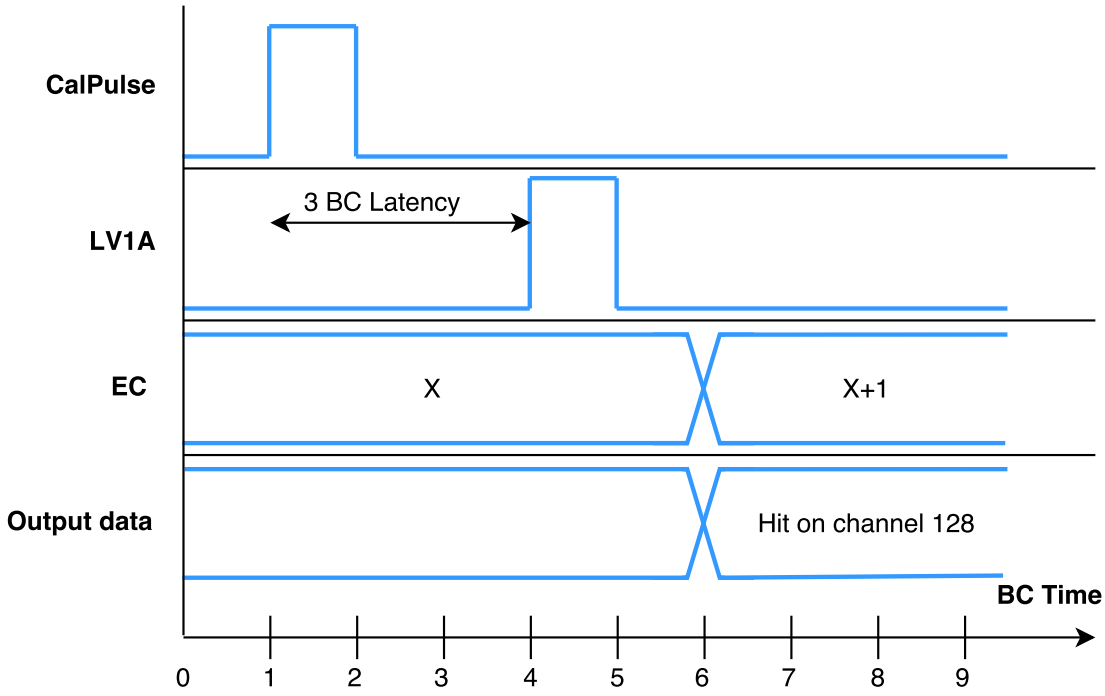

Figure 4.3: Self-triggering of a VFAT3 channel. After LV1A, EC increments and the output data gives the 128-bits tracking data corresponding to the hit. In this case, only the 128th bit is 1.

4.4 Digital signals quality

The VFAT3 and the FPGA are not using the same standard voltages. FPGA provides Low Voltage Differential Signaling (LVDS) signals while, moving to ever higher frequencies has led the VFAT3 to reduce the voltage amplitudes by using Scalable Low Voltage Signaling (SLVS) ports. A conversion between those standards thus also had to be implemented on the transmission lines. A summary of the specifications of those both standards are shown in table 4.2.

Voltage	LVDS	SLVS
Common mode	1.2 V	600 mV
Output swing	800 mV	500 mV

Table 4.2: Common voltage and output swing (peak to peak) levels for LVDS and SLVS technologies.

Therefore, SLVS signal quality has been verified. You can see on figure 4.4 a first eye diagram corresponding to the SLVS 320 MHz clock sent to the chip. However such a fast signal reveals some jitter and slow edges.

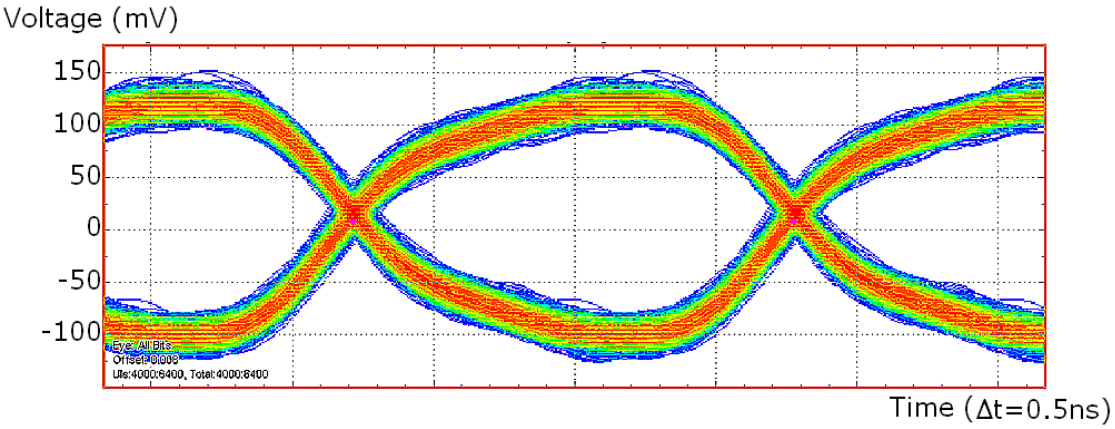

Figure 4.4: Eye diagram of the SLVS 320 MHz clock received by the VFAT3 chip using a low-quality probe.

Therefore a better probe has been used with a lower capacitance and reducing the mutual inductance. The resulting eye diagram has improved: figure 4.5 compare the LVDS signal with the SLVS signal. Both eye diagrams are clearly defined.

The same verification has been done on the data path sent to the VFAT3 and containing fillers 0x00 and 0xff. The eye diagrams are shown on figure 4.6 and show no defect.

Then the data coming from the chip have been evaluated. Figure 4.7 shows the signal received and corresponds well to what is expected (fillers 0b10000001 and 0b01111110). However, we see lowly damped oscillations on the edges of the signal.

This is confirmed by looking at the figure 4.8 which may impact the understanding of the date by the FPGA. However, by intensive digital testing, no failure were detected. The current hypothesis is that this 320 MHz signal is measured with test points on the custom boards in the middle of the transmission line, provoking reflections and disturbing the signal's quality. Measuring the signal closer to the line termination would then get rid of those defects, explaining why the FPGA has no difficulty to understand the data. Unfortunately, the Kintex-7 evaluation kit does not provide such test points.

Comparing the different diagrams above, we can distinguish difference in output swing for the SLVS signals. Indeed, the transmitted clock and data (figures 4.5 and 4.6) to the chip are converted from LVDS thanks to a passive resistor bridge while the data sent back by the VFAT3 is basically already in SLVS format (figure 4.8). Therefore we can witness a drop of the amplitudes caused by the resistor bridge. However, as the VFAT3 fully understands the data sent, characterization has been carried on and adjusting the resistor values is postponed for the next prototype.

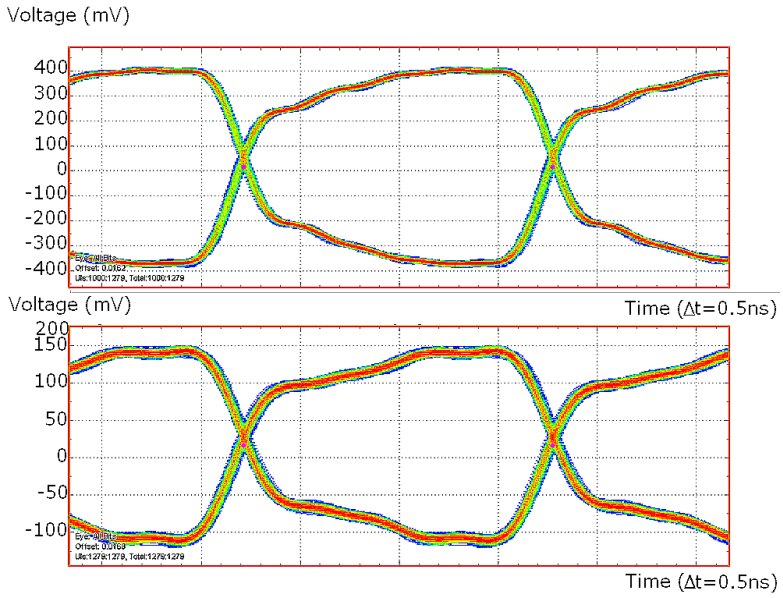

Figure 4.5: Eye diagram of the LVDS (top) and SLVS (down) 320 MHz clock received by the VFAT3 chip.

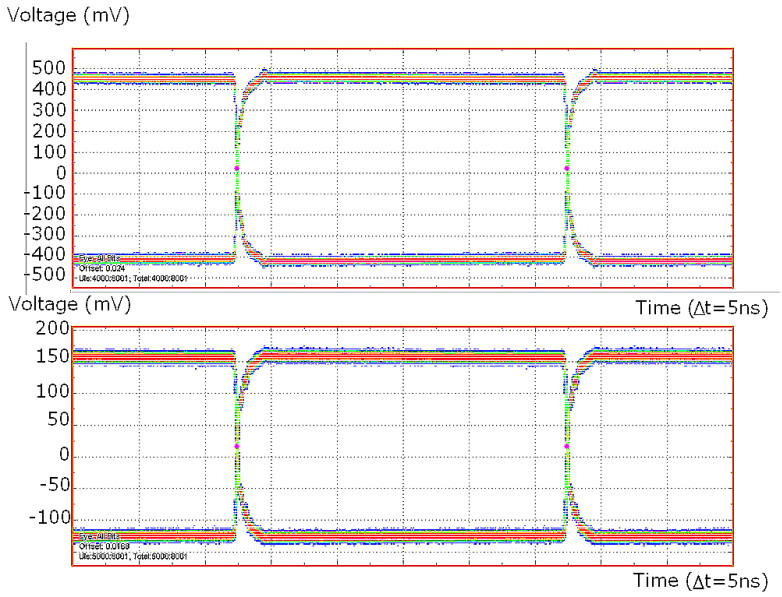

Figure 4.6: Eye diagram of the LVDS (top) and SLVS (down) data signal received by the VFAT3 chip.

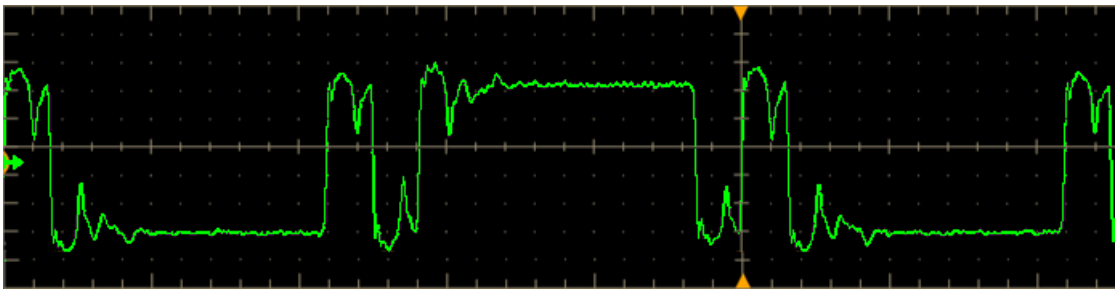

Figure 4.7: Behaviour of the data signal transmitted by the chip.

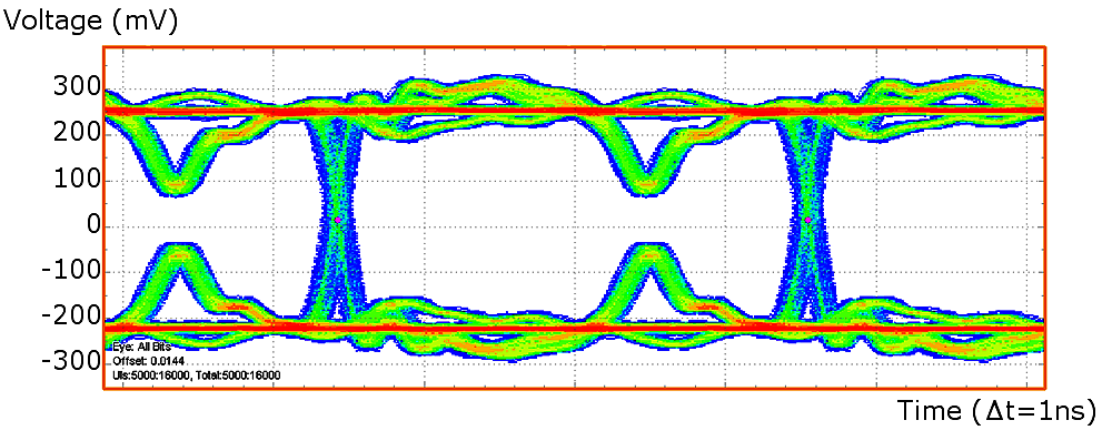

Figure 4.8: Eye diagram of the data signal transmitted by the VFAT3 chip.

4.5 SRAMs and Single Event Latch-up

A bit apart from the VFAT3 digital tests, two other CERN groups have reported a potential problem with radiation for two different chips produced with the same technology, at the same time than the VFAT3, in particular its SRAMs. These groups have recently observed Single Event Latch-Up (SEL) on those designs.

SEL is an uncontrolled current flow between the power supplies because of a so-called parasitic *Silicon Controlled Rectifier* (SCR) circuit existing in bulk CMOS technologies, as illustrated on figure 4.9.

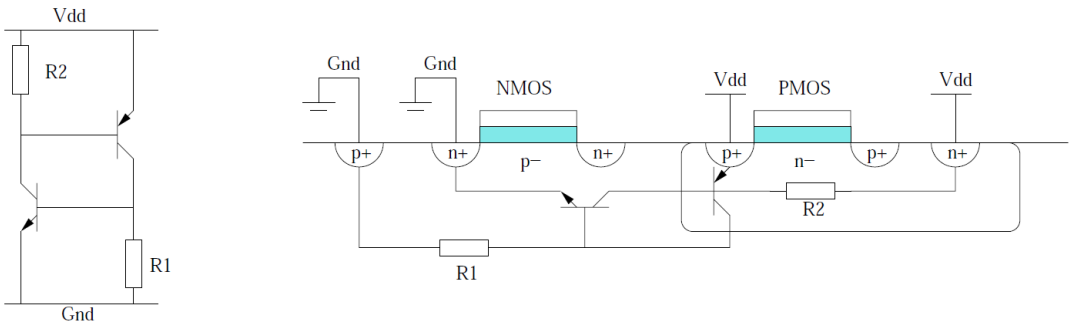

Figure 4.9: SCR circuit (left) and parasitic SCR in bulk CMOS (right). [19]

The SCR circuit presents a positive feedback between the two bipolar transistors. As long as they are off, the circuit will remain stable but in radiation environment, carriers may be injected into the base of one bipolar transistor and provoke the unstable reaction. Therefore, the power supplies are short-circuited, resulting in dramatic failure. [19]

In order to reduce the probability of SEL, design engineers have defined the rule to keep R_1 and R_2 as low as possible by increasing the number of substrate contacts within a minimum distance from the MOS transistor. [19]

Despite that both designs cited above have followed these design rules, SEL has nevertheless showed up and it is expected the same defect come up with the VFAT3 during the upcoming radiation testing. For this reason, other SRAMs will have to be selected to replace the existing ones for the final release of the chip.

Conclusion To conclude this chapter, the digital functionalities have been tested successfully. The quality of the signals in the front-end of the chip has also been verified and the translation from LVDS to SLVS signals has been analyzed.

However, one defect has been discovered about the Power-On-Reset circuit of the chip preventing it from leaving its reset state. Hopefully, this issue could be bypassed in order to carry on the characterization. On the other hand, the potential issue of SEL occurring in VFAT3's SRAMs move towards the need of a new release of the chip.

Chapter 5

Analog functional testing

Beside the digital part, the behaviour of the analog signals is critically important as this is where the input signal from the detector is amplified, shaped and digitized for the rest of the DAQ electronics.

5.1 VFAT3 front-end

As explained in the previous chapter, once the VFAT3 chip has been configured properly, the front-end can in turn operate.

Recalling the block diagram of VFAT3 in figure 2.3,a zoom can be done on the front-end of the 128 channels, depicted on figure 5.1. It is composed of a preamplifier, a shaper, a single-to-differential amplifier and the CFD.

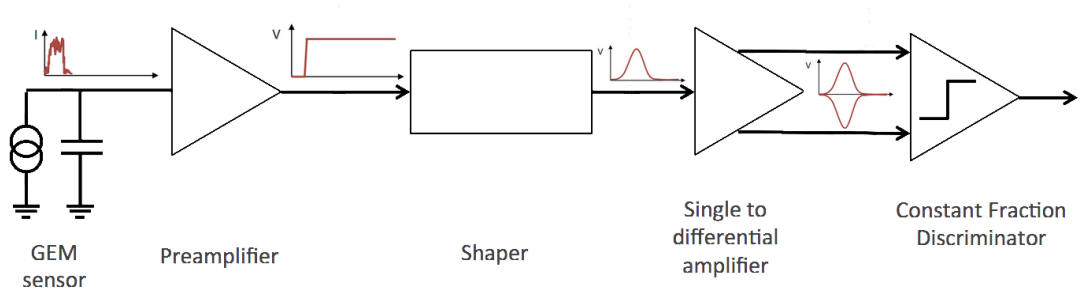

Figure 5.1: Front-end of a channel inside the VFAT3 chip.

5.1.1 Preamplifier

The input of the amplifier receives a pulse equivalent to the charge arriving from the detector on the corresponding channel. Its amplitude is too low for the probes used

to display it on an oscilloscope but the output of the preamplifier stage is shown on figure 5.2. You can see the shape of the resulting charge integration as explained in section 2.2.1.

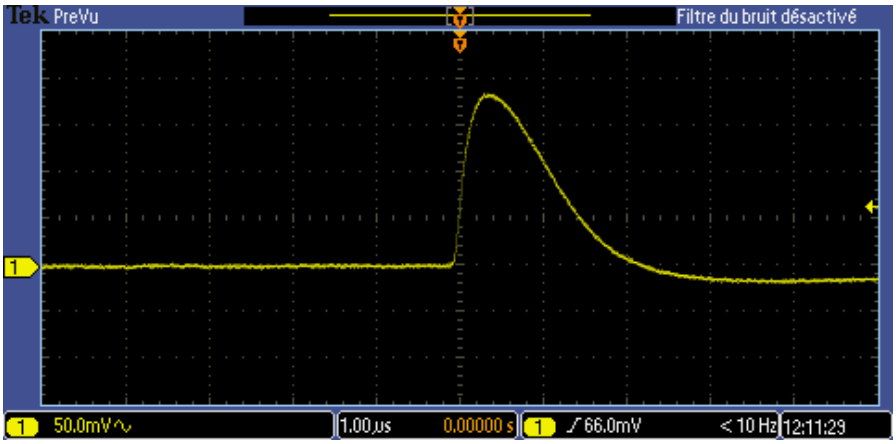

Figure 5.2: Preamplifier response to a calibration pulse corresponding to an input charge

5.1.2 Shaper

As we discussed in section 2.2.1, the signal needs good time resolution. To adjust that, the shaper is composed of several RC and CR stages in order to shape the edges of the signal. The operation is illustrated on figure 5.3, where we can see that the output pulse duration is much narrower.

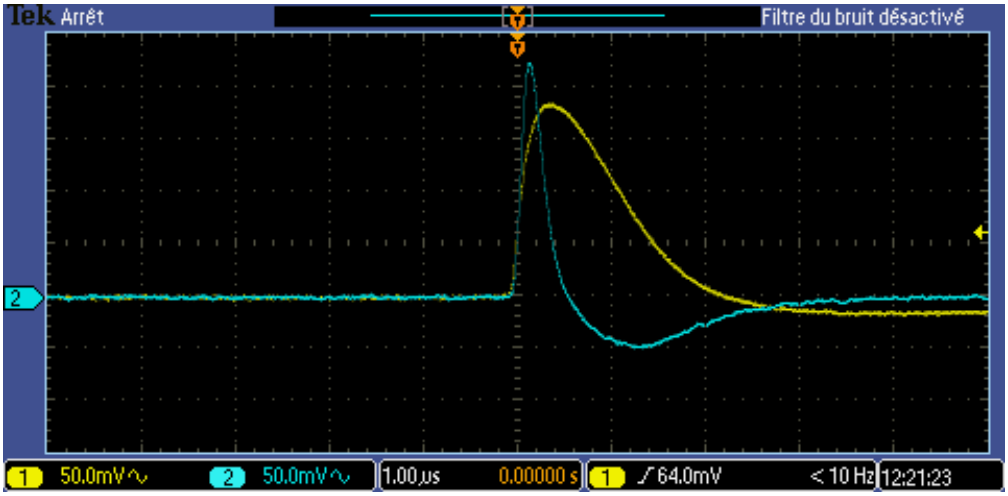

Figure 5.3: Output of the preamplifier is directly connected to the shaper input (yellow) and the response from the shaper (blue) is far more narrow in time.

5.1.3 Single-to-differential amplifier

This stage is simply converting the signal from the shaper in a differential one for entering the CFD. The operation is depicted on figure 5.4.

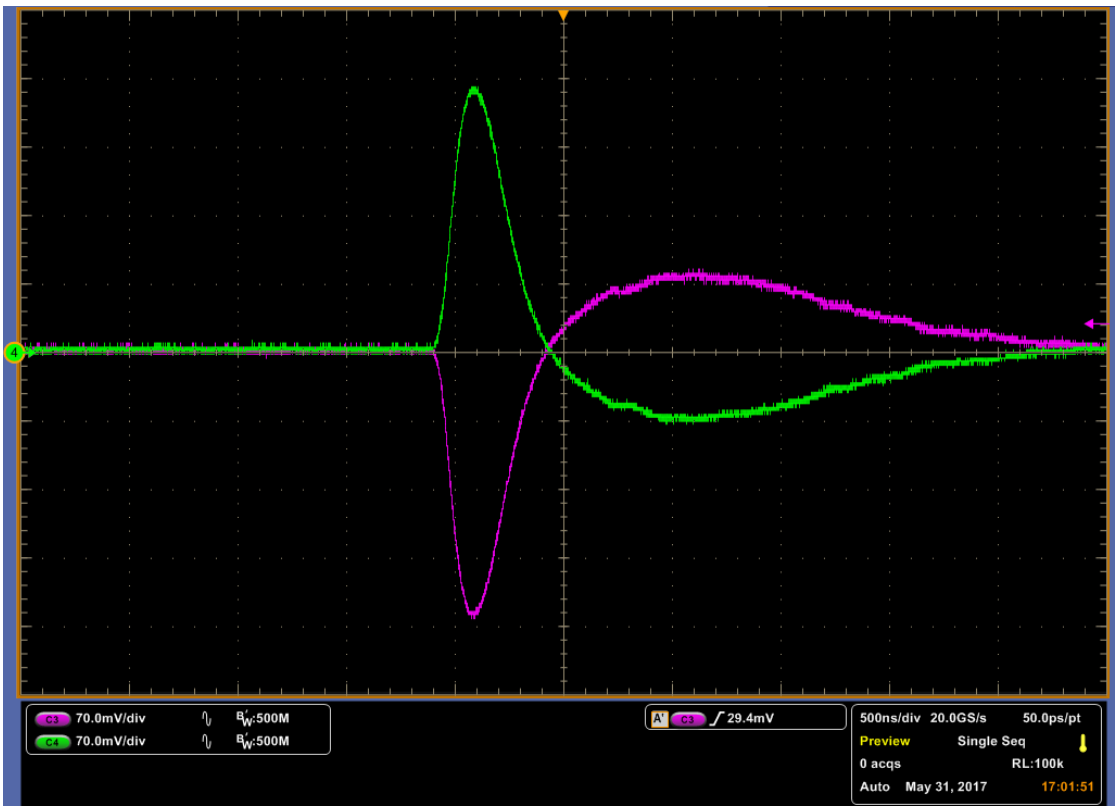

Figure 5.4: Output of the single-to-differential amplifier.

5.1.4 CFD

Then, the differential signals enter the CFD in order to provide a time resolution independent from the signal's amplitude. Figure 5.5 shows the resulting pulse starting at the zero-crossing of the invariant signal discussed in section 2.2.1 and figure 2.7. A study of the CFD time resolution efficiency is currently under progress.

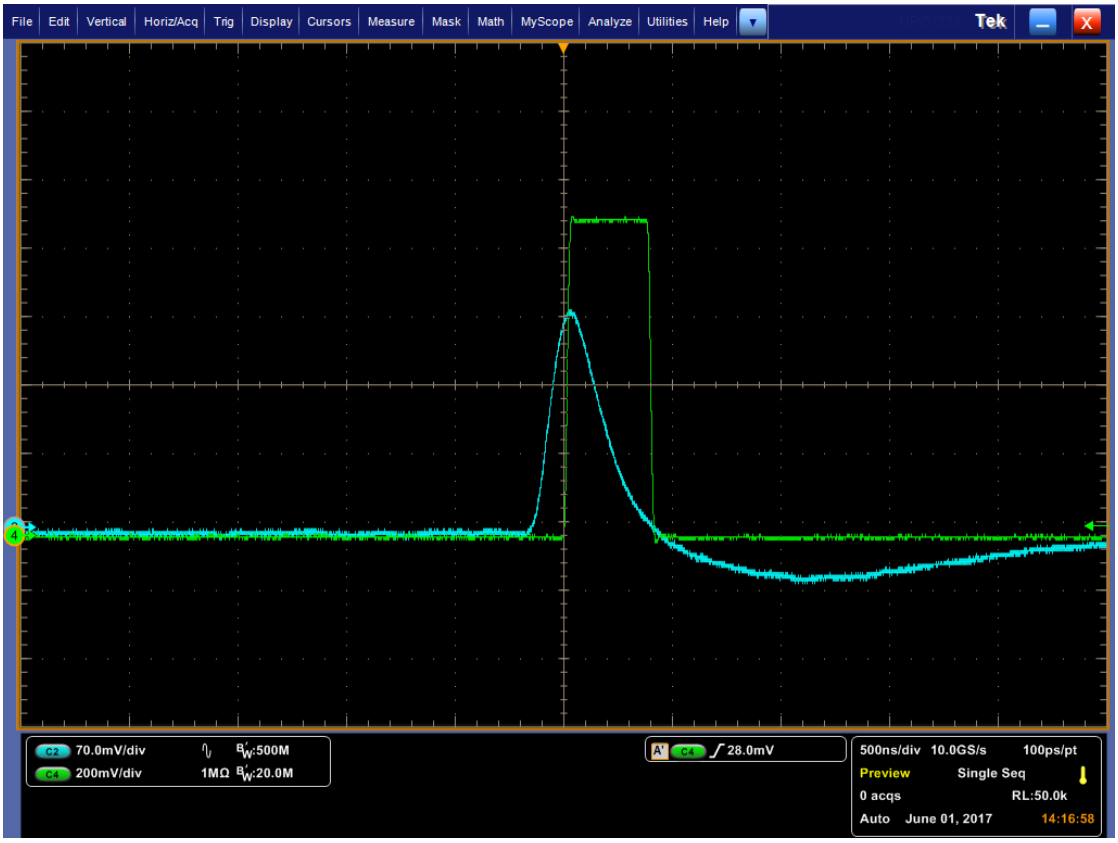

Figure 5.5: CFD operation with the positive differential input(blue) and the CFD output(green).

5.2 S-curves and noise characterization

5.2.1 Principle

The S-curve is a scan routine allowing to characterize the noise behaviour on a channel of the VFAT3 chip. It consists in scanning the ratio of *passing event* for increasing input pulse amplitude with respect to a given threshold. [8] This gives an S-shape

to the resulting curve, hence its name. Figure 5.6 shows an S-curve example for one channel of a VFAT2 chip.

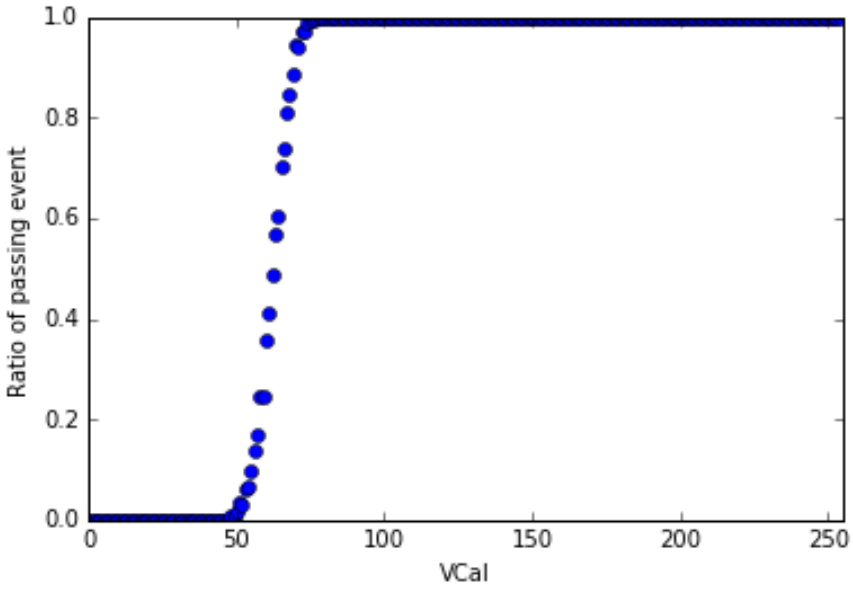

Figure 5.6: S-curve example for one channel of a VFAT2 chip. [8]

Actually, the curve should theoretically look like a step function as an event should always be considered as *passing* once the pulse amplitude (VCal) is above the threshold. However, the noise degrades the shape of the curve. Hence the possibility to extract noise information from this routine.

To this end, the S-curve can be fitted to the error function, shifted on the range [0, 1]: [8]

$$f(x) = \frac{1}{2}(1 + erf(\frac{x-\mu}{\sigma\sqrt{2}}) \tag{5.1}$$

Where x is a gaussian variable of mean μ and standard deviation σ, while the error function $erf(x)$ is in the form of $\frac{1}{\sqrt{\pi}} \int_{-x}^{x} e^{-t^2} \mathrm{d}t$.

To fit the S-curve to the error function illustrated on figure 5.7, two parameters are adjusted: the mean μ, representing the detection level of the S-curve and the standard deviation, representing the noise level on the channel: if σ is large,the slope is big and noise is important while σ is low, the slope is steep and the curve approaches a step function.

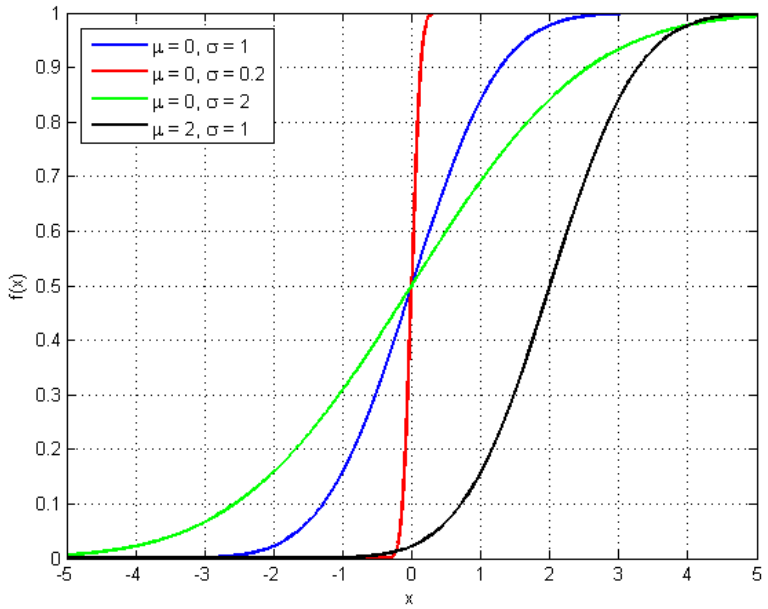

Figure 5.7: Illustration of the error function to fit according to the parameters μ and σ.

5.2.2 VFAT3 S-curves

A plot of the S-curves for every channel of the VFAT3 chips is shown on figure 5.8. The first outcome is that each channel's front-end is working properly. Then, we can highlight the steep slope of each channel as we reach the 100 % within only 3 VCal giving a first positive evaluation of the noise behaviour.

We can now extract the mean and the standard deviation from the fitting of the error function. The mean (figure 5.9) gives a detection level of the channels of $VCal \simeq 26$. While the average standard deviation (figure 5.10) gives $\sigma = 0.57$.

These values can then be converted into Equivalent Noise Charge (ENC) values thanks to a linear fitting of the measured charge corresponding to the value provided by the Digital-to-Analog Converter (DAC) available on the chip. A preliminary straight line of this fitting is plotted on figure 5.11 and the slope provides the conversion factor to get a first approximation of the ENC value of the noise.

Applying to the standard deviation of the S-curves, one gets :

$$ENC = 0.2178 \times \sigma = 0.1459\,\text{fC} \tag{5.2}$$

ENC is also often referred in number of electrons instead of fC simply by dividing the noise value by the electron elementary charge (1.6×10^{-19} C). The latter result is

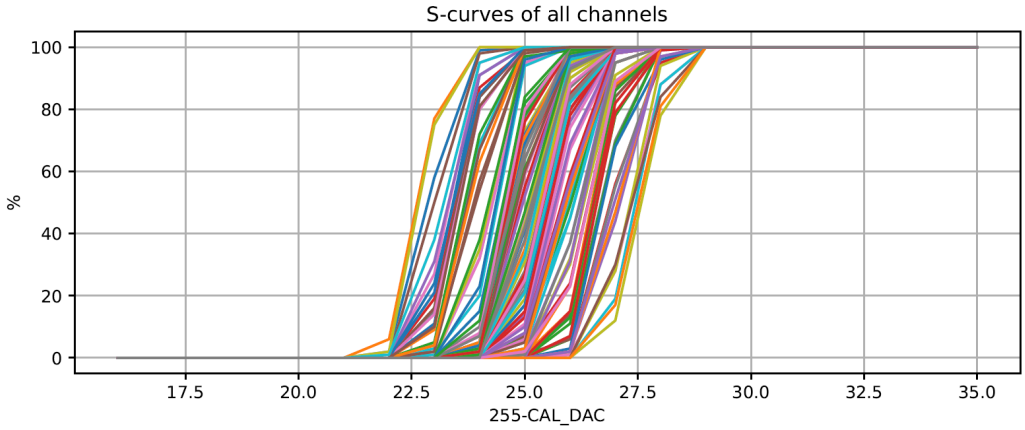

Figure 5.8: S-curves for all VFAT3 channels zoomed in VCal values between 17 and 35 (VCal is defined by an 8-bit registers between 0 and 255).

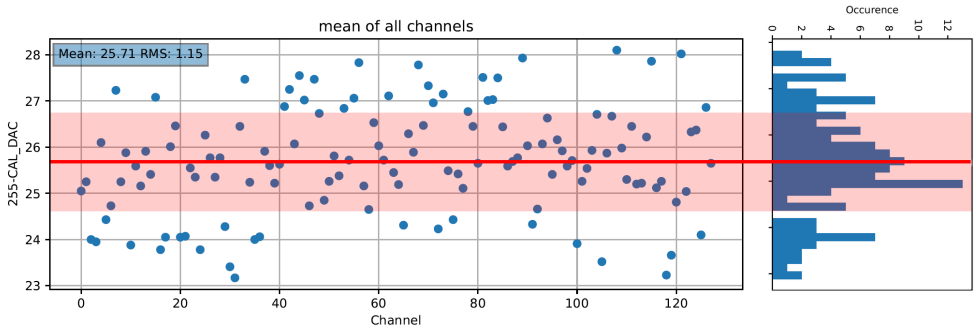

Figure 5.9: VCal mean of the 128 channels of the VFAT3 chip.

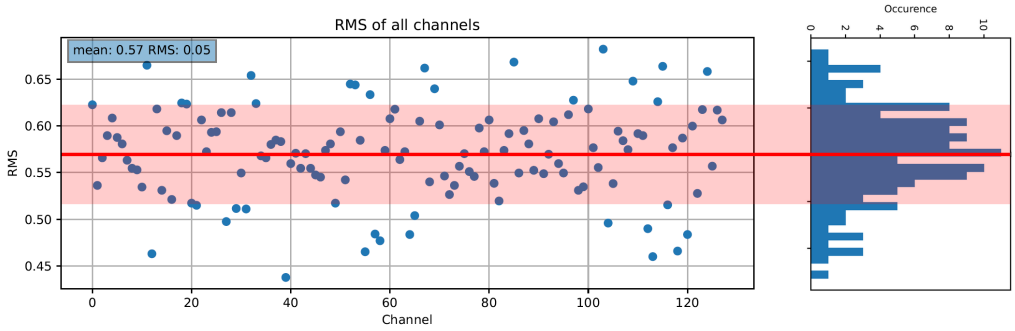

Figure 5.10: Standard deviation of the VCal value around the mean for the 128 channels of the VFAT3 chip.

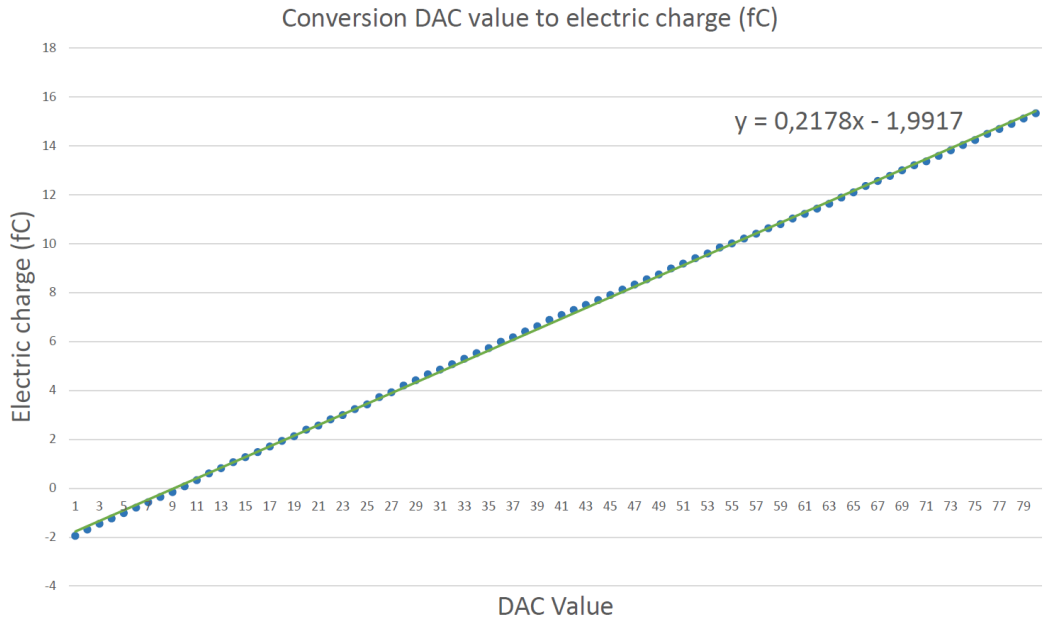

Figure 5.11: Linear fitting (green) of the charge values measured (blue) at the output of the DAC.

compared with the simulated ENC expected in the corresponding case of the chip not being connected to the GEB (that is, a capacitive load of 0 pF) in table 5.1.

	Simulation	**Measurement**
ENC	516 e^-	912 e^-

Table 5.1: ENC results for 0 pF capacitive load compared to simulation with a channel configuration of shaping time = 100 ns and a high gain.

We can see that we are above the expected values. However, as already stated, this conversion factor comes from a first approximation of the linear fitting. Besides, recent results from another set-up using a different configuration has shown noise level of 539 e^-, very close to the expectations and, therefore, approving the noise behaviour of the VFAT3 chip.

Conclusion In this chapter, we have checked the shape of the front-end analog signals, in particular the CFD has shown to be working and more advanced analysis of the time resolution are ongoing. Then the first S-curves have been generated in order to get a first characterization of the noise in the channels of the VFAT3 and, though the calibration is not ideal yet, results are not inconsistent and external results have proved we will be around the simulation target.

Chapter 6

Project management

This chapter is a bit aside from the rest of the core but as this master thesis is part of an important project carried out in CERN, by many institutes (30 in the case of GE1/1), it is therefore necessary to detail which part of the project has been assigned to whom in order to clarify what is my personal contribution. It will also detail what have been the issues encountered and how I managed them throughout the months.

6.1 Work assignment

In chapter 3, the test bench is discussed in terms of hardware, firmware and software. The hardware custom boards have been designed by CERN team while the software and firmware had to be developed from scratch. I attended several workshops occuring between the Particle Physics Department and the BEAMS from ULB, the CERN, Lappeeranta University of Technology (LUT), in Finland and the National Institute for Nuclear Physics (INFN) in Bari, Italy. In these workshops I participated and contributed to defining the architecture of the firmware and the software as they are stated in section 3.2.

Afterwards, software has been developed as part of a PhD thesis in LUT while the firmware has been developed by myself as the interface between the chip and the software.

6.2 Planning

I started to plan the timing of my master thesis very soon using Gantt charts reviewed regularly throughout the year. They are available in appendix C.

Imposing this self-discipline has allowed for several benefits during the project:

- Plan at the very beginning a significant time margin for unforeseen event and to minimize last minute rush. In my case, one month has been taken into account.
- Having a clear view of the critical path in the project. It allows to determine what are the crucial steps of which delays may compromise submitting the work within the deadline.
- Highlight the possibility of working on independent tasks concurrently to reduce the time frame.

6.2.1 Unforeseen events

The content of this thesis does not reflect the unforeseen events which occured during its realisation though it is important to discuss what they are and how they have been managed.

The different versions of the charts in appendix C have put in evidence different unforeseen events delaying the planned work.

Ipbus implementation

Although the Ipbus is developed by the CERN and pieces of firmware and software are available, the implementation of it in the FPGA has not been as trivial as expected. To briefly explain, the firmware available was designed in VHDL using ISE software from Xilinx. However, modelling on Kintex 7 FPGAs has to be done under Vivado. It has therefore been necessary to convert the existing firmware for Vivado by adapting the Xilinx IPs used but also the design constraints.

Once the implementation has been over, there were yet trouble with using Ipbus regularly throughout the firmware development: issues during synthesis, firmware not responding, and so on. This was happening in an erratic fashion and the causes were therefore very complex to find out. This was circumvented by using version controlling and frequently recovering the last working firmware version.

VFAT3 arrival

VFAT3 arrival was clearly a node belonging to the critical path. As explained in section 3.1, the VFAT3 was laying on the translation board (see figure B.6) with many testing points available in order to fully characterize the chip. There were so many tiny pins to route on the board that stringent technology had to be used. Among others, the top layer of the translation board was buried in order to place the chip and having two layers for routing the tracks, by regular routing and mechanical bonding.

These harsh requirements delayed the VFAT3 arrival by several weeks because of problems in production by the manufacturer. Decision has been taken by the CERN

to simplify the translation board by reducing the number of testing points and relax the technology requirements, resulting in the actual translation board presented in this thesis (see figures B.4 and B.5).

The main drawback of this action is that the trigger path cannot be characterized. This will have to be done later with the exhaustive version of the translation board.

Test bench instability

During the characterization of the chip, it turned out that the testing set-up had some instability as it could not run properly over a certain amount of time: at some point, we can witness a drop of the digital current consumed below 20 mA and the VFAT3 were no more sending any data. After investigation, as the problem was only appearing in our test bench in Brussels despite using the same configuration, the firmware and software were dismissed of any suspicion. Finally, by looking at the VFAT3 chip with a microscope, we found out that 3 bondings are a bit bent over and seem to touch themselves. It cannot be proved yet but there is a high probability that a short-circuit is causing this failure.

In default thereof, to run longer routines during characterization, the software was adapted locally to do the tests in smaller chunks.

Despite those unforeseen events, keeping track of the planning periodically allowed me to take care of them and work accordingly to stick to the deadlines.

6.2.2 Risk analysis

The risk of having the VFAT3 arrival delayed was something we were aware of from the very beginning of the thesis as it was part of the critical path and depending on many uncontrolled external factors.

For that reason, a contingency plan was proposed in case the chip could not arrived or be tested in time. This second subject was to study the quality of SLVS signals, as shortly discussed in section 4.4 but for realistic situation, that is, by simulating the actual GEB and the different length of the transmission lines from each VFAT3 until the Opto-hybrid, but also contributing to the commissioning of the triple-GEM detector prototype currently under test in CMS.

However, fortunately, the delays have been well handled and characterization has been carried on as initially planned.

6.3 Learning outcomes

To conclude, I think it is also of particular interest to shortly mention the outcomes I gained from such a particular experience.

Indeed, doing its master thesis as part of a major project such as in CERN is very challenging since it adds to the thesis requirements a whole dimension of project management, teamwork, maturity management, risk factors awareness, and so on.

Those are additional constraints hardly appearing in pure research subjects but they are of special interest and very motivating for an engineer which has to learn dealing with them regarding its career.

Conclusion

As part of the next long shutdown of the LHC, CMS is planned to be upgraded. Among others, the GE1/1 project will implement a new type of detector using triple-GEM technology.

A first detector has been designed and implemented in CMS in early 2017 to act as a proof-of-concept and determine potential unforeseen issues.

The GE1/1 development has proceeded and the VFAT chip gathering the signals from the detector has recently been redesigned as the VFAT3. The aim of this master thesis has therefore been to characterize this chip. It has implied several tasks.

First, a dedicated test bench has been developed for characterizing the chip. To interact with it, implementing a firmware and software interface has also been achieved. Their architecture could not simply be recycled from the VFAT2 system as the communication protocol has changed and the VFAT2 system was optimized for operating in CMS and not for debugging purpose.

Once the test bench and the communication software and firmware have been developed, a series of tests have been carried out on the VFAT3 chip.

Many functionalities have been verified in particular on the digital side: the Communication port and Slow Control run in ideal conditions and the chip can be configured seamlessly while the quality of the signals has been approved. For the front-end part, each stage has shown positive response. Then S-curves have been generated to evaluate noise behaviour of the VFAT3 channels and revealed a noise level in agreement with the one simulated.

Still, some malfunctioning have also been spotted, projecting a second design of the VFAT3 for the next months. However, the Power-On-Reset issue is not critical and the SEL potential issue is clearly not due to the chip design but rather most probably due to the chosen technology. Therefore, it is important to emphasize that, although still preliminary, all the measurements obtained in this thesis show that the VFAT3 chip behaves as expected.

In the future, more advanced tests will be performed on the front-end part in addition to the qualitative characterization presented in this thesis, namely in terms of linearity, gain or stability but also time resolution study of the CFD and radiation testing will be carried out in order to possibly reveal the SRAMs failure.

Appendix A

Additional CMS pictures

Figure A.1: The CMS end-cap and a GEM-detector position highlighted in red. [10]

Figure A.2: Another view of the CMS end-cap and a GEM-detector position highlighted in red.

Figure A.3: The author enjoying

Appendix B

Custom boards for VFAT3 test bench

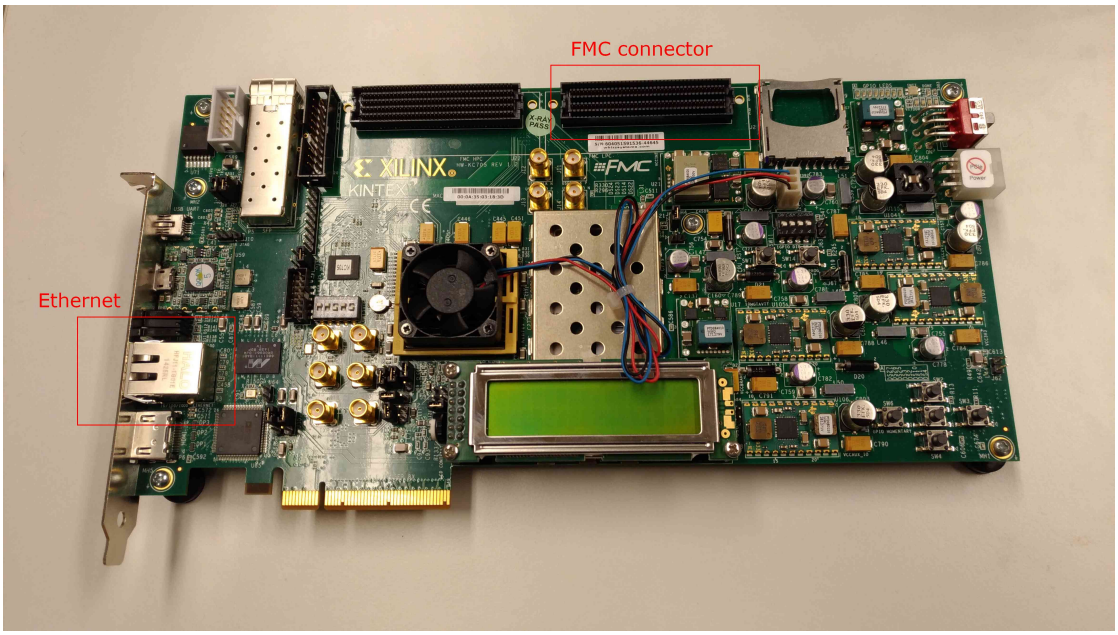

Figure B.1: The Kintex-7 Evaluation Kit from Xilinx holding the FPGA. The FMC connector on the top-right side is used to communicate with the VFAT3 via the Verification board. The ipbus communication with the software is done via the ethernet port on the left side of the board.

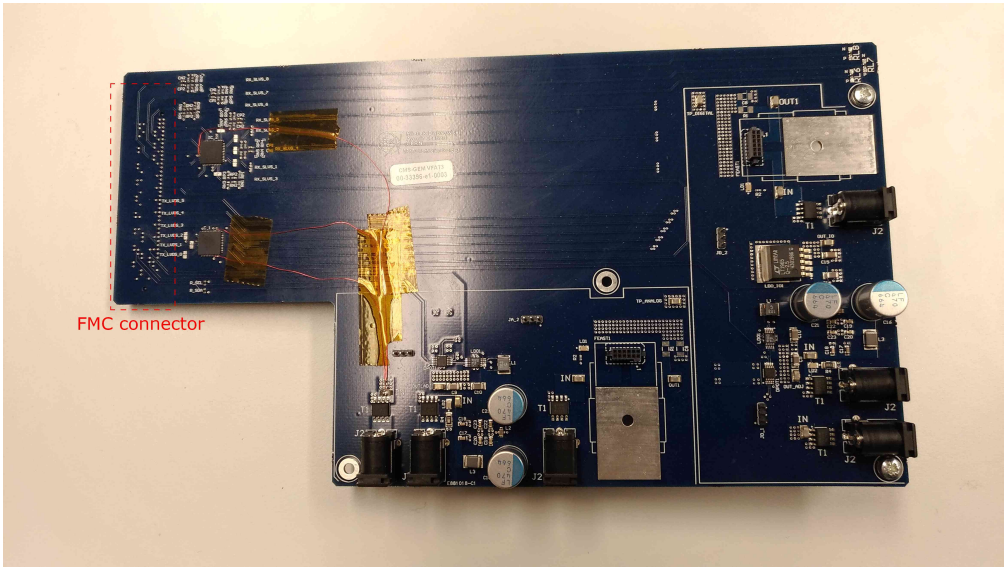

Figure B.2: The Verification board v1 is plugged in on the FMC connector of the Kintex-7 board using the connector on the left, available on the bottom side of the board. It has been used only for developing the firmware by looping the data sent from the FPGA back to it.

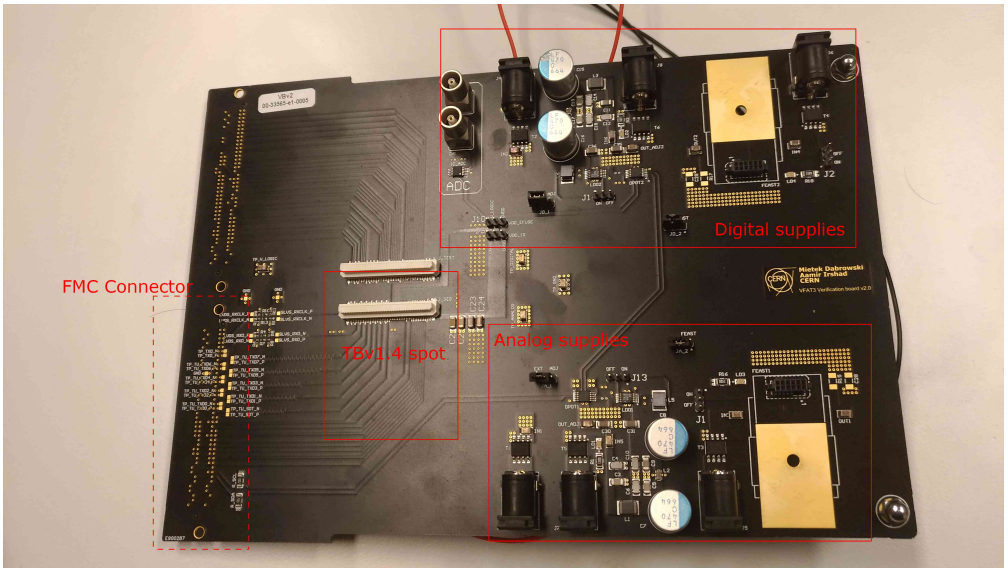

Figure B.3: The Verification board v2 is used to communicate with the VFAT3 chip. The latter is plugged in the corresponding white connector. Different power supply connectors are available to power up the analog and digital part of the VFAT3.

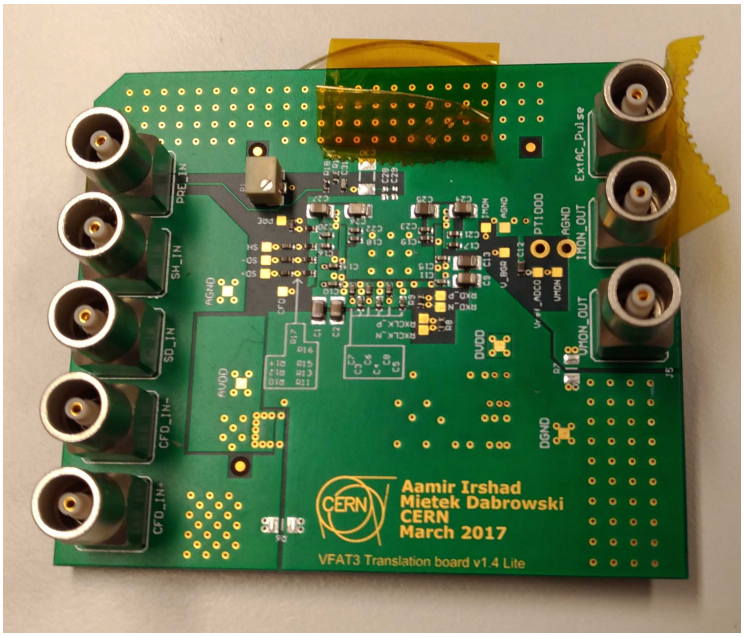

Figure B.4: The translation board v1.4. On its top side, it provides several testing points in order to test and characterize the chip properly.

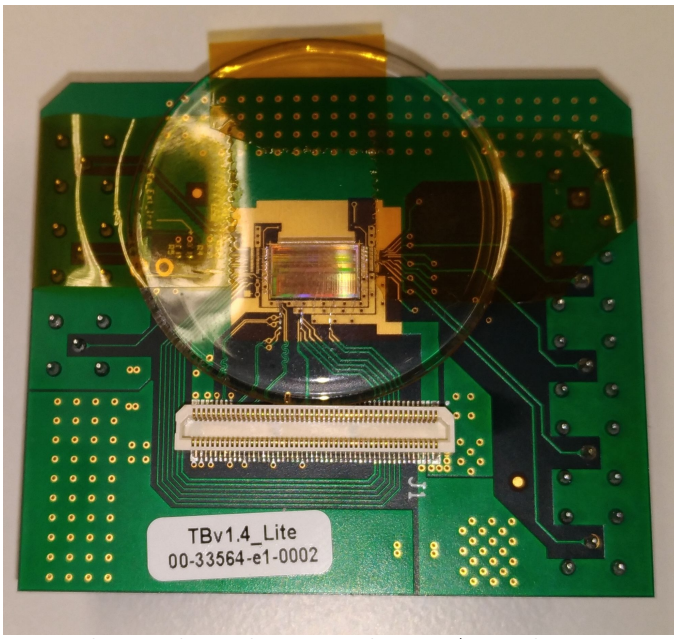

Figure B.5: The translation board v1.4. The VFAT3 chip sits on the bottom side of the board, under a plastic cover to protect the bonding .

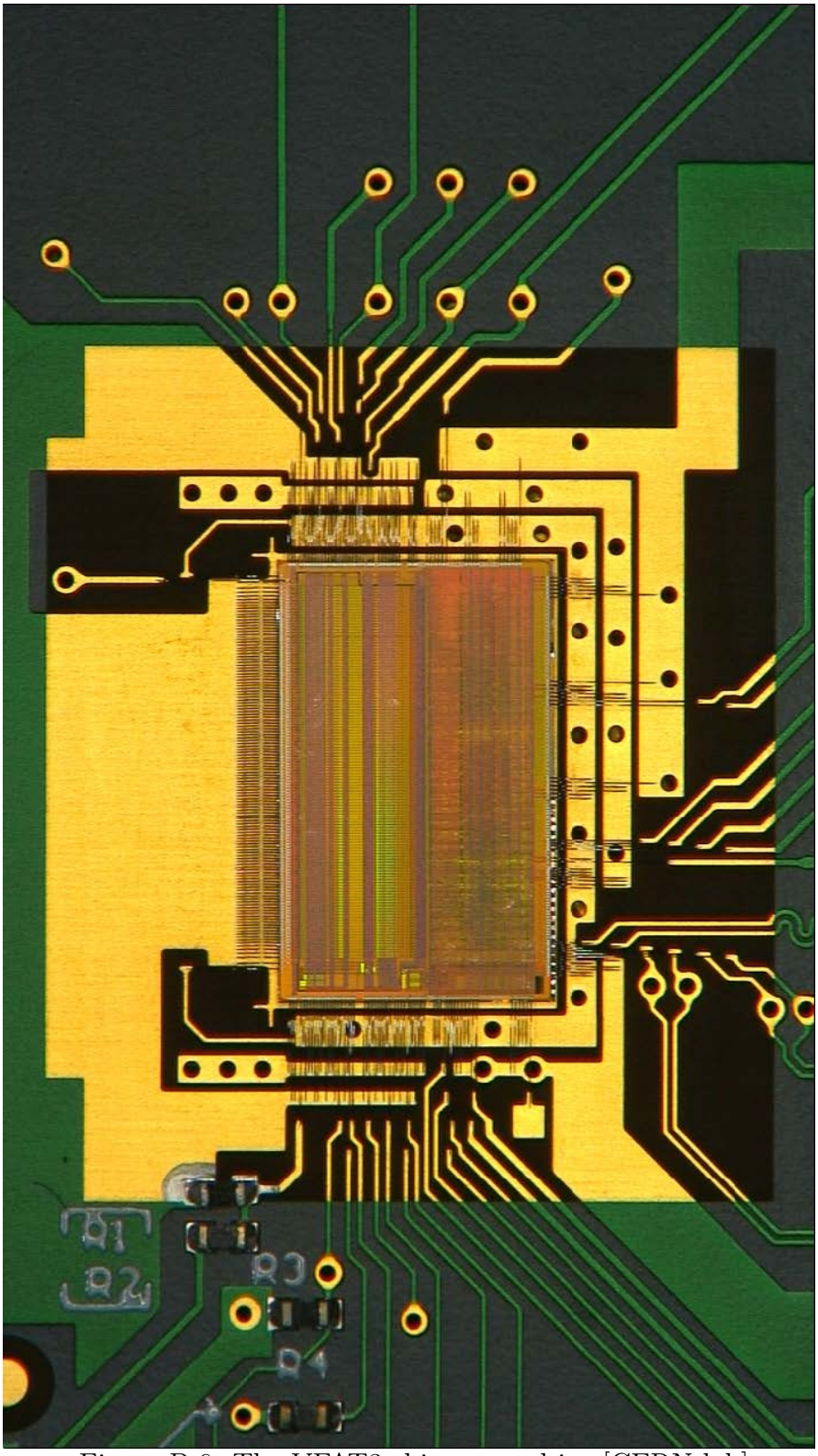

Figure B.6: The VFAT3 chip zoomed in. [CERN lab]

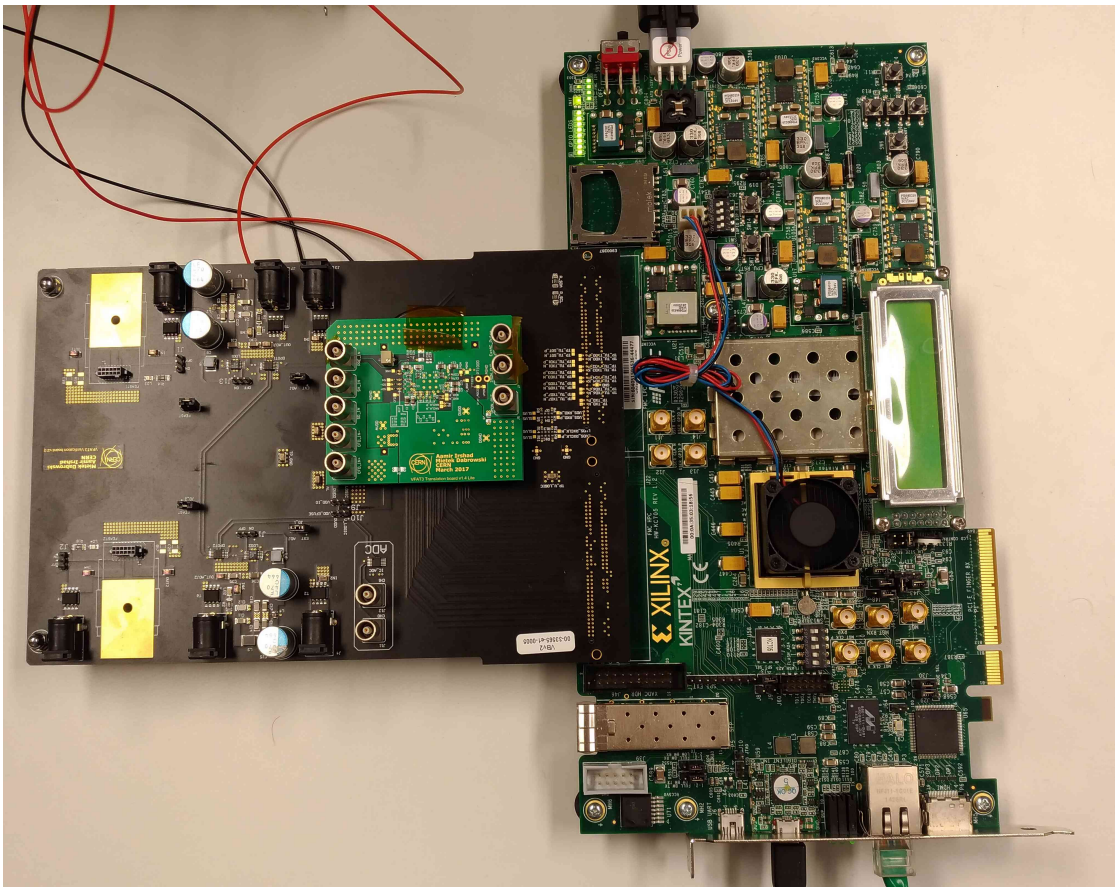

Figure B.7: The full test bench set-up zoomed in.

Appendix C

Gantt diagrams

The aim of this appendix is to highlight the organization during this master thesis and the prevention with respect to the delays expected for the VFAT3 arrival and other unforeseen events. Not every Gantt diagrams have been appended.

For the sake of clarity, the firmware development and the characterization which are the most critical parts are put in evidence.

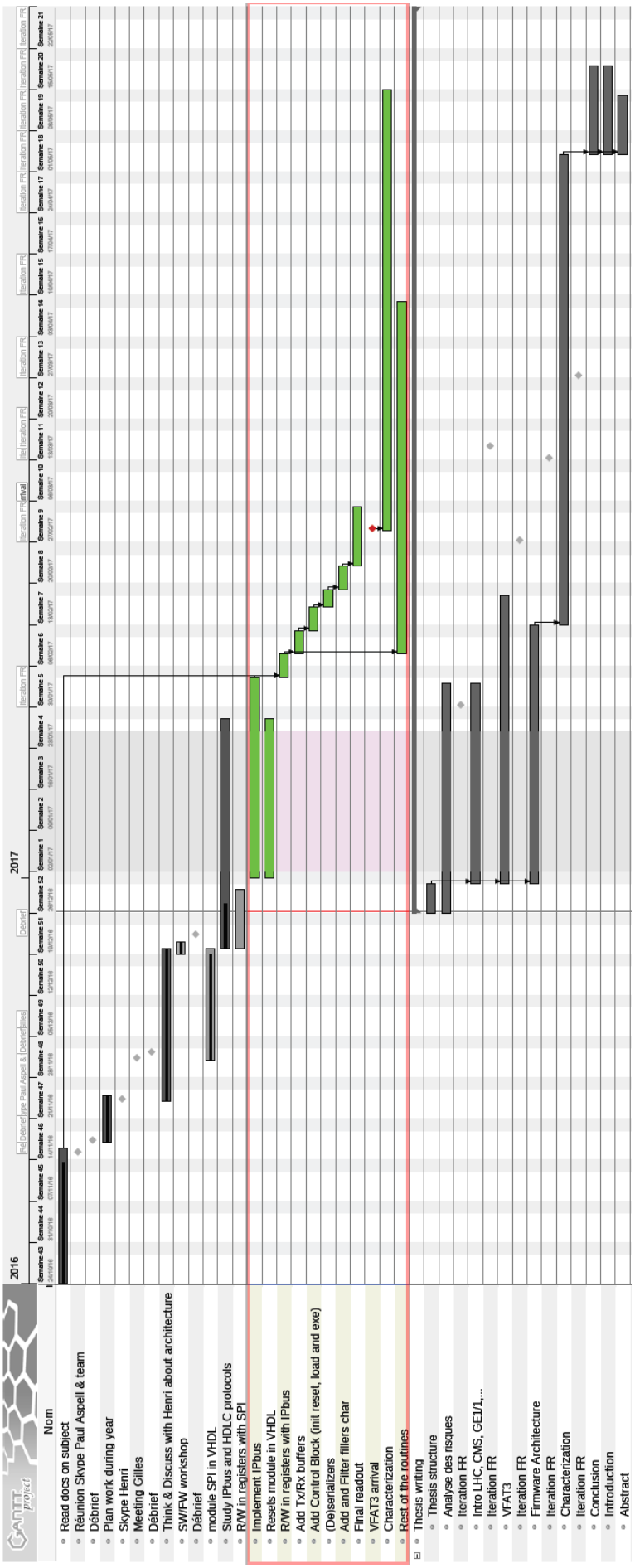

Figure C.1: Gantt diagram version 2. A time margin of one month was preserved for unforeseen events and delays. VFAT3 arrival planned for March 1, 2017

Figure C.2: Gantt diagram version 4. VFAT3 arrival postponed to March 30, 2017

Figure C.3: Gantt diagram version 5. VFAT3 arrival on April 12, 2017

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