ULB Faculté des Sciences

The CMS High Granularity Calorimeter—Front-end Design, Characterization and Implementation

Thesis submitted by Fakhri Alam Khan
in fulfilment of the requirements of the PhD Degree in Sciences (“Doctorat en Sciences”)
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Declaration

I declare that this dissertation is my original research report. It has been written entirely by me and has not been submitted, either wholly or in part, for any other professional qualification or academic award. Where parts of the research are the result of joint efforts, collaborative work has been explicitly acknowledged. The experimental activities described in this dissertation—particularly the design, testing, and analysis of Hexaboard performance and the silicon module laser-based timing studies—have been carried out primarily by myself. All plots related to these studies are original and generated by me.
For the beam test results discussed in the thesis, I have used selected plots from the HGCAL collaboration database, with proper credit and reference.
All literature, data, and technical sources used in the preparation of this thesis have been duly cited and acknowledged in accordance with academic standards.

Acknowledgement

I would like to express my deepest gratitude to my PhD supervisors, Dr. Gilles De Lentdecker and Dr. Paul Aspell, for their unwavering support and mentorship throughout this research journey. Their guidance—both technical and academic—has been instrumental in shaping the direction and execution of this work. I am especially thankful to Dr. Gilles De Lentdecker for his patience and invaluable feedback through numerous iterations of this thesis, which greatly refined its clarity and scientific rigor. I am equally grateful to Dr. Paul Aspell and Dr. David Barney for their foundational role in creating this PhD opportunity and for securing the institutional and financial framework that made this research possible.

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Dedication

To my beloved wife, Ruby—
for her endless love, patience, and unwavering support through every challenge of this journey.

And to my three precious children,
Hashir, Abeera, and Anabia—
whose smiles, laughter, and innocence brought light and strength to even the most difficult days.

This work is as much yours as it is mine.

Abstract

The High Granularity Calorimeter (HGCAL) is a groundbreaking upgrade to the Compact Muon Solenoid (CMS) detector for the High Luminosity Large Hadron Collider (HL-LHC). It is designed to operate under extreme conditions of high radiation, particle flux, and unprecedented pileup densities. This thesis presents the comprehensive development, optimisation, and validation of the front-end readout electronics for HGCAL, with a primary focus on the Hexaboards, which are complex multilayer printed circuit boards that serve as the readout board for the silicon sensor modules.

The research undertaken in this work encompasses the full design cycle of the Low-Density (LD) and High-Density (HD) Hexaboards, from conceptualization to iterative prototyping, performance optimisation, and system validation. A systematic approach incorporating front-end electronics simulations and experimental testing enabled significant improvements in electronic stability, signal integrity, and noise suppression. Through successive iterations, the electronics noise was reduced from approximately 40 ADC units to 1.5 ADC units ($\sim$1900 electrons for a 47 pF detector capacitance), a reduction of more than 10-fold—while the signal-to-noise ratio (S/N) improved by a factor of 10. Consequently, the performance met the stringent requirements outlined in the HGCAL Technical Design Report (TDR). Beam tests conducted at CERN's Super Proton Synchrotron (SPS) validated the performance of the silicon Hex-Module and, by extension, confirmed that the Hexaboard design meets stringent specifications. The results demonstrate exceptional reliability and precise charge and timing resolution.

In parallel, this thesis explores the timing performance of HGCAL's silicon modules through the development of a laser-based test system, enabling precise charge injection and high-resolution time-of-arrival (TOA) measurements. The timing studies, incorporating variations in temperature, electronic jitter, and time-walk effects, informed key calibrations necessary for optimising event reconstruction in the high-luminosity regime. Integration of these timing parameters into HGCAL physics simulations further assessed their impact on neutral hadron and photon reconstruction efficiency, ensuring robust pileup mitigation strategies.

This work establishes a validated, high-performance readout system for HGCAL, ensuring its readiness for large-scale production and integration into CMS. The methodologies and optimisations developed herein will support high-precision calorimetry and data integrity in the HL-LHC era, reinforcing the CMS detector's capability for advanced physics analyses in the forthcoming decade.

The thesis is structured as follows: Chapter 1 introduces the LHC and HL-LHC, outlining the CMS experiment and the limitations of its current detector. It establishes the need for an upgraded endcap calorimeter for Phase II operations, presenting the HGCAL as the optimal solution for HL-LHC conditions. Chapter 2 motivates the HGCAL upgrade and follows a top-down approach to justify its design. It defines the calorimeter structure, explains the necessity of high granularity, and outlines key technologi-

cal choices addressing performance requirements. The chapter systematically answers the many 'whys' behind HGCAL's implementation and concludes with its impact on CMS physics. Chapter 3 focuses on the readout electronics, detailing the HGCROC ASIC as the front-end chip responsible for charge measurement, timing precision, and data processing. Chapter 4 explores the challenges in silicon readout Hexaboard design, and defines a design strategy for addressing these challenges. It concludes with an analysis of different Hexaboard variants and their on-cassette powering and control schemes. Chapter 5 validates Hexaboard designs across multiple iterations. Performance is assessed through noise studies, pedestal stability, and a comparative analysis of intrinsic and coherent noise, establishing the final optimized design for stable HGCAL operation. Chapter 6, the final chapter, evaluates silicon module performance using beam tests and laser-based characterization, assessing its response to MIP signals and timing resolution. The results confirm overall detector performance, ensuring compliance with HL-LHC requirements.

This thesis comprehensively documents the development, optimization, and validation of the CMS HGCAL readout system, providing a foundation for its deployment in the HL-LHC era.

List of abbreviations

HL – LHC	High-Luminosity Large Hadron Collider
LHC	Large Hadron Collider
HGCAL	High Granularity Calorimeter
CMS	Compact Muon Solenoid
ATLAS	A Toroidal LHC Apparatus
LHCb	Large Hadron Collider beauty
ALICE	A Large Ion Collider Experiment
PSB	Proton Synchrotron Booster
PS	Proton Synchrotron
LS	Long Shutdown
NbTi	Niobium-Titanium
Nb3Sn	Niobium-tin
SM	Standard Model
BSM	Beyond Standard Model
QCD	Quantum Chromodynamics
CSC	Cathode Strip Chamber
RPC	Resistive Plate Chamber
GEM	Gas Electron Multiplier
BRIL	Beam Radiation Instrumentation and Luminosity
FBCM	Fast Beam Condition Monitor
DT	Drift Tube
HB	Hexaboard
MIP	Minimum ionization particle
LD	Low Density
HD	High Density
IT	Inner Tracker
OT	Outer Tracker
APD	Avalanche photodiode
VPT	Vacuum phototriode
HPD	hybrid photodiodes
L1Trigger	Level1 Trigger
HLT	High-Level Trigger
BTL	Barrel Timing Layer
ETL	EndCap Timing Layer
LGADs	Low-Gain Avalanche Detectors
TDR	Technical Design Report
$PbWO_4$	Lead tungstate
GMTube	Geiger–Müller Tube
TOT	Time over Threshold
PLL	Phase Locked Loop
DLL	Delay Locked Loop
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
CRRC	Capacitor-Resistor-Resistor-Capacitor
ADC	Analog to Digital Converter
SARADC	Successive Approximation Register ADC

DAC	Digital to Analog converter
T_p	Peaking Time
$SINAD$	Signal-to-Noise and Distortion Ratio
$ENOB$	Effective Number of Bits
FoM	Figure of Merit
$TDCs$	Time to Digital Converters
$CDCs$	Coarse Time to Digital Converters
$FDCs$	Fine Time to Digital Converters
LSB	Least Significant Bit
MSB	Most Significant Bit
LDO	Low Dropout Voltage
PCB	Printed Circuit Board
$ASICs$	application-specific chips
MAC	Module Assembly Center
BGA	Ball Grid Array
TOA	Time of Arrival
$LD-NSH-HB-V2$	Low Density Non-Stepped Hole Hexaboard-Version 2
NSH	Non-Stepped Hole
PTH	Plated-Through Hole
Lx	Layer x of Hexaboard
$USCB$	The University of California, Santa Barbara
PDN	Power Distribution Network
BT	Beam Test
SPS	Super Proton Synchrotron
SOL	start of life
EOL	End of life
NIM	Nuclear Instrument Module
$FWHM$	Full Width at Half Maximum
$IRLaser$	Infrared Laser

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Chapter 1

Introduction to CMS Phase-II Upgrades

1.1 Introduction

This chapter provides a comprehensive overview of the Compact Muon Solenoid (CMS) Phase-II upgrades, which are essential for adapting the detector systems to the challenging operational conditions of the High-Luminosity Large Hadron Collider (HL-LHC). The HL-LHC is designed to deliver unprecedented levels of luminosity, resulting in higher collision rates, increased particle interactions (pileup), and elevated radiation levels. These advancements and challenges, while promising for exploring new physics, impose significant demands on the CMS detector. To maintain its performance and ensure precision in physics analyses, extensive upgrades across its subsystems are planned. The chapter begins with an introduction to the Large Hadron Collider (LHC), including its operation, design, and key parameters that form the foundation of its physics goals (Section 1.2). The subsequent sections delve into the physics motivation behind the LHC, particularly focusing on the exploration of the Standard Model (SM), the discovery of the Higgs boson (Section 1.3). The discussion then transitions to the HL-LHC project, outlining the motivation for its upgrades, the anticipated challenges, and the enhancements to its capabilities (Section 1.4). This section highlights the increased luminosity and pileup levels that necessitate a new phase of detector upgrades. A detailed description of the CMS detector and its subsystems is presented in Section 1.5. This includes a breakdown of its key components, such as the tracker, calorimeters, superconducting solenoid, and muon system, which work in unison to identify and measure particles resulting from collisions. Special attention is given to the calorimeter system, as it plays a central role in detecting photons, electrons, and jets. An overview of the forecasted challenges for Phase-II operations, along with the corresponding planned upgrades to the CMS sub-detectors, is presented in sections 1.6 and 1.7 respectively. These upgrades aim to improve the detector's precision, radiation resilience, and capacity to manage high pileup conditions, ensuring that the CMS experiment continues to lead advancements in high-energy physics research. Finally, the chapter concludes by discussing the challenges posed by the HL-LHC to the CMS endcap calorimeter systems in Section 1.8, with an emphasis on the effects of radiation damage, high pileup, and increased data rates. These challenges significantly impact the performance of the calorimeter system, particularly in the endcap regions, necessitating its replacement with the HGCAL. By providing a structured overview of the LHC, CMS detector, and the challenges of Phase II, this chapter sets the stage for understanding the role of the HGCAL and its contributions to future physics analyses at the HL-LHC.

1.2 Introduction to LHC

The Large Hadron Collider (LHC), the world's most powerful particle accelerator, is located at the European Organisation for Nuclear Research (CERN). It explores the fundamental components of matter and their interactions by colliding high-energy proton pairs. Designed with a center-of-mass energy of $\sqrt{s} = 14\,\text{TeV}$ and an instantaneous luminosity of $L = 10^{34}\,\text{cm}^{-2}\,\text{s}^{-1}$, the LHC enables the study of phenomena under conditions akin to those prevailing approximately 10^{-12} seconds after the Big Bang. These high-energy collisions generate energy densities comparable to those during this early phase of the universe's evolution. The LHC also conducts specialized experiments using heavy-ion collisions, facilitating deeper insights into the quark-gluon plasma state of matter. More details about the LHC's engineering and physics can be found in the technical design reports [31–34].

The primary objective of the LHC was to confirm the existence of the Higgs boson and its scope extends far beyond this. The LHC's ongoing mission is to characterize the Higgs boson in unprecedented detail, study its rare processes, and uncover potential deviations from Standard Model (SM) predictions. Additionally, the LHC explores phenomena that the SM cannot fully explain, such as the nature of dark matter, the matter-antimatter asymmetry in the universe, and the possibility of extra dimensions [35].

The LHC is a ring collider with a circumference of $\sim 27\,\text{km}$, comprising eight straight sections and eight arcs. Located approximately 100 m underground, it occupies the tunnel previously used by its predecessor, the Large Electron-Positron Collider (LEP) [36]. The CERN accelerator complex, including all beamline stages, is illustrated in figure 1.1. To maintain the quality of the beams by minimizing interactions between proton beams and residual gas molecules, the LHC maintains an ultrahigh vacuum of approximately $10^{-13}\,\text{bar}$ within its beam pipes.

The beams are guided by 1,232 superconducting dipole magnets, each 15 m long, which generate intense magnetic fields of up to 8.3 T. These fields are produced by electric currents of 11.8 kA passing through superconducting coils made of Niobium-Titanium (NbTi), which are maintained at a cryogenic temperature of 1.9 K. In addition, 392 quadrupole magnets focus the particle beams, ensuring they remain focused as they traverse the accelerator. Constrained by the tunnel's 3.7 m width, engineers devised an innovative twin-bore magnet scheme, integrating two sets of coils and beam pipes into a single structure. This design maximizes space utilization and enhances operational efficiency, exemplifying the LHC's innovative approach to scientific discovery [37, 38].

Operation

Proton acceleration at the LHC begins with compressed hydrogen stored in a small container. Hydrogen atoms are injected into LINAC-2, a linear accelerator, where a high electric field ionizes the atoms, removing electrons to produce proton packets. These protons, initially traveling at one-third the speed of light, advance through a series of increasingly sophisticated acceleration stages.

The Proton Synchrotron Booster (PSB) is the first stop, dividing proton packets into bunches distributed across four rings for initial acceleration. Subsequently, the protons enter the Proton Synchrotron (PS), a 628 m circular accelerator where they reach speeds exceeding 99.9% of the speed of light and gain up to 25 GeV of energy. These accelerated protons are transferred to the Super Proton Synchrotron (SPS) [39], a ring of approximately 7 km in circumference, where their energy is further increased to 450 GeV. From the SPS, protons are injected into the LHC's twin vacuum rings, circulating in opposite directions. At collision points, synchronized proton beams collide with a combined energy of 14 TeV (TeV), twice the energy of the individual beams.

The acceleration process is highly efficient, taking approximately 30 min to prepare and inject 2808 proton bunches into the LHC. Proton bunches are spaced 7.5 m apart, corresponding to a time interval of 25 ns between bunches, allowing for the maximum number of bunches per beam. Superconducting magnets, powered by currents of 12 kA, guide and confine the beams in their high-speed orbits. Acceleration

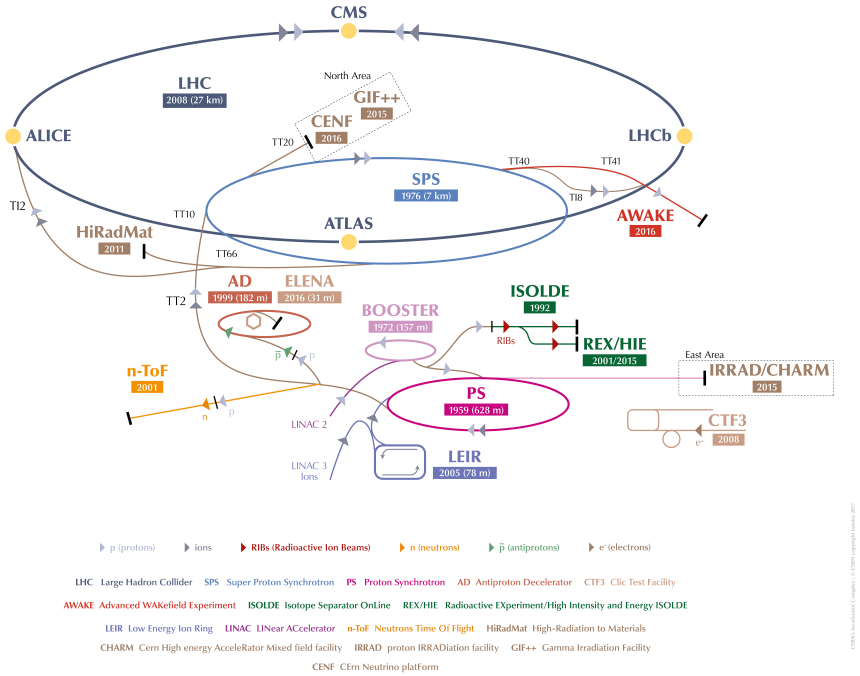


Figure 1.1: CERN Accelerator Complex, adapted from [1].

is achieved through eight radio-frequency cavities per beam, operating at a frequency of 40.079 MHz, with each cavity imparting an additional 2 MeV of kinetic energy to individual protons.

Maintaining beam stability and focus along the LHC's 27 km circumference relies on a complex system of superconducting magnets. Dipole magnets provide beam steering, while quadrupole magnets ensure transverse focusing. To counteract longitudinal momentum spread, specialized magnets such as sextupole, octupole, and decapole magnets are strategically placed along the beamline.

Following full acceleration, proton beams are directed to collide at four designated interaction points, each equipped with a specialized detector system. Two of them, ATLAS (A Toroidal LHC Apparatus) [40] and CMS (Compact Muon Solenoid) [11], serve as general-purpose experiments, capable of observing a wide range of particle interactions. The remaining two detectors are more specialized: LHC b (Large Hadron Collider beauty) [41], focuses on the properties and decays of particles containing bottom quarks, contributing to the understanding of matter-antimatter asymmetry. ALICE (A Large Ion Collider Experiment) [42], is dedicated to studying heavy-ion collisions and exploring the quark-gluon plasma (QGP), a state of matter prevalent in the early universe.

Important beam parameters

Instantaneous luminosity: The instantaneous luminosity L determines the event rate per unit time, $\frac{dN}{dt}$, for a process with a given cross section σ, is expressed as:

$$\frac{dN}{dt} = L\sigma. \tag{1.1}$$

where σ is the cross section, which indicates the area of an incoming particle available for collision and hence shows its collision probability and is measured in unit of area "barn" ($= 10^{-24}\,\text{cm}^2$). The instantaneous luminosity is measured in $\text{cm}^{-2}\text{s}^{-1}$. Its design value for LHC is $L = 10^{34}\ \text{cm}^{-2}\text{s}^{-1}$.
Instegral luminosity: The integrated luminosity L_{int} representing the total data recorded over a specific period, typically a year, and is expressed as:

$$L_{\text{int}} = \int L dt, \tag{1.2}$$

where L is the instantaneous luminosity. The integrated luminosity is commonly measured in inverse femtobarns (fb^{-1}) or inverse picobarns (pb^{-1}), and it serves as a key parameter for evaluating the performance of a particle collider and the amount of data collected for physics analyses.
Figure 1.2 presents the cumulative integrated luminosity recorded by the CMS experiment from 2010 to 2024 at various center-of-mass energies. The plot emphasizes the annual progress in data collection, showcasing significant contributions from the distinct operational phases of the LHC, known as Runs.

The operational timeline of the LHC is divided into periods called *Runs*, during which the machine operates continuously to collect data. The first operational phase, **Run 1 (2010–2012)**, marked the initial operation of the LHC, achieving center-of-mass energies of up to 8 TeV. This was followed by **Long Shutdown 1 (LS1, 2013–2014)**, during which significant maintenance and upgrades were conducted. **Run 2 (2015–2018)** introduced an increased center-of-mass energy of 13 TeV and substantial improvements in beam intensity and stability, resulting in a marked rise in integrated luminosity. Following **Long Shutdown 2 (LS2, 2019–2021)**, **Run 3** commenced in 2022, further enhancing LHC performance with accelerator and detector upgrades that enabled higher collision rates and improved data collection efficiency at a center-of-mass energy of 13.6 TeV. The next phase, **Long Shutdown 3 (LS3)**, scheduled to begin in June 2026, will see the implementation of the **Phase-II upgrade**. This upgrade is essential for the transition to the High Luminosity LHC (HL-LHC), aiming to significantly enhance luminosity and improve detector performance to meet the challenges of high-radiation and high-pileup environments.

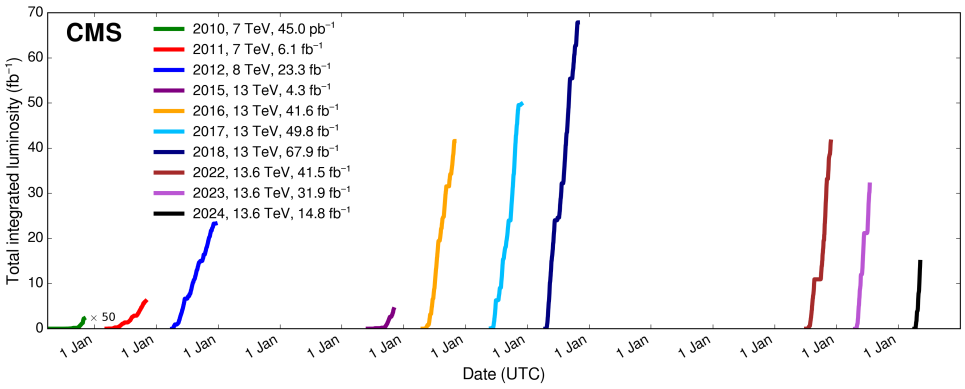


Figure 1.2: Cumulative integrated luminosity recorded by the CMS experiment from 2010 to 2024 at different center-of-mass energies. The plot highlights yearly progress in luminosity, with milestones achieved in key data-taking periods, adapted from [2].

The instantaneous luminosity can be calculated from the beam parameters as follows:

$$L = \frac{N_p n_b f_{rev} \gamma_r}{4\pi \varepsilon_n \beta^*} F, \tag{1.3}$$

where N_p is the number of particles per bunch, n_b is the number of bunches, f_{rev} is the revolution frequency, γ_r is the relativistic gamma factor, ε_n represents the beam emittance, β^* is the beta parameter related to the magnet focusing power at the interaction point, and F accounts for the reduction in luminosity due to the beams' crossing angle θ_c and the transverse and longitudinal RMS bunch sizes (σ_{xy} and σ_z) and given by:

$$F = \sqrt{1 + \left(\frac{\theta_c \sigma_z}{2\sigma_{xy}}\right)^2}. \tag{1.4}$$

The detailed derivation and explanation of the Luminosity can be found in reference [43]. A summary of all operating parameters of LHC can be found in the table 1.1

Parameter	Meaning	Nominal value
$\sqrt{s}$	Center-of-mass energy	14 TeV
Δt	Bunch separation	25 ns
n_b	Number of bunches	2808
N_p	Number of protons per bunches	$1.15 \cdot 10^{11}$
f_{rev}	Revolution frequency	11245 Hz
σ_z	Transverse bunch r.m.s. at the IP	16.7 μm
σ_{xy}	Longitudinal bunch r.m.s.	7.55 cm
$\beta^\star$	Beta function at the IP	0.55 m
θ_c	Crossing angle at the IP	285 μrad
ε_n	Transverse emmittance	3.75 μm

Table 1.1: Nominal parameters of the LHC in proton-proton collisions.

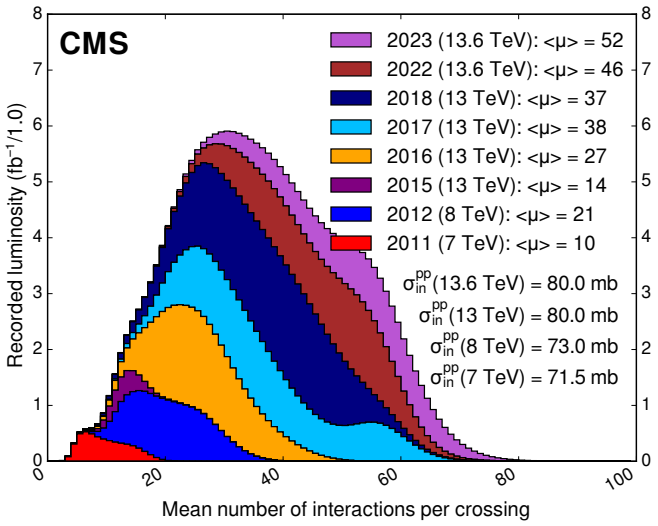


Figure 1.3: Pileup distribution at CMS from 2010 to 2023, showing the increase in average pileup rates ($\langle PU \rangle$) with rising luminosity and center-of-mass energies. The maximum pileup of 52 interactions per bunch crossing was observed during Run 3 at 13.6 TeV, adapted from [2].

Pileup: The average number of interactions per bunch crossing, referred to as pileup, is a critical param-

eter for LHC experiments and is given by the formula:

$$\langle PU \rangle = \frac{L\sigma_{\text{inel}}}{n_b f_{\text{rev}}}, \tag{1.5}$$

where L is the instantaneous luminosity, σ_{inel} is the inelastic proton-proton (pp) cross-section, n_b is the number of bunches, and f_{rev} is the revolution frequency. The LHC was designed for a pileup rate of 22 interactions per bunch crossing under nominal conditions. However, as shown in figure 1.3, upgrades to the accelerator and beam, including increased proton bunch intensity and luminosity, have raised the pileup rate. During Run 3, it averaged 52 interactions per bunch crossing, due to operational advancements that enhanced luminosity and data collection capabilities, though these changes also introduced challenges in managing increased background noise and event reconstruction.

1.3 The Standard Model

The Standard Model (SM) of particle physics is a theoretical framework that explains the fundamental particles and their interactions, excluding gravity. This model is akin to the periodic table for chemistry in that it categorises and describes the basic constituents of matter. Over a century of scientific inquiry led to the identification and discovery of all particles predicted by the SM. The electron was the first to be discovered by J.J. Thomson in 1897 [44], and the most recent, the Higgs boson, was observed in 2012 at CERN by the ATLAS and CMS collaborations [45, 46].

The content of SM is outlined in figure 1.4. The SM categorises elementary particles based on their spin, a type of intrinsic angular momentum. Particles are divided into two groups:

Fermions: Fermions, which have half-integer spin, make up matter and antimatter. These particles includes:

- Six quarks: up, down, charm, strange, top, bottom.
- Six leptons: electron (e), muon (μ), tau (τ), and their corresponding neutrinos: electron-neutrino, muon-neutrino, and tau-neutrino.

These fermions have three generations, with each successive generation being more massive but similar in behaviour to the first, which includes the up and down quarks and the electron and electron-neutrino that are fundamental to the composition of everyday matter.

Bosons: Bosons have integer spin and are responsible for mediating forces between particles:

- The photon mediates the electromagnetic force.
- The gluon carries the strong force.
- The W and Z bosons are mediater for the weak force.

At high energies, the electromagnetic and weak forces merge into a single electroweak force, demonstrating the unification of these interactions under certain conditions. The detail of SM is given in reference [47].

1.3.1 The Higgs Boson at the LHC

On July 4, 2012, the CMS and ATLAS Collaborations announced the discovery of a new boson with spin-0 and a mass of approximately 125 GeV [45, 46], now known as the Higgs boson. This particle, predicted in 1964 [48], resolved a crucial question in the SM of particle physics: how fundamental particles acquire mass. The discovery, based on proton-proton collision data from LHC Run 1 (2011–2012), confirmed

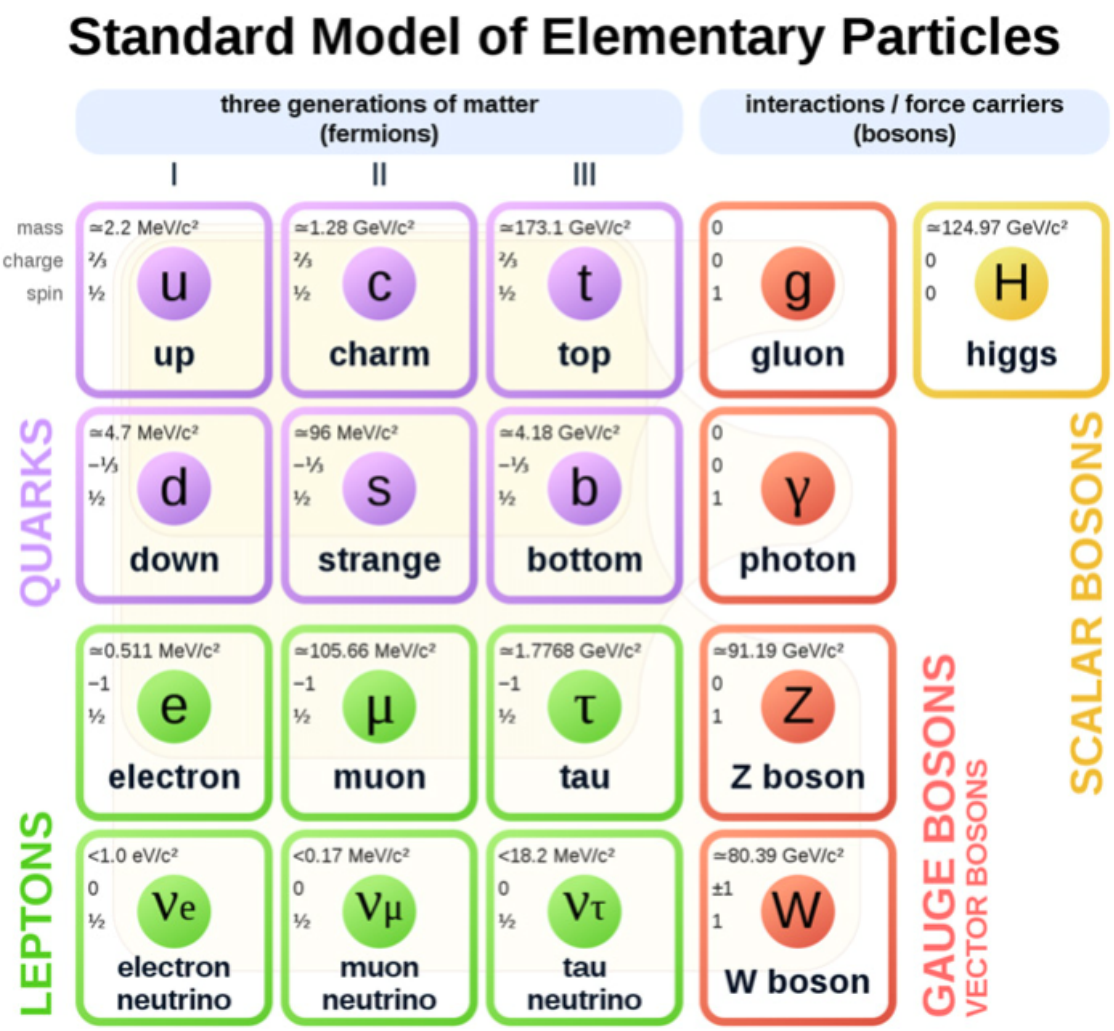


Figure 1.4: Standard Model of particle Physics, image taken from [3]

the existence of this scalar boson. The invariant mass distributions reconstructed in CMS detector for the $H \to \gamma\gamma$ and $H \to ZZ^* \to 4\ell$ decay channels are shown in figure 1.5. These two channels, known as golden channels, mainly used for higg discovery by both CMS and ATLAS and are senstive due to their excellent mass resolution and low background contamination.

Higgs Boson Production Mechanisms: The Higgs boson can be produced through several mechanisms, illustrated in figure 1.6. Gluon-gluon fusion (ggH) is the dominant production mode across all center-of-mass energies ($\sqrt{s}$). Vector boson fusion (VBF), involving the exchange of W or Z bosons between quarks, is distinguished by two high-energy jets widely separated in pseudorapidity. This geometry makes the CMS endcap calorimeters vital for detecting such jets, enabling effective event reconstruction. Other processes include associated production with vector bosons (VH), top quarks (ttH), and bottom quarks (bbH), which, while less common, are significant for targeted studies.

Decay Modes: The Higgs boson decays into various SM particles, with branching ratios dependent on the decay channel, as summarized in Table 1.2. While $H \to b\bar{b}$ has the highest branching ratio (58.2%), its use is hindered by significant background noise from Quantum Chromodynamics (QCD) processes.

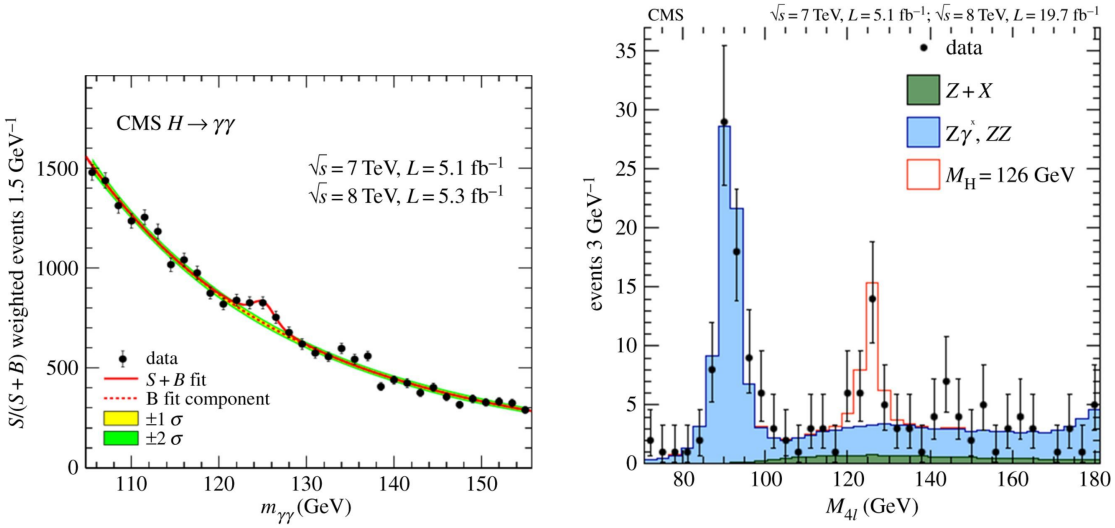


Figure 1.5: (Left) Diphoton invariant mass distribution ($m_{\gamma\gamma}$) for $H \to \gamma\gamma$ events recorded by CMS at $\sqrt{s} = 7\,\text{TeV}$ and $8\,\text{TeV}$, weighted by the signal-to-background ratio. The expected signal and background components are overlaid. (Right) Four-lepton invariant mass distribution ($M_{4\ell}$) for $H \to ZZ^* \to 4\ell$ candidates, showing a distinct peak at $125\,\text{GeV}$. Background contributions include irreducible ZZ and reducible processes such as $Z\gamma^*$ and $Z+X$, adapted from [4].

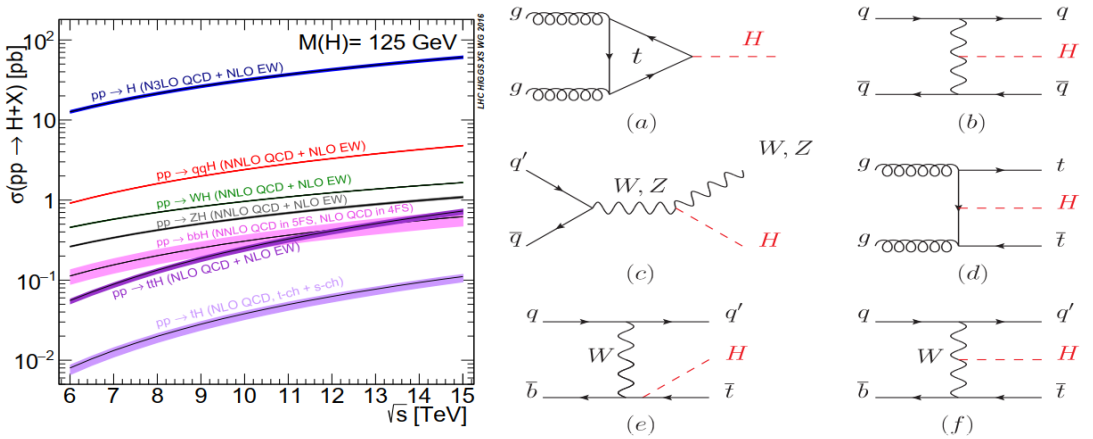


Figure 1.6: (Left) Higgs boson production cross sections as a function of the center-of-mass energy $\sqrt{s}$, illustrating the dominance of gluon-gluon fusion (ggH) across the energy range. (Right) Feynman diagrams corresponding to the primary Higgs boson production mechanisms: (a) gluon-gluon fusion (ggH) (b) vector boson fusion (VBF), (c) associated production with a vector boson (VH), (d) associated production with a top-quark pair (ttH), (e) single top-associated production (tH), and (f) production in association with bottom quarks (bbH), adopted from [5].

In contrast, the $H \to \gamma\gamma$ and $H \to ZZ^* \to 4\ell$ channels, despite their lower branching ratios, are crucial for Higgs boson studies due to their superior mass resolution, making them the primary 'golden channels' in

the discovery and analysis of the Higgs boson.

The constituents of these golden decays, photons and leptons are detected with high precision using the electromagnetic calorimeter (ECAL). The endcap ECAL, in particular, is vital for capturing high-energy photons and electrons, especially those originating from decays in the forward region. Furthermore, the reconstruction of jets in the vector boson fusion (*VBF*) process, characterized by widely separated jets in pseudorapidity, relies heavily on the combined performance of the endcap ECAL and hadronic calorimeter (HCAL). These features underscore the critical role of the endcap calorimeters in Higgs boson physics, enabling detailed analyses of its production and decay mechanisms.

Poor Mass Resolution Channels		**Good Mass Resolution Channels**	
Decay Mode	BR (%)	Decay Mode	BR (%)
$H \to b\bar{b}$	58.2	$H \to ZZ^*$	2.6
$H \to WW^*$	21.4	$H \to \gamma\gamma$	0.23
$H \to gg$	8.2	$H \to Z\gamma$	0.15
$H \to \tau^+\tau^-$	6.3	$H \to \mu^+\mu^-$	0.02

Table 1.2: Summary of Higgs boson decay modes (branching fractions and resolutions) for a 125 GeV mass in the SM, adopted from [49].

The discovery of the Higgs boson marked a historic achievement in physics, confirming the mechanism through which particles acquire mass within the SM. However, this discovery is not the conclusion but rather the beginning of a deeper exploration into the properties of this fundamental particle. To precisely characterize the Higgs boson's couplings, study its rare production and decay processes, and search for possible deviations from SM predictions, a significantly larger dataset and more robust detection systems are required. To achieve the required statistical precision and broaden the discovery potential for physics beyond the Standard Model (BSM), the LHC will undergo a major upgrade to enter its next operational phase: the High-Luminosity LHC (HL-LHC).

1.4 Introduction to HL-LHC

Despite the remarkable achievements of the LHC, numerous intriguing questions still linger, including the enigma of dark matter and the perplexing disparity between matter and antimatter. In order to tackle these inquiries, CERN has decided to expand the LHC's physics program by implementing substantial upgrades, which will result in the creation of the High-Luminosity LHC (HL-LHC) project. The HL-LHC will operate after the current LHC **Run3** with the goal of increasing the luminosity of the collider by a factor of 10 beyond the design value, to collect an integrated luminosity of up to 3000 fb^{-1} over about ten years of operation. This substantial increase in luminosity will allow physicists to collect more data, provides more statistics that will lead to more precise measurements and a greater potential to observe rare processes that are beyond the reach of the current LHC [50].

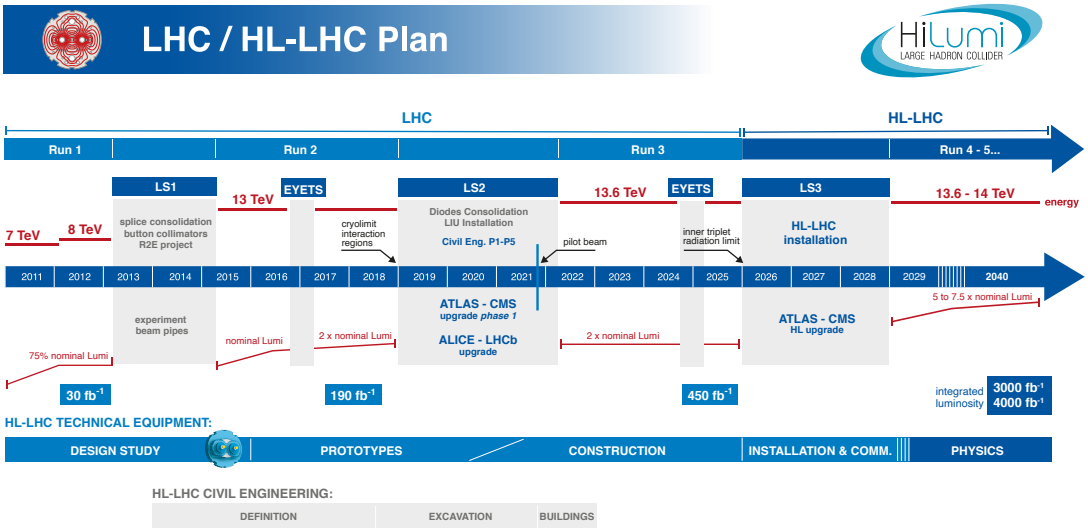


Figure 1.7: Timeline of LHC and HL-LHC Plans. This timeline highlights key phases and milestones from Run 1 to HL-LHC operations, including energy levels, luminosity achievements, and major upgrades during Long Shutdowns (LS1, LS2, LS3). The phases of design, prototyping, construction, installation, and physics operation are also shown [6].

The timeline of the HL-LHC upgrades and operational parameters is depicted in figure 1.7. The current LHC operation is set to conclude at the end of Run 3, achieving an integrated luminosity of 450fb^{-1}. The installation of the HL-LHC upgrades will take place during LS3. At the HL-LHC, a nominal instantaneous luminosity of $L = 5 \cdot 10^{34}$ cm^{-2} s^{-1} is anticipated, corresponding to five times the LHC design value. With 160 days of physics operation per year and a physics efficiency of 50%, it is possible to collect 250fb^{-1} of integrated luminosity annually, reaching a total of 3000fb^{-1} by 2040. An overview of LHC parameters across different phase is give in table 1.3 [49]. More details about the HL-LHC operation and updates can be find out in references [49–51].

Motivation for HL-LHC Upgrades: The HL-LHC project has the goal of boosting the LHC's capabilities by greatly increasing its luminosity, which is a measure of the number of collisions occurring per second. With increased luminosity, scientists will have the opportunity to gather a greater amount of data, resulting in enhanced measurement accuracy and a higher likelihood of uncovering rare phenomena and

Parameter	Design	Run-1	Run-2	Run-3	HL-LHC
Energy [TeV]	14	7/8	13	14	14
Bunch spacing [ns]	25	50	25	25	25
Bunch Intensity $[10^{11}\text{ppb}]$	1.15	1.6	1.2	up to 1.8	2.2
Number of bunches	2800	1400	2500	2800	2800
Emittance [μm]	3.5	2.2	2.2	2.5	2.5
Crossing angle [μrad]	285	-	$300 \rightarrow 260$	$300 \rightarrow 260$	TBD
Peak luminosity $[10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}]$	1.0	0.8	2.0	2.0	5.0
Integrated luminosity $[\text{fb}^{-1}]$	40	30	160	300	3000
Peak pileup	25	45	60	55	150

Table 1.3: Overview of key accelerator parameters for the LHC, including the design specifications and values utilized during Run-1 and Run-2, as well as the projected parameters for Run-3 and the HL-LHC shown in [49].

particles. This will achieved through a concentrated effort to study the Higgs boson in great detail and to delve into physics that goes BSM. This entails the exploration of novel particles or interactions that may shed light on unexplained phenomena, including dark matter and the matter-antimatter asymmetry. The project also involves the integration of cutting-edge technologies such as state-of-the-art superconducting magnets, highly accurate timing detectors, and enhanced tracking and calorimetric systems capable of managing increased collision rates and radiation levels. Notable improvements to the ATLAS and CMS detectors, such as upgraded calorimeters and timing detectors, are set to enhance performance in the demanding conditions of the HL-LHC [14, 49, 50].

HL-LHC challenges: The High luminosity presents a number of notable challenges:

1. **Pile-up**: With higher luminosities, there is a significant increase in the number of interactions per bunch-crossing, going from the current range of 20-40 to approximately 140-200. Isolating and analyzing individual events becomes quite challenging in this scenario. State-of-the-art data processing algorithms and cutting-edge detector technologies are essential to handle this level of complexity and guarantee precise event reconstruction.

2. **Harsh radiation environment**: The higher frequency of collisions leads to a more intense radiation environment. Over time, the performance of detectors and other critical components may be negatively affected by higher radiation levels. As a result, it is necessary to enhance the durability and dependability of the LHC's detectors by developing radiation-tolerant materials and designs.

Upgrades for the LHC: In order to accomplish the objectives of the HL-LHC, there are several significant upgrades that are being planned for the LHC itself [50], are given below:

1. Installation of new niobium-tin superconducting quadrupole magnets: The β^* parameter at the interaction points (IPs) will undergo a significant reduction in order to enhance luminosity. To achieve this reduction, the installation of new, wide-aperture inner triplet magnets is necessary. These magnets will use niobium-tin (Nb3Sn) superconductors, which offer higher magnetic fields and improved radiation resistance compared to the previously employed niobium-titanium (NbTi)

magnets. It is important to have a higher field strength in order to achieve tighter beam focusing at the collision points.

2. Crab cavities: Compact superconducting cavities, also referred to as 'crab cavities,' are utilized to rotate the proton bunches prior to collision. This modification decreases the crossing angle of the beams, resulting in a larger overlap area and improved luminosity [52, 53].

3. Injectors upgrades: Significant upgrades underwent for the injector systems during LS2, with the aim of delivering high-intensity beams to the LHC. These upgrades targeted all stages of the injector complex—from Linac4 through the PS Booster, Proton Synchrotron (PS), and Super Proton Synchrotron (SPS). The objective was to deliver beams with enhanced brightness and higher bunch intensities, while preserving transverse emittance, thereby enabling the LHC to operate at significantly elevated luminosity levels [54].

Improvements to the Experiments: Significant upgrades are being made to the experiments for the HL-LHC operation, specifically the ATLAS and CMS detectors, in order to effectively handle the increased luminosity and radiation levels. The required upgrade for CMS will be discussed in section 1.7.

1.5 Compact Muon Solenoid Detector (CMS) Detector

The Compact Muon Solenoid (CMS) is a general-purpose detector at the LHC, situated approximately 100 meters underground in Cessy, France, near Geneva. The CMS experiment investigates proton-proton and Pb-Pb collisions at center-of-mass energies of 14 TeV (pp) and 5.5 TeV (Pb-Pb), with respective luminosity levels reaching $10^{34}\text{cm}^{-2}\text{s}^{-1}$ and $10^{27}\text{cm}^{-2}\text{s}^{-1}$. These energy scales enable precision studies of SM physics, particularly the properties of the Higgs boson, and allow the search for new physics phenomena.

The detector is designed to reconstruct and measure all stable particles emerging from high-energy interactions. These include hadrons (protons, neutrons, kaons, pions), leptons (electrons, muons and taus), and photons, while neutrinos are inferred indirectly through missing transverse energy (MET) calculations. Precise measurements of momentum, energy, charge, and vertex position are essential for distinguishing between signals originating from the primary interaction vertex and those arising from pile-up events.

The CMS detector adopts a layered, onion-like geometry, optimized to provide hermetic coverage with an almost 4π solid angle acceptance. Its cylindrical structure, with a 15-meter diameter and a 21.5-meter length, is one of the most compact yet dense detectors in the LHC experiments, weighing approximately 12,500 tonnes. A detailed illustration of the CMS detector and its key subsystems is presented in figure 1.8.

At its core, CMS houses a superconducting solenoid, generating a 3.8 T magnetic field, one of the strongest ever deployed in a collider experiment. This field enables the precise curvature of charged particle trajectories, allowing momentum determination with high accuracy. The field is contained within a 12,500-tonne steel return yoke, which also serves as the structural framework and integrates the muon detection system.

Encircling the beamline, the tracking system consists of silicon pixel and microstrip detectors, which provide fine-grained spatial resolution for vertex reconstruction and momentum measurements. Beyond the tracker, the electromagnetic calorimeter (ECAL), composed of lead tungstate ($PbWO_4$) crystals, facilitates high-resolution energy measurements of electrons and photons. The hadronic calorimeter (HCAL), constructed using brass and plastic scintillators, ensures efficient containment of hadronic showers and contributes to jet energy measurements and MET calculations. The muon system, embedded within the return yoke, incorporates drift tubes, cathode strip chambers, and resistive plate chambers, forming a

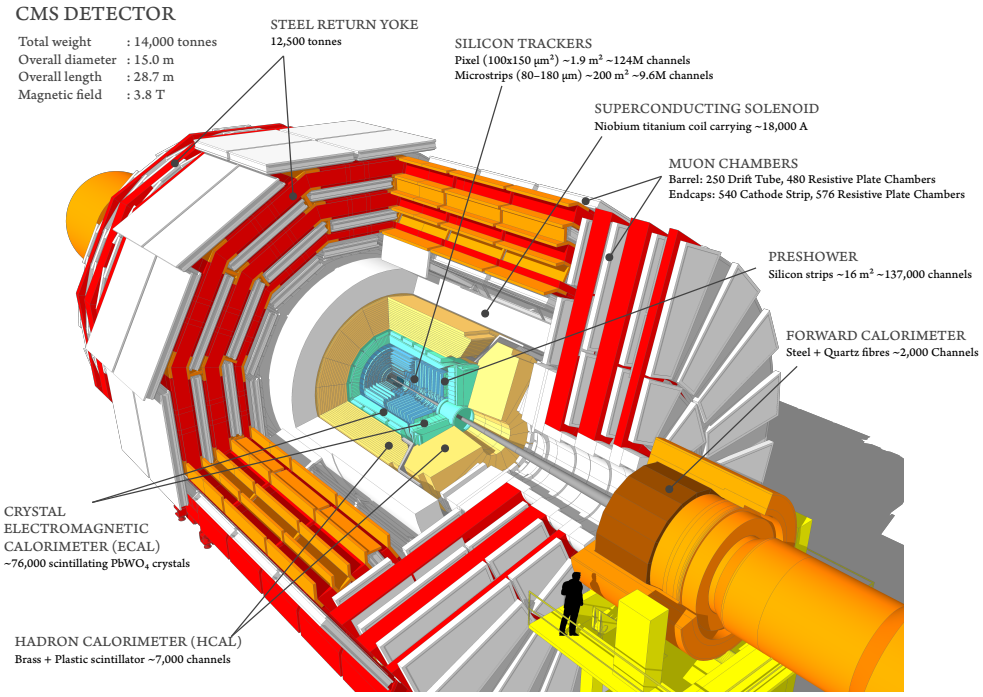


Figure 1.8: An overview of the CMS detector and its subsystems [7].

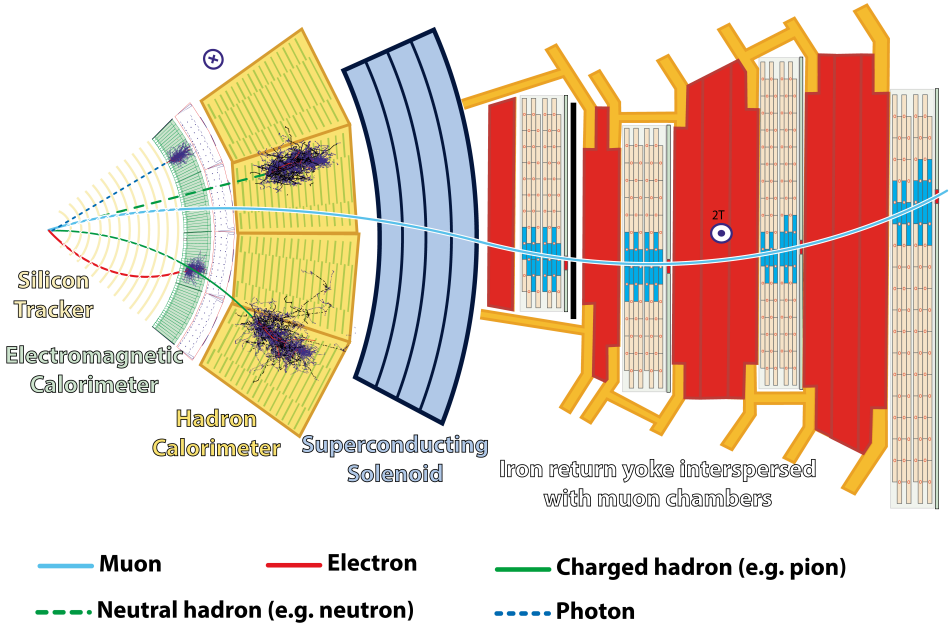


Figure 1.9: CMS slice view [8].

multi-layered detection scheme that ensures robust muon identification, a crucial feature in many physics analyses, including Higgs boson decays and beyond-SM searches.

A functional overview of the CMS detector can be understood through its cross-sectional representation, shown in figure 1.9. This schematic illustrates how different particles interact with various sub-detectors as they traverse the CMS detector. Charged particles, such as electrons and charged hadrons, first pass through the silicon tracking system, where their trajectories are measured. The bending of these tracks under the influence of the magnetic field enables precise momentum reconstruction. Electrons and photons then deposit their energy in the ECAL, while hadrons primarily interact within the HCAL. Neutral particles, such as neutrons, are detected through their interactions in the HCAL. Muons, on the other hand, penetrate all detector layers, leaving signals in the muon chambers located within the return yoke. This layered approach allows CMS to achieve a comprehensive reconstruction of high-energy collision events, ensuring precise measurements of all fundamental particle signaturess [11].

The subsequent subsections present a brief discussion about the CMS coordinate system, followed by an overview of the major sub-detector system, highlighting their design, operational principles, and contributions to high-energy physics analyses.

1.5.1 Coordinate system

Figure 1.10 depicts the coordinate system utilized by the CMS and ATLAS detectors. It is a right-handed coordinate system, where the origin is at the interaction points (IP), the x-axis is directed towards the LHC ring center, the y-axis is in an upward direction, and the z-axis is along the beam line. Given the detector's cylindrical structure, a polar coordinate system is also used. The azimuthal angle ϕ is defined as the angle in the transverse (x-y) plane relative to the z-axis, while r presenting the radial coordinate. The detector's segmentation in the r-z plane is determined by the concept of rapidity. Rapidity is a measure of a particle's energy and momentum along the beam axis, represented by E and p_z respectively.

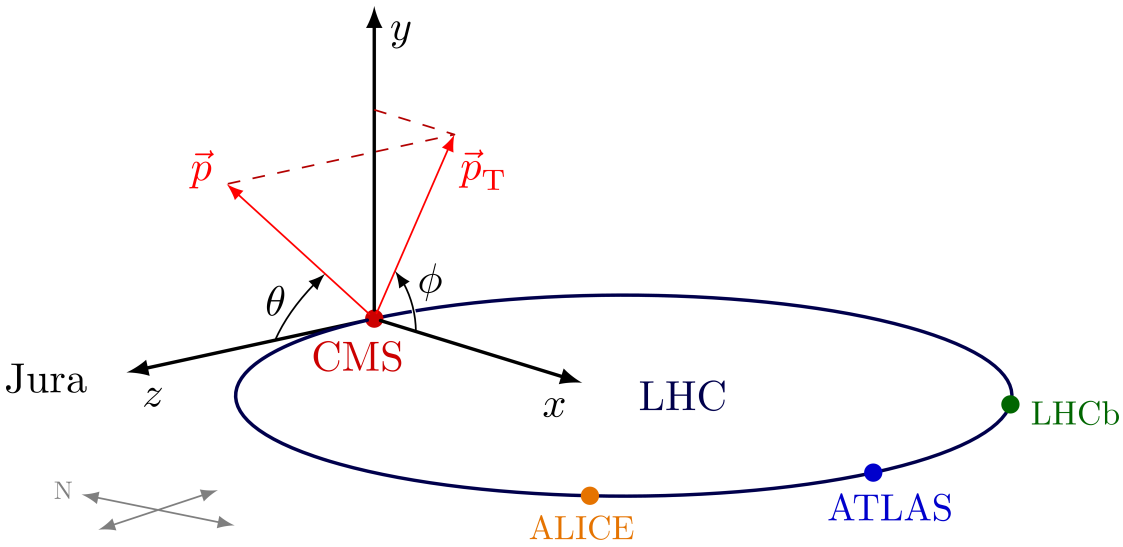


Figure 1.10: Diagram illustrating the CMS coordinate systems [9].

$$Y = 0.5 \ln\left(\frac{E + p_z}{E - p_z}\right). \tag{1.6}$$

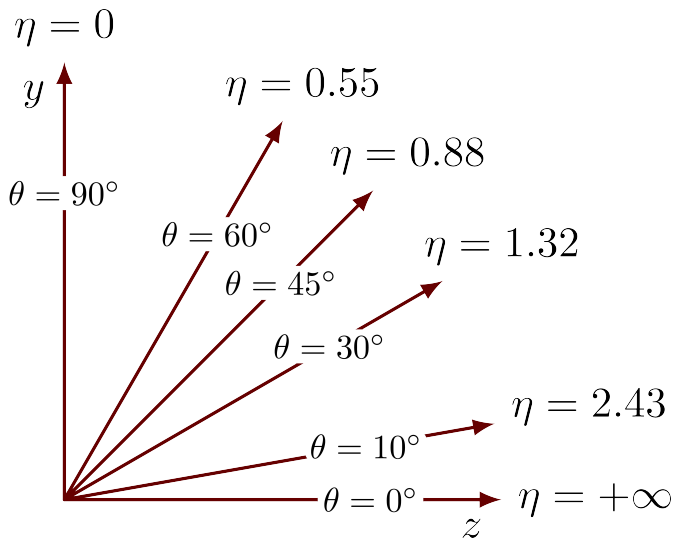


Figure 1.11: Diagram illustrating the relationship between pseudorapidity (η) and the polar angle (θ) for various values of θ [9].

The rapidity for ultra-relativistic ($m/E \ll 1$) particles simplifies to pseudo rapidity and is given as:

$$\eta = \frac{1}{2}\ln\left(\frac{p+p_z}{p-p_z}\right) = -\ln\tan\left(\frac{\theta}{2}\right). \tag{1.7}$$

The η values vary from 0 at $\theta = \frac{\pi}{2}$ to $\pm\infty$ at $\theta = 0(\pi)$, as shown in figure 1.11. The spatial separation between two particles is expressed, in a Lorentz boost-invariant frame, as a function of their angular distance as:

$$\Delta R = \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2}.$$

where θ represents the polar angle in relation to the beam axis [50].

1.5.2 CMS Subdetector Systems

The CMS detector is composed of multiple subsystems, each designed for specific detection and measurement functions, as illustrated in figure 1.8. A cross-sectional view highlighting the arrangement of these sub-detectors is presented in figure 1.9. The detailed description of these sub-detector systems is provided below:

The CMS Tracker

The CMS Tracker subsystem [55, 56] is a high-precision silicon-based detection system designed to reconstruct the trajectories of charged particles within the CMS experiment. As these particles traverse the Tracker, they ionize the silicon, generating electron-hole pairs that drift under an applied electric field. The resulting signals are collected by finely segmented readout electronics, allowing precise momentum and vertex reconstruction even in dense collision environments.

The Tracker consists of two primary components: the innermost Pixel Detector and the outer Silicon Strip Tracker, forming a highly granular system, as illustrated in figure 1.12. The Pixel Detector, containing approximately 100 million silicon pixels, is positioned closest to the beamline and provides

an exceptional spatial resolution of approximately 10 µm, enabling precise vertex determination important for separating interaction points. Beyond this, the Silicon Strip Tracker extends radially outward, covering a larger volume with nearly 10 million silicon microstrips, enhancing tracking coverage and momentum resolution.

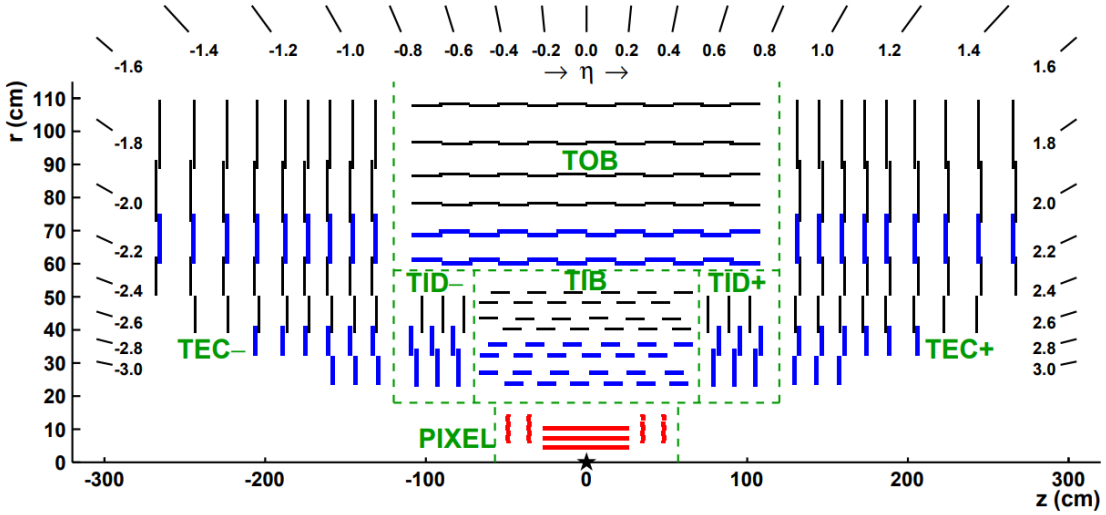


Figure 1.12: A schematic cross-section of the CMS Tracker in the *r*-*z* plane, illustrating its various subsystems, including the Pixel Detector, Tracker Inner Barrel (TIB), Tracker Inner Disks (TID), Tracker Outer Barrel (TOB), and Tracker Endcaps (TEC), adapted from [10].

As shown in figure 1.12, the Pixel Detector is located near the beamline, followed by multiple layers of strip detectors arranged in concentric cylindrical shells and disk-shaped structures. The Silicon Strip Tracker is further divided into distinct subsystems: the Tracker Inner Barrel (TIB), which provides precise tracking in the central region; the Tracker Inner Disks (TID), ensuring coverage in the transition between barrel and endcap regions; the Tracker Outer Barrel (TOB), responsible for tracking at larger radii; and the Tracker Endcaps (TEC), which extend tracking capabilities into the forward regions. These layers ensure robust tracking across a pseudorapidity range of $|\eta| < 2.5$.

This combination of high granularity, low material budget, and precision tracking makes the CMS Tracker a critical component for studying complex collision events, enabling both precision Standard Model measurements and searches for new physics at the LHC.

The CMS Electromagnetic and Hadronic Calorimeters

This thesis focuses on the High Granularity Calorimeter, HGCAL, which will replace the existing endcap calorimeters. Therefore, a detailed discussion of the current CMS calorimeter systems is presented here.

The CMS experiment employs electromagnetic and hadronic calorimeters with a broad pseudorapidity coverage range of $-5 < \eta < 5$. These calorimeters are essential for the identification and reconstruction of photons and electrons and play a pivotal role in measuring jets and missing transverse energy (E_T^{miss}) at the HL-LHC.

Efficient identification of photons and electrons with high resolution is essential for detecting Higgs boson decays into final states involving photons and leptons, such as di-photon ($H \to \gamma\gamma$) or four-lepton ($H \to ZZ^* \to 4\ell$) decay channels. Additionally, accurate separation of electrons from hadrons and the use of particle-flow techniques for jet and E_T^{miss} measurements rely heavily on combined information from

the tracker and calorimeters.

The CMS calorimeter system consists of two main components: the Electromagnetic Calorimeter (ECAL) and the Hadronic Calorimeter (HCAL). These calorimeters utilize specialized technologies and distinct configurations in their respective regions.

Electromagnetic Calorimeter (ECAL): The ECAL [11,57] is a homogeneous and hermetic calorimeter designed to measure the energy of electrons and photons with high precision. It is constructed from $PbWO_4$ scintillating crystals, as shown in figure 1.13. The crystals' high density ($8.28\,g/cm^3$), short radiation length ($X_0 = 0.89\,cm$), and small Molière radius ($R_m = 2.2\,cm$) enable the design of a compact calorimeter with fine granularity [58]. Upon interaction with particles, these crystals emit blue-green scintillation light peaking at 420 nm to 430 nm, which is detected by photodetectors, as illustrated in figure 1.14.

The ECAL's energy resolution for single particles is parameterized as:

$$\left(\frac{\sigma}{E}\right)^2 = \left(\frac{2.8\%}{\sqrt{E}}\right)^2 + \left(\frac{0.12}{E}\right)^2 + (0.30\%)^2. \tag{1.8}$$

where E is in GeV. Initial evaluations using beam tests and subsequent LHC collisions demonstrated a Z-mass resolution of approximately 2% in the barrel and 2%-5% in the endcap regions [59]. The ECAL have two parts, Electromagnetic Barrel (EB) and Elecromagnetic Endcap (EE):

The ECAL Barrel (EB): The EB consists of 61,200 $PbWO_4$ crystals arranged in a cylindrical shape around the LHC beam axis. Each crystal measures 23 cm in length and has a front face of $2.2\,cm \times 2.2\,cm$. It covers $|\eta| < 1.48$ [59]. Avalanche photodiodes (APDs), selected for their high sensitivity and performance in the CMS magnetic field, detect the scintillation light [60].

The ECAL Endcaps (EE): The EE extends the coverage to $|\eta| < 3.0$ and consists of 7,324 $PbWO_4$ crystals per endcap. Each crystal measures 22 cm in length and has a cross-section of $2.6\,cm \times 2.6\,cm$. Vacuum phototriodes (VPTs) are employed in the endcaps for their radiation resilience near the beamline [61].

Pre-shower (ES): The pre-shower detector, installed in front of the EE, identifies neutral pions (π^0) in the endcap fiducial region ($1.653 < |\eta| < 2.6$). It also enhances the distinction between electrons and minimum ionizing particles (MIPs) and improves the position determination of photons and electrons. The pre-shower consists of two active silicon strip sensor planes [11].

Hadronic Calorimeter (HCAL): The HCAL [11, 62, 63] is a segmented calorimeter responsible for measuring the energy of hadrons, including protons and neutrons. It employs layers of dense absorber material (brass) interspersed with plastic scintillator tiles. The energy resolution for hadron-induced showers in the HE region is given by:

$$\left(\frac{\sigma_{h,HE}}{\mu_{h,HE}}\right)^2 = \left(\frac{106.1\%}{\sqrt{E/GeV}}\right)^2 + (4.0\%)^2. \tag{1.9}$$

where E is in GeV [63].

A cross-sectional representation of the HCAL is depicted in figure 1.15, illustrating the distinct subcomponents of the CMS HCAL system. The mian sub-parts of HCAL are:

HCAL Barrel (HB): Encircling the Electromagnetic Barrel (EB), the HB is composed of alternating layers of brass and plastic scintillators. The structure consists of 32 modules, each incorporating approximately 1,700 scintillating crystals. The light produced from scintillation is collected via optical fibers and transmitted to hybrid photodiodes (HPDs) for precise signal readout.

HCAL Endcap (HE): The HE extends the calorimetric coverage to regions of higher pseudorapidity, ensuring seamless energy measurement beyond the HB. Each endcap consists of two distinct discs,

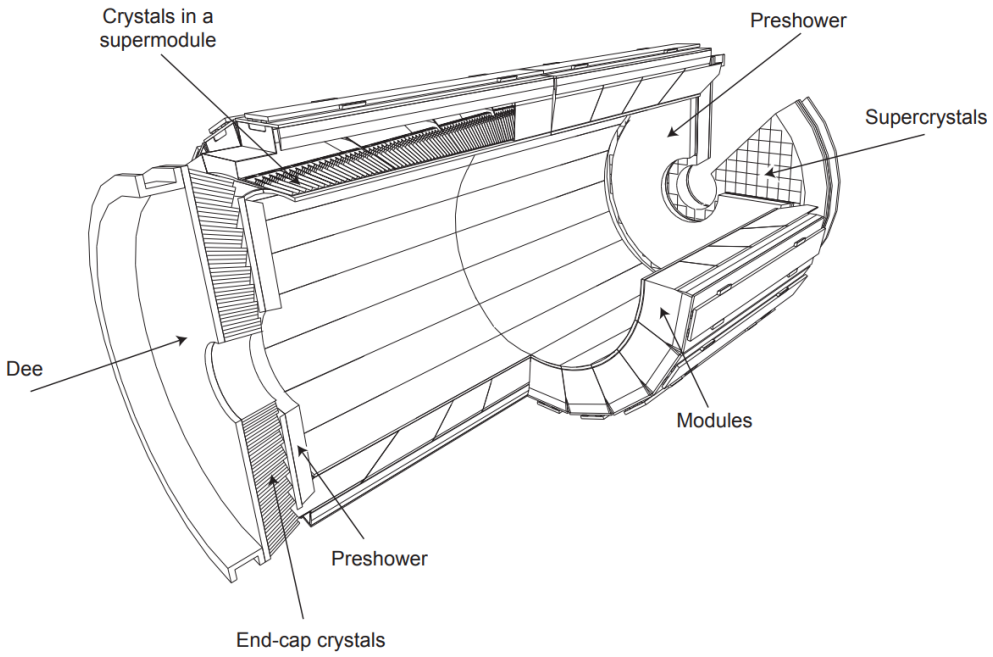


Figure 1.13: Diagram of the CMS electromagnetic calorimeter illustrating the configuration of crystal modules, supermodules, and endcaps, with the preshower positioned in front, adopted from [11].

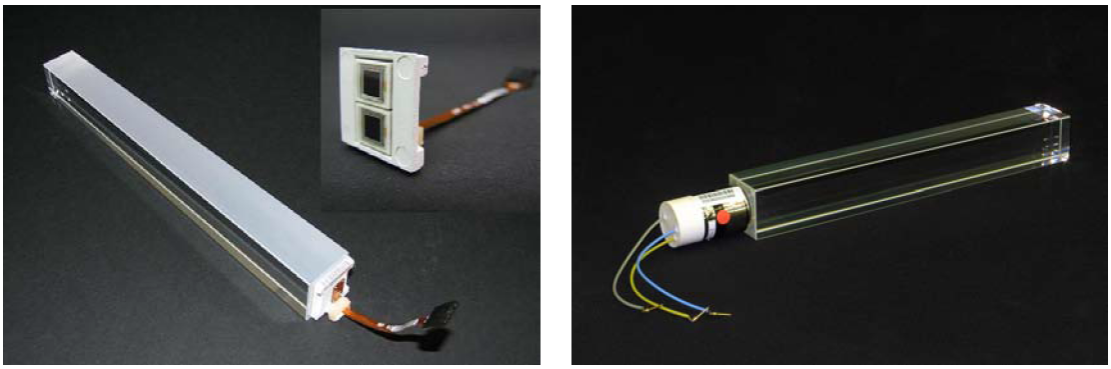


Figure 1.14: $PbWO_4$ crystals with photodetectors attached. Left: A barrel crystal with depolished upper face and APD capsule. Right: An endcap crystal with VPT, adopted from [11].

containing a total of 3,662 scintillating crystals. Silicon photomultipliers (SiPMs) are utilized in the HE to provide enhanced signal gain and superior radiation resistance.

Forward and Outer Calorimeters (HF and HO): The HF extends the HCAL coverage to pseudo-rapidities up to $|\eta| < 5.0$, which is critical for precise transverse energy measurements in the forward regions. The HO, situated externally to the HB, complements hadronic energy resolution while contributing to muon system measurements, ensuring robust energy reconstruction.

The multi-layered architecture of the HCAL facilitates efficient hadronic energy measurements while

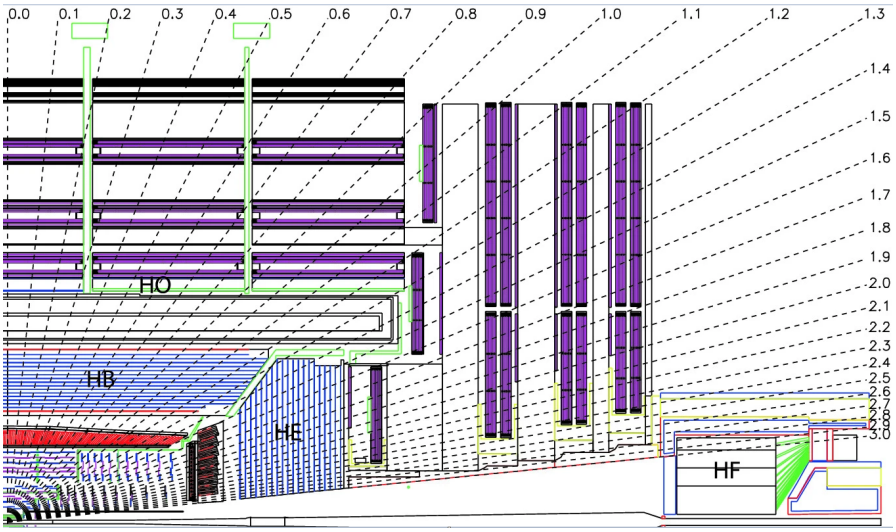


Figure 1.15: A cross-sectional view of the CMS HCAL [11].

ensuring reliable calculations of missing transverse energy (E_T^{miss}), which plays a crucial role in the detection of weakly interacting particles such as neutrinos.

Superconducting Solenoid

The superconducting solenoid magnet is a central component of the CMS detector, essential for enabling precise momentum measurements of charged particles. The solenoid is a 12.5 m long cylindrical structure with a diameter of 6.3 m and a mass exceeding 12,000 t, making it the heaviest single element of the CMS detector. It is designed to generate a uniform magnetic field of 3.8 T, which bends the trajectories of charged particles as they traverse the detector, enabling accurate determination of their momenta through the tracker.

The solenoid's coil is constructed from superconducting niobium-titanium (NbTi) cables, which are cooled to 4.5 K using liquid helium to maintain superconductivity. The coil carries an electric current of up to 18 kA, ensuring the generation of the powerful magnetic field required for precise particle trajectory bending. The solenoid's magnetic field extends outward and is returned through a 1.9 m thick iron yoke, which also serves to support the muon system. The yoke is segmented into multiple layers to interleave with muon detectors and enhance their efficiency.

This system is critical not only for bending charged particle trajectories but also for achieving the high-resolution momentum measurements necessary for the CMS experiment's physics goals.

Muon System

The muon detection system [64] forms the outermost layer of the CMS detector and is primarily designed to detect muons, which are minimally ionizing particles that traverse the dense iron return yoke with limited energy loss. While other high-energy charged particles, such as hadrons, can occasionally pass through the system, muons are distinguishable due to their specific ionization patterns and ability to penetrate the detector layers with minimal interaction.

This system enables precise tracking and identification of muons, supporting a wide range of physics analyses. These include studies of Higgs boson decays, such as $H \to ZZ^* \to 4\ell$, where muons appear in the final state, as well as searches for phenomena beyond the Standard Model and tests of theoretical

predictions. The muon system integrates seamlessly with the CMS detector to provide detailed event reconstruction in high-luminosity collision environments.

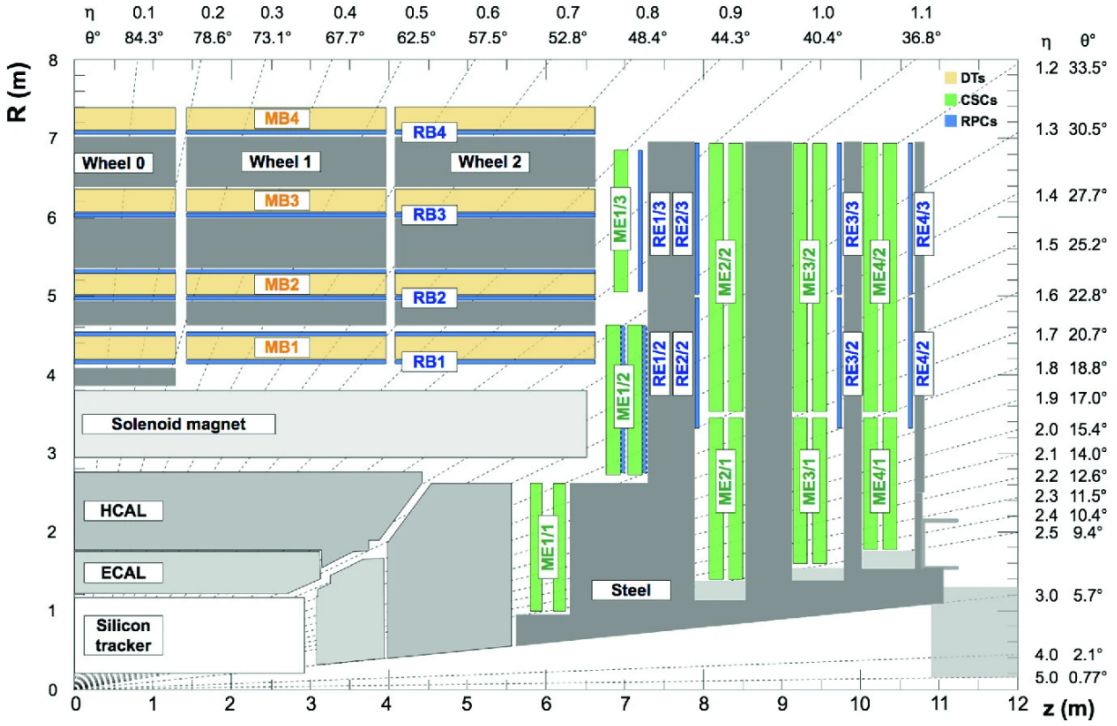


Figure 1.16: A cross-sectional view of the CMS Muon system [11].

Figure 1.16 shows a cross-sectioanl view of differet subparts of the Muon system. The Muon system utilizes four distinct types of gaseous detectors interleaved with the iron return yoke, which also contains the superconducting solenoid's magnetic field. These detectors are optimized for different functions, including tracking, triggering, and time measurement. The primary components are:

Drift Tubes (DTs): Located in the barrel region ($|\eta| < 1.2$), the DT chambers are used for precise position measurements. The barrel contains 250 DT chambers, each capable of measuring the drift time of ionized electrons with a precision of approximately 380 ns. This configuration ensures accurate muon tracking in the lower radiation and flux environment of the barrel region.

Cathode Strip Chambers (CSCs): Situated in the endcap region ($1.2 < |\eta| < 2.4$), the CSCs are designed to handle the high particle flux and radiation levels typical of the forward regions. The endcaps consist of 468 CSCs, arranged in 3–4 layers depending on the detector's radial position, providing excellent spatial resolution and robust muon tracking under challenging conditions.

Resistive Plate Chambers (RPCs): Used in both the barrel and endcap regions for fast triggering. The RPCs have excellent time resolution, enabling efficient identification of collision events involving muons. These chambers provide redundancy and complement the DTs and CSCs for robust muon identification.

Gas Electron Multipliers (GEMs): Recently introduced in the forward region during LS2 to extend coverage and enhance muon tracking in the highest radiation areas ($2.4 < |\eta| < 3.0$). GEMs offer high granularity and radiation resistance, making them essential for future high-luminosity operations.

The muon system achieves a spatial resolution of approximately 100 µm and a timing resolution of 1 ns, enabling precise reconstruction of muon trajectories and their momenta. The combination of DTs,

CSCs, RPCs, and GEMs ensures full 4π solid-angle coverage, providing redundancy and robustness for muon identification in diverse collision environments.

The integration of the muon system with the rest of the CMS detector allows for accurate measurements of missing transverse energy (E_T^{miss}) and detailed studies of events involving muons.

The CMS Trigger System

To handle the immense data rates generated by collisions at the LHC, where bunch crossings occur every 25 ns, the CMS experiment employs a two-stage trigger system. This system is essential for reducing the overwhelming event rates to manageable levels while retaining only the most relevant data for physics analyses.

The first stage, known as Level 1 (L1), is a hardware-based trigger that utilizes custom electronics to process data from the calorimeter and muon detectors. Trigger primitives, such as energy deposits in the calorimeters and muon chamber hits, are combined regionally to identify candidate trigger objects. These are then forwarded to the Global Trigger, which makes a trigger decision within a latency of 4 µs. The L1 system reduces the input event rate from the 40 MHz LHC bunch crossing frequency to a manageable 100 kHz.

The second stage called the High-Level Trigger (HLT), operates on a farm of commercial processors and processes the full detector data. Advanced algorithms are applied at this stage to refine the event selection, allowing for the retention of physics-rich events. The HLT further reduces the event rate to approximately 1 kHz, with selected events stored for offline analysis.

This two-stage trigger system facilitates efficient data acquisition and supports precision physics analyses at the CMS experiment.

1.6 Phase-II Challenges for the CMS

The HL-LHC will transform detector operations by significantly increasing instantaneous and integrated luminosity. This will lead to higher particle hit rates, more simultaneous interactions per collision (140–200), and increased radiation levels. To leverage HL-LHC's enhanced performance, CMS detectors must undergo significant upgrades for three primary reasons:

- Radiation degrades sensing elements and electronics over time.
- Current electronics cannot handle expected high hit, data, and trigger rates.
- High pileup events degrade performance, resulting in high track densities per unit area.

One of the key challenges for the HL-LHC is the substantial increase in radiation levels due to collision rates reaching up to 5×10^9 interactions per second. This high radiation environment poses severe risks to detector materials and associated electronics, particularly near the beam pipe where radiation intensity is most pronounced. As shown in figure 1.17, simulations at an integrated luminosity of 3000 fb^{-1} indicate absorbed doses reaching 1 Grad (10^7 Gy) and fluences up to $2 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$. The red line in the figure marks the threshold beyond which the radiation levels exceed the existing CMS design specifications. To counteract these formidable conditions, it is imperative to incorporate radiation-hardened materials and innovate design enhancements to ensure the enduring functionality of detectors under such extreme circumstances [14].

The increased trigger and data rates present another challenge. In Phase-II, the maximum trigger frequencies will rise to 750 kHz for L1-Trigger and 7.5 kHz for the HLT, with latencies extending to 12.5 µs. These requirements demand enhanced detector granularity, updated electronics, and expanded data bandwidth to handle the increased volume of information.

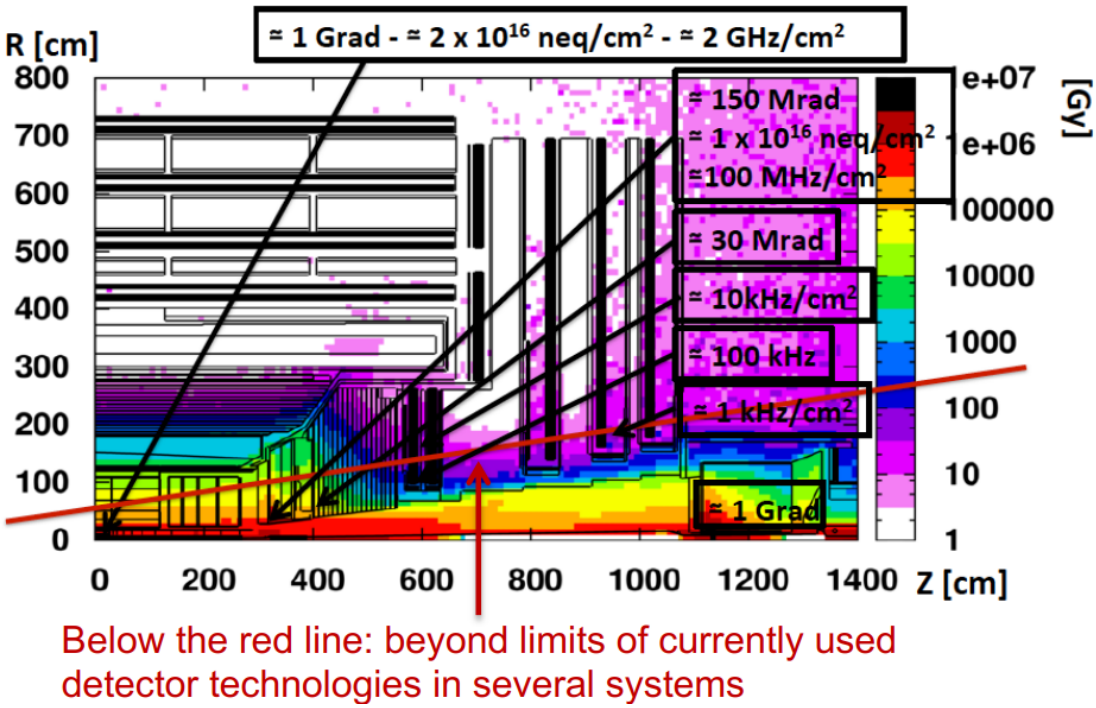


Figure 1.17: Absorbed dose in the CMS cavern after an integrated luminosity of 3000 fb^{-1}. The transverse distance from the beamline is represented by R (in cm), and the distance along the beamline from the Interaction Point at $Z = 0$ is denoted by Z (in cm). The absorbed dose near the beamline reaches up to 1 Grad (10^7 Gy), and the maximum fluence recorded is 2×10^{16} n_{eq}/cm^2. The red line indicates the limits of currently used detector technologies in several systems. Adopted from ref. [12] (slide 17).

High pileup, with up to 140 interactions per bunch crossing, further complicates the Phase-II operations by creating dense track environments. This significantly challenges event reconstruction and degrades detector performance. Upgrades to the tracking and calorimetry systems are essential to mitigate the effects of pileup, maintain high-resolution measurements, and enable accurate particle identification.

To address these challenges, several sub-detectors are being enhanced or replaced, and new systems are under development to improve performance in high-luminosity conditions. Major installations are planned for LS3 (2026–2029), building on the upgrades implemented during LS2. These efforts will ensure the CMS detector is well-prepared to meet the demands of HL-LHC operations, maintaining its ability to deliver precise and reliable data for physics analyses [14, 50].

1.7 Phase-II Upgrades to CMS Sub-Detectors

To address the challenges posed by the Phase-II operation of the HL-LHC, the CMS detector requires extensive upgrades across multiple subsystems. Detailed information about these upgrades can be found in [14, 50, 65, 66]. A brief summary of these upgrades is provided below:

Silicon Tracker As a cornerstone of the CMS Phase-II upgrades, the new silicon tracker is designed to sustain optimal performance under the unprecedented particle flux and radiation levels of the HL-LHC.

The upgraded tracker significantly enhances granularity, increasing the number of readout channels by a factor of 25 compared to its predecessor. This advancement includes approximately 2×10^9 hybrid micropixels in the Inner Tracker (IT) and 43×10^6 microstrip sensors along with 170×10^6 macropixels in the Outer Tracker (OT).

The new tracker extends the pseudorapidity coverage to $|\eta| < 4.0$, enabling broader acceptance and improved tracking efficiency in the forward regions. Designed for increased radiation tolerance, it is capable of withstanding radiation levels up to an order of magnitude higher than those endured by the existing tracking system. The OT incorporates an advanced Level-1 (L1) trigger functionality, leveraging hit coincidences, or *stubs*, to facilitate transverse momentum discrimination. These enhancements ensure precise track reconstruction and robust performance, even under extreme pileup conditions [67].

Timing Layer Introducing an advanced timing layer is crucial for mitigating pileup effects, which can significantly impair event reconstruction accuracy. These new timing detectors will achieve an impressive time resolution of 30-50 ps, enabling precise differentiation of overlapping vertices and enhancing the isolation of leptons and photons. This, in turn, improves the reconstruction of hadronic jets and missing transverse momentum. The Barrel Timing Layer (BTL), incorporating Cerium-doped LYSO crystals read out by Silicon Photomultipliers (SiPMs), will cover the central region. Meanwhile, the Endcap Timing Layer (ETL) will utilize Low-Gain Avalanche Detectors (LGADs) to extend coverage to higher pseudorapidities, thereby bolstering the detector's capacity to search for long-lived particles [68].

Calorimetry Significant upgrades to the calorimetry system will markedly improve its energy resolution and timing precision. The barrel electromagnetic (EM) calorimeter will retain its PbWO4 crystals but be enhanced with upgraded front-end electronics, achieving a 30 ps resolution for electrons and photons. The endcap ECAL and HCAL will be replaced by the HGCal, an 5D (x, y, z, E, t) imaging calorimeter with electromagentics (CEE) and hadronics (CEH) parts, provide unprecednet transvers and laterral granularity with 6 million silicon sensor channels and 250,000 scintillator tiles read out by SiPMs. These advancements will enable precise particle flow reconstruction and expand the detector's reach for vector boson fusion, and long-lived particle searches [6, 65].

Muon System The CMS Phase-II muon system is undergoing extensive upgrades to meet the stringent requirements of the HL-LHC. These enhancements aim to improve the system's performance, redundancy, and geometric coverage, ensuring accurate muon detection in the HL-LHC enviroment.

The current muon detectors, consisting of DT, CSC, RPC, will be upgraded with advanced electronics to handle increased trigger rates and improve timing resolution. RPCs will achieve a timing precision of 1.5 ns, while DT chambers will reach 2 ns, providing precise timing data for the L1-trigger. To mitigate radiation effects, the upgraded components will include radiation-hard materials and operate at reduced voltages. Furthermore, FPGA-based trigger systems will enhance the sensitivity of the muon detectors to rare decay modes and long-lived particles, supporting a broader range of physics analyses.

The forward region will see significant improvements with the installation of new GEM detectors and upgraded RPCs (iRPCs), extending the detector's coverage to $|\eta| = 2.8$. The GE2/1 and ME0 stations will enhance spatial resolution and provide robust radiation resistance, addressing the challenges posed by high-luminosity environments. These upgrades will complement the existing GE1/1 stations installed during LS2. The forward RPCs, such as RE3/1 and RE4/1, will be replaced with iRPCs to improve timing precision and ensure efficient muon identification in high-pileup conditions.

The integration of these upgrades will significantly enhance the muon system's geometric coverage, timing, and trigger efficiency. The combined improvements will strengthen the CMS detector's capability to handle the complex collision environments of the HL-LHC, facilitating precision measurements and advancing the search for new physics [69].

Beam Instrumentation and Luminosity The Beam Radiation Instrumentation and Luminosity (BRIL) project will introduce cutting-edge systems for beam timing, beam loss monitoring, and luminosity measurements. A new dedicated bunch-by-bunch luminometer, the Fast Beam Condition Monitor (FBCM), will provide high-precision luminosity determination, essential for accurate Higgs cross-section measurements. This system will employ silicon pad sensors with fast front-end ASICs, ensuring real-time feedback on beam conditions and enhancing the protection of sensitive CMS instrumentation. The design draws from the successful Run 2 Upgraded Fast Beams Conditions Monitor (BCM1F) concept, integrating Phase-II technology to maintain performance and reliability throughout the HL-LHC era.

These upgrades will enable the CMS detector to fully exploit the HL-LHC's capabilities, paving the way for groundbreaking discoveries and advancing our understanding of fundamental physics. This meticulous planning and execution will ensure that the CMS experiment remains at the forefront of particle physics research well into the future [70].

1.8 CMS Phase-II Calorimeter System Challenges

The existing CMS calorimeters were originally designed to operate under a maximum integrated luminosity of $500\,\mathrm{fb}^{-1}$ at a peak instantaneous luminosity of $1\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Following the Phase-I upgrades, the HCAL was enhanced to accommodate luminosities up to $2\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. In anticipation of the HL-LHC phase, luminosities are projected to reach about $5-7\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, significantly elevating the integrated luminosity to $3000\,\mathrm{fb}^{-1}$. This substantial increase necessitates extensive upgrades or replacements of critical calorimeter components to ensure operational integrity under these heightened conditions [14]. Following are the key challenges foreseen by the CMS calorimeters:

Radiation Challenges: The Phase-II upgrade of the CMS detector presents significant operational challenges due to extreme radiation levels, particularly in the endcap regions. Simulation studies, as illustrated in figures 1.18 and 1.19, evaluate the absorbed radiation dose and neutron fluence at an integrated luminosity of $3000\,\mathrm{fb}^{-1}$. The results indicate that the absorbed dose reaches up to 2 MGy, while the neutron fluence exceeds $1\times10^{16}\,\mathrm{cm}^{-2}$ in the forward region. These radiation levels significantly exceed the original design specifications of the calorimeter components, particularly within the pseudo-rapidity range $1.48<|\eta|<3.0$.

Sustained exposure to such high radiation levels induces severe performance degradation, leading to increased leakage currents, charge trapping in silicon sensors, and material deterioration. Consequently, these effects reduce the signal-to-noise ratio and deteriorate the energy resolution of the calorimeter. To ensure optimal detector performance under HL-LHC conditions, the implementation of radiation-hard sensor technologies, enhanced cooling mechanisms, and advanced calibration methodologies is essential to mitigate the impact of radiation-induced aging.

ECAL's components degradation: The ECAL experiences performance degradation due to prolonged exposure to ionizing radiation. A key factor contributing to this degradation is the formation of color centers in $PbWO_4$ crystals, which occurs when ionizing radiation induces defects in the crystal lattice. These defects trap charge carriers, creating absorption centers that reduce the transmission of scintillation light and, consequently, the overall calorimeter response.

Figure 1.20 illustrates the evolution of the ECAL response to laser light between 2011 and 2018 across different η regions. A notable reduction in response exceeding 80% is observed in the high-$|\eta|$ region ($|\eta|>2.4$), while the barrel region ($|\eta|<1.4$) exhibits a significantly smaller decline of approximately 10%. This differential response highlights the increasing impact of radiation damage with increasing pseudorapidity.

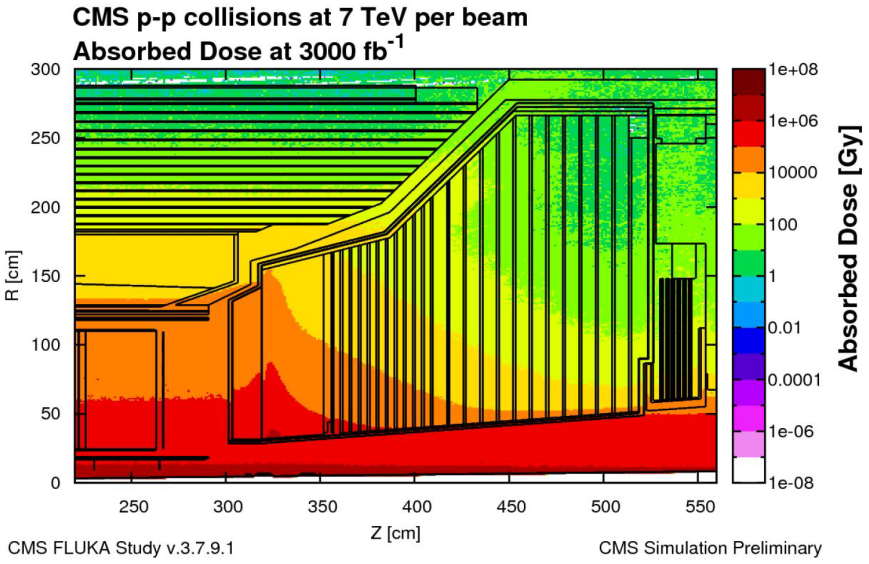


Figure 1.18: Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of 3000 fb^{-1}, simulated using the FLUKA program. This is depicted as a two-dimensional map with radial (r) and longitudinal (z) coordinates [6].

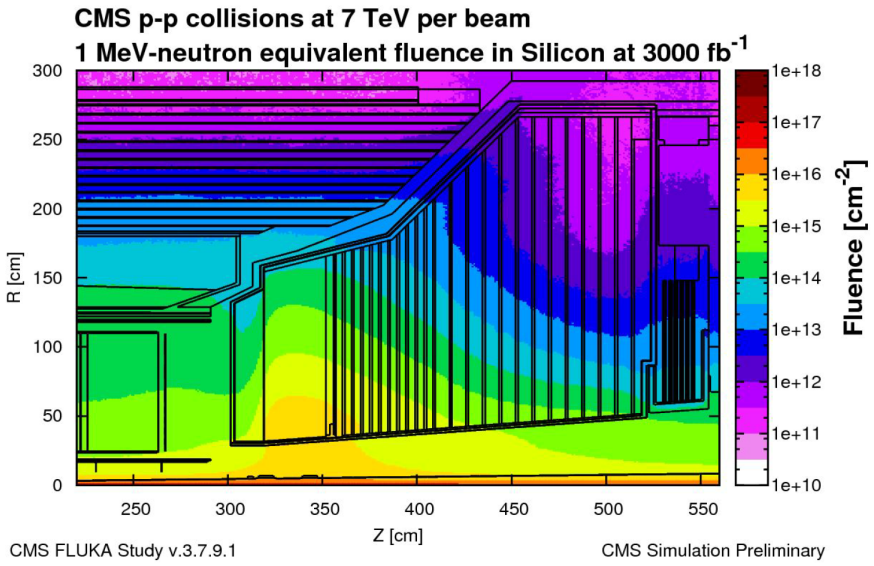


Figure 1.19: Simulated distribution of 1 MeV neutron-equivalent fluence within the HGCAL volume, corresponding to CMS proton–proton collisions at $\sqrt{s} = 7$ TeV per beam after an integrated luminosity of 3000 fb^{-1}. The map, produced using the FLUKA simulation toolkit, is presented as a function of radial (R) and longitudinal (Z) coordinates, and illustrates the radiation environment relevant for the design and qualification of HGCAL components [6].

Beyond signal attenuation in $PbWO_4$ crystals, radiation-induced effects also impact the photodetec-

tors, contributing to elevated noise levels and deteriorating energy resolution. Figure 1.21 (left) presents the projected sensitivity of ECAL at different integrated luminosities, while the right panel quantifies the degradation of energy resolution, $\sigma_{\text{eff}}(E)/E$, for photons from Higgs boson decays across different pileup conditions. These results underscore the challenge of maintaining energy resolution, particularly in the endcap region, where the cumulative radiation exposure is significantly higher.

While the barrel ECAL remains viable for continued operation with upgraded electronics, the severe degradation observed in the endcap necessitates a full replacement to meet the stringent performance requirements of the High-Luminosity LHC (HL-LHC) era.

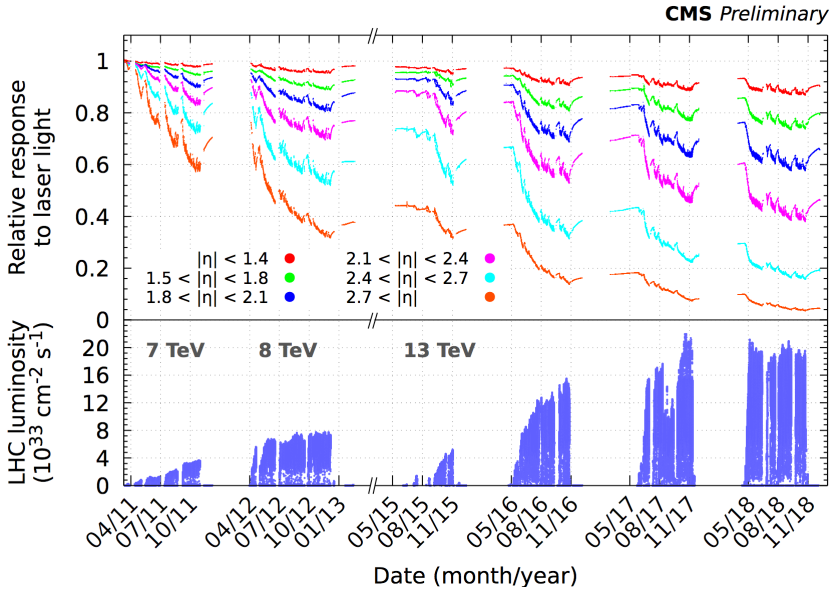


Figure 1.20: The CMS ECAL crystal response to laser light during 2011-2018 at different η: Measured at 440 nm (2011) and 447 nm (from 2012 onwards), is shown for multiple pseudorapidity intervals. Each curve represents the average normalized response for ECAL crystals within a given η bin, indicating the degree of radiation-induced transparency loss. The maximum degradation reaches approximately 13% in the ECAL barrel and up to 62% at $|\eta| \sim 2.5$, near the edge of the tracker acceptance. Periods of signal recovery during LHC shutdowns are visible, reflecting the partial annealing of radiation damage. The lower panel displays the corresponding instantaneous LHC luminosity, illustrating the direct correlation between accumulated dose and signal loss. These measurements, performed every 40 minutes, are used to correct physics data for radiation effects in the ECAL response [13].

HCAL Challenges: The HCAL faces significant performance degradation due to radiation exposure, particularly in the HE tiles. During the 2012 run, these tiles experienced a 30% decrease in light output after exposure to 10^3 Gy, as shown in figure 1.22. Projections for 3000 fb^{-1} suggest further attenuation, necessitating the replacement of the HE. The reduced light yield impacts the calorimeter's ability to accurately measure hadronic showers, undermining jet energy resolution and missing transverse energy calculations.

HO and HF Challenges: The outer hadronic calorimeter (HO) and forward calorimeter (HF) are less affected by radiation compared to the endcap components. The HO remains largely unaffected due to its

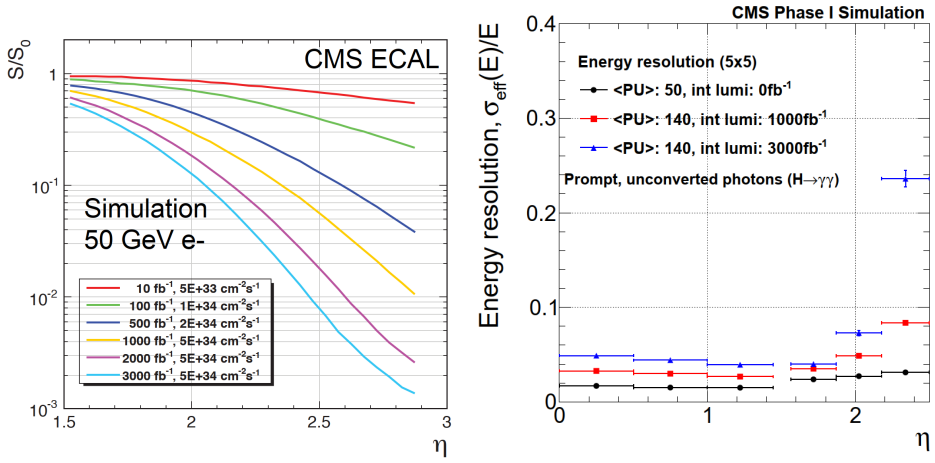


Figure 1.21: ECAL sensitivity at different integral luminosity levels (left) and energy resolution $\sigma_{\text{eff}}(E)/E$ for photons from Higgs boson decay, shown for different integrated luminosities and pileup levels (right), taken from [14].

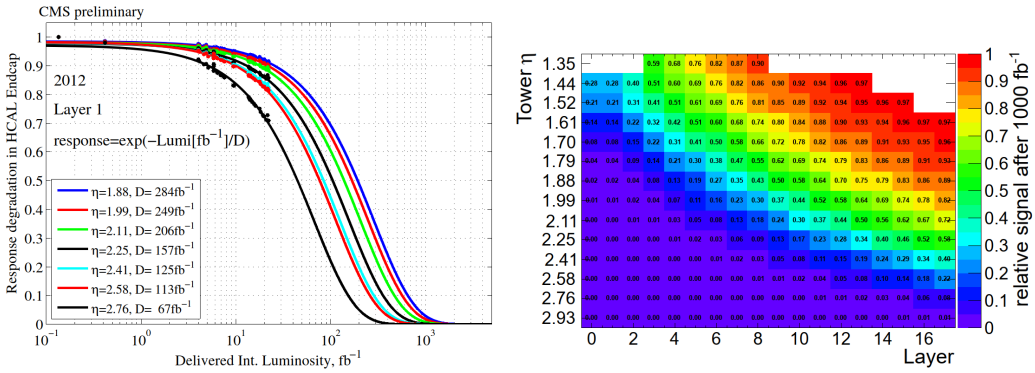


Figure 1.22: The decrease in light signal from the first layer of HE as a function of accumulated luminosity for various tile positions (η) is shown, along with an exponential fit, taken from [14] (left), the expected light attenuation from different HE tiles at $L = 3000\text{fb}^{-1}$ (right).

location, while the HF is specifically designed to withstand high radiation levels. Both calorimeters can meet Phase-II requirements without significant upgrades.

1.8.1 Transition to the High Granularity Calorimeter (HGCAL)

Given these challenges, the ECAL and HCAL endcaps cannot meet the Phase-II requirements and will be replaced by the High Granularity Calorimeter (HGCAL) [6]. The HGCAL, shown in figure 1.23, introduces a 5D calorimetry concept, offering enhanced spatial and timing resolution, improved radiation hardness, and superior performance under high pileup conditions. This advanced design ensures that the CMS detector remains capable of delivering precise measurements and robust particle identification during HL-LHC operations. A detailed discussion of the HGCAL design and functionality will be presented in the next chapter.

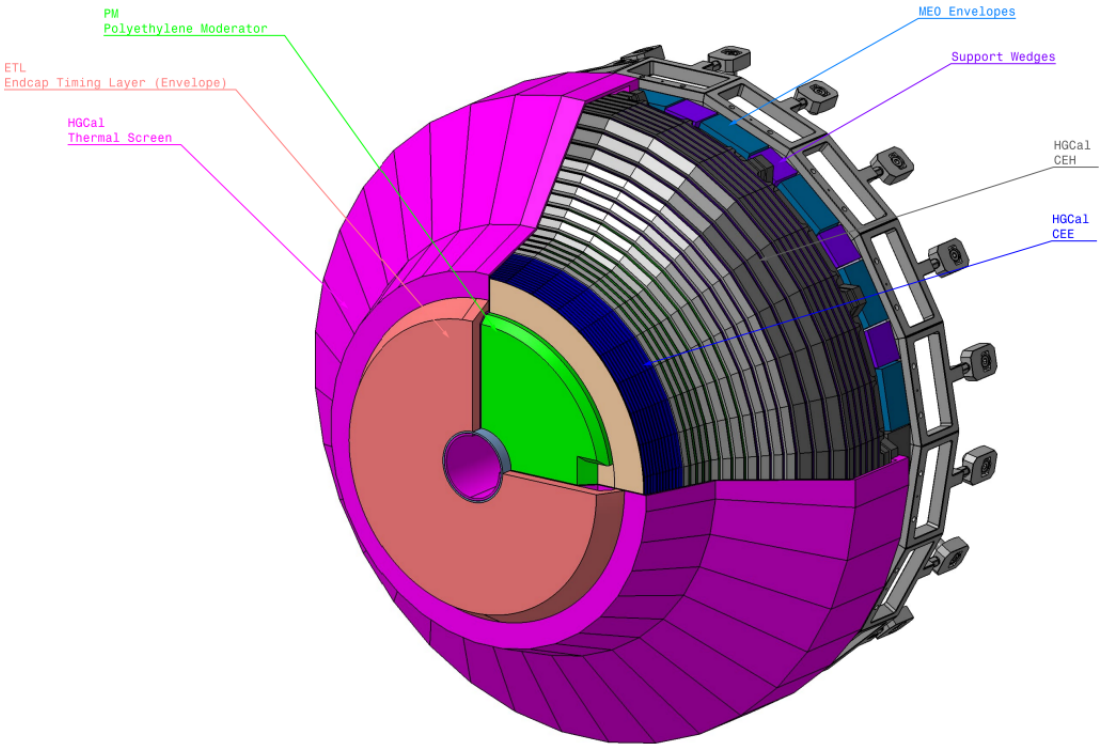


Figure 1.23: The Isometric view of the 47-layer HGCAL model.

1.9 Conclusion

This chapter provided a comprehensive introduction to the LHC and its physics objectives, along with an overview of the challenges and advancements associated with the HL-LHC era. Starting with the operational principles of the LHC and its remarkable achievements, the discussion transitioned to the primary goals of the HL-LHC, which include increasing the luminosity to enable more precise measurements and access to rare processes.

The chapter also outlined the structure and functionality of the CMS detector, highlighting the role of its key subsystems, such as the tracker, calorimeters, muon system, and the triggering framework. Each subsystem was presented in the context of its contributions to particle detection and the challenges it faces due to the harsher operating environment of the HL-LHC. Special emphasis was given to the calorimeter systems, particularly the electromagnetic and hadronic calorimeters, which are vital for accurate particle energy measurements but are significantly impacted by increased radiation and pileup.

To address these challenges, the CMS detector will undergo major upgrades during the Phase-II program. Among the critical upgrades is the replacement of the endcap calorimeters with the High Granularity Calorimeter (HGCAL), a cutting-edge technology that will enhance spatial and timing precision while maintaining reliability in extreme conditions. This marks a significant step forward in the detector's ability to handle high luminosity and high pileup scenarios.

Chapter 2

Introduction to HGCAL and Its integral parts

2.1 Introduction

The High Granularity Calorimeter (HGCAL) represents a major upgrade designed to prepare the CMS detector for the HL-LHC operational phase. This state-of-the-art detector will replace the existing Endcap ECAL and HCAL subsystems, ensuring exceptional performance under the extreme conditions of intense radiation and high pileup densities while maintaining precision in energy, spatial, and timing measurements.

The primary motivation for the HGCAL, discussed in Section 2.2, arises from the limitations of the current CMS endcap calorimeters. These systems face significant performance degradation under HL-LHC conditions. To ensure precise physics measurements in this challenging environment, a complete replacement with a highly segmented, radiation-tolerant, and cost-efficient calorimeter is imperative.

Section 2.3 provides a detailed overview of the HGCAL's structure, emphasising its division into electromagnetic (CE-E) and hadronic (CE-H) compartments. The CE-E employs silicon sensors throughout, leveraging their exceptional radiation hardness and timing precision. In the CE-H, a hybrid design is adopted, with silicon modules in high-radiation regions and cost-effective scintillator tiles in areas of lower radiation exposure. This approach balances cost efficiency with high performance.

The design and implementation of silicon sensors, a pivotal component of the HGCAL, are examined in Section 2.4. This section addresses critical design considerations, including the choice of silicon as the active material, the rationale behind its hexagonal geometry, the deployment of varying sensor thicknesses and cell sizes, and the adoption of n-on-p DC-coupled sensors for their superior charge collection efficiency in high-fluence environments.

The granularity of HGCAL is addressed in Section 2.5, which highlights its unprecedented longitudinal and lateral segmentation. This configuration enables precise reconstruction of electromagnetic and hadronic showers, significantly improving the resolution of physics objects. The modular architecture, described in Section 2.6, allows for efficient assembly and integration, facilitating maintenance and scalability. The overarching physics objectives of the HGCAL are presented in Section 2.7, and a comparative evaluation with other calorimeter systems at the LHC is provided in Section 2.8.

The focus of this thesis is the readout design and implementation for the silicon region of the HGCAL. Emphasis is placed on the silicon sensors, silicon-only cassettes, and silicon modules. This chapter lays the foundation for comprehending the HGCAL's innovative design and its pivotal role in advancing the

physics program at the HL-LHC.

2.2 Motivation

The HL-LHC will introduce significant challenges, including a high-radiation environment and extreme pile-up conditions, as detailed in Section 1.8. These operational conditions exceed the design limits of the current CMS Endcap calorimeter systems, including the ECAL and HCAL, necessitating their replacement.

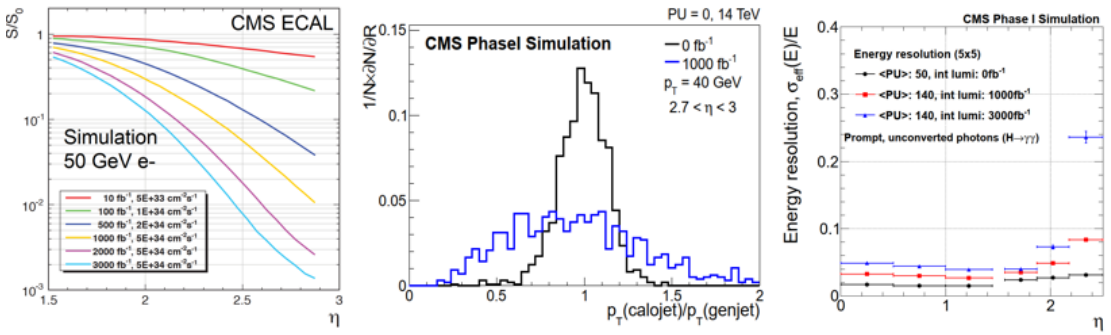


Figure 2.1: Performance degradation of the existing CMS calorimeters: (Left) Loss of scintillation light output (S/S_0) in $PbWO_4$ crystals as a function of pseudorapidity (η) for a 50 GeV electron under various radiation conditions. (Middle) Jet energy resolution ($p_T^{\text{calojet}}/p_T^{\text{genjet}}$) comparison at integrated luminosities of 0 fb^{-1} and 1000 fb^{-1}, showing degradation due to radiation. (Right) Photon energy resolution ($\sigma_{\text{eff}}(E)/E$) versus η, illustrating worsening performance with increased pile-up adopted from [14].

Figure 2.1 summarizes the critical performance degradations of the current Endcap calorimeters under the extreme conditions of the HL-LHC. The left panel demonstrates the loss of scintillation light output (S/S_0) in $PbWO_4$ crystals as radiation levels increase, particularly in forward pseudorapidity (η), resulting in significant sensitivity losses. The middle panel compares the jet energy resolution ($p_T^{\text{calojet}}/p_T^{\text{genjet}}$) at integrated luminosities of 0 fb^{-1} and 1000 fb^{-1}, highlighting substantial degradation due to accumulated radiation effects, which impair the accuracy of momentum reconstruction. The right panel shows the worsening photon energy resolution ($\sigma_{\text{eff}}(E)/E$) with increasing pile-up, further emphasizing the inability of the current system to deliver precise energy measurements.

To address these limitations, the existing Endcap ECAL and HCAL will be replaced by the High Granularity Calorimeter (HGCAL). With its high radiation tolerance and fine granularity, the HGCAL is specifically designed to cope with the Phase-II challenges of the HL-LHC, ensuring precise energy under extreme conditions.

2.2.1 Desired Specifications for the New System

The HGCAL upgrade demands several critical specifications to ensure optimal performance over its full operational lifetime. These specifications are essential to maintain energy resolution, signal-to-noise ratio, calibration accuracy, and data bandwidth, ensuring that the physics performance remains at Phase-I levels even under the increasingly challenging operational conditions of the HL-LHC. The key specifications are summarized in Table 2.1.

Specification	Details
Radiation Tolerance	Preserve energy resolution post 3000fb^{-1}; inter-cell calibration $\approx 3\%$ using MIP signals
Dense Calorimeter	Maintain lateral compactness of showers
Fine Lateral Granularity	Small cell sizes $\left(\approx 0.5-1\ \text{cm}^2\right)$; high S/N ratio; two-shower separation for pileup mitigation.
Fine Longitudinal Granularity	Fine sampling of showers; good electromagnetic energy resolution, pattern recognition.
Precision Timing Measurement	Precise timing for high-energy showers; pileup rejection; vertex identification measurement.
Trigger Contribution	Contribute to the level-1 trigger decision

Table 2.1: Requirements for the HGCAL upgrades, adapted from [6].

2.3 High Granularity Calorimeter (HGCAL)

The High Granularity Calorimeter (HGCAL) is a state-of-the-art 5D imaging calorimeter designed to address the stringent requirements imposed by the HL-LHC, including elevated radiation levels and high event pileup densities. As part of the CMS Phase-II upgrade, HGCAL will replace the existing endcap calorimeter systems (ECAL, HCAL, and Pre-shower) during the Long Shutdown 3 (LS3), ensuring enhanced performance for both electromagnetic and hadronic energy measurements under extreme HL-LHC conditions. Its design enables high-precision reconstruction of complex event topologies by capturing multi-dimensional information, spatial coordinates (x, y, z), deposited energy (E), and time of arrival (t), establishing it as a true 5D imaging calorimeter.

Figure 2.2 presents an overview of HGCAL's layered configuration, revealing its division into two functionally distinct yet complementary compartments: the electromagnetic endcap (CE-E) and the hadronic endcap (CE-H). The CE-E, positioned closest to the interaction region, comprises 26 sampling layers (13 double layers) utilizing Cu, CuW, and Pb absorbers. These are interleaved with radiation-hard silicon sensors, selected for their excellent timing response and high granularity. The CE-E achieves a depth of approximately 25 radiation lengths (X_0), enabling fine segmentation for electromagnetic shower resolution.

In contrast, the CE-H section, situated downstream, consists of 21 layers employing stainless steel absorbers. Here, silicon is retained in the innermost, high-radiation regions, while the outer zones adopt cost-effective plastic scintillator tiles instrumented with silicon photomultipliers (SiPMs). This hybrid active medium balances performance and cost, extending the total interaction depth by 8.5 nuclear interaction lengths (λ).

To ensure optimal spatial and timing performance, the inner CE-H and entire CE-E regions are instrumented with silicon Hex-Modules, while the outer CE-H regions utilize scintillator tiles. Figure 2.3 illustrates this dual-layer configuration. The silicon-only layer from CE-E (left) shows a radial segmentation of sensors by thickness 300 μm, 200 μm, and 120 μm to align with varying radiation fluences. In contrast, the CE-H layer (right) demonstrates a hybrid layout, combining inner silicon modules with outer scintillator tiles to maintain detection performance in a cost-conscious design.

Silicon sensors and Hex-Modules: The silicon sensors, chosen for their radiation hardness and superior timing response, form the foundation of HGCAL's high-performance layers. A total of 620 m^2 of silicon hexagonal sensors are employed, segmented into three thicknesses: 120 μm, 200 μm, and 300 μm. These sensors are diced from 8-inch circular wafers into hexagonal modules for optimal material utilization. Each module is integrated into the HGCAL cassettes, which are assembled to form

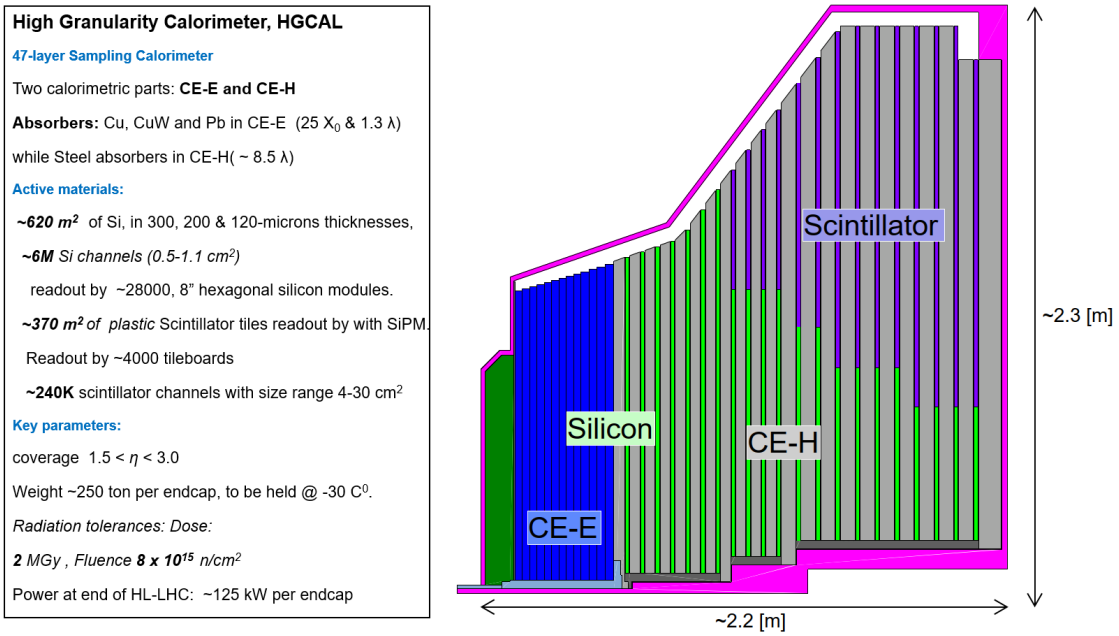


Figure 2.2: Cross-sectional view of HGCAL: The electromagnetic compartment (CE-E) and hadronic compartment (CE-H) incorporate silicon and scintillator layers with different absorber materials, achieving both high resolution and radiation tolerance.

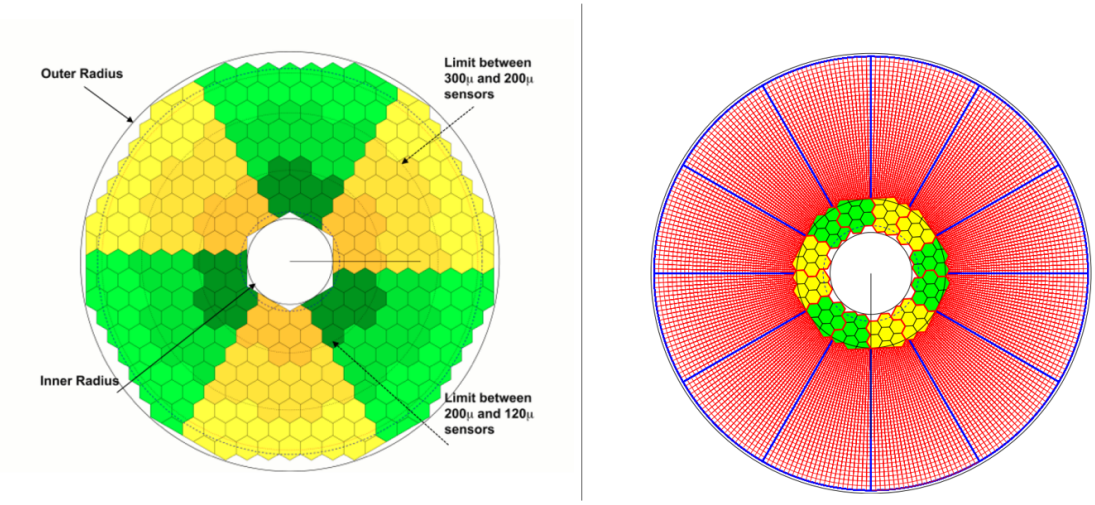
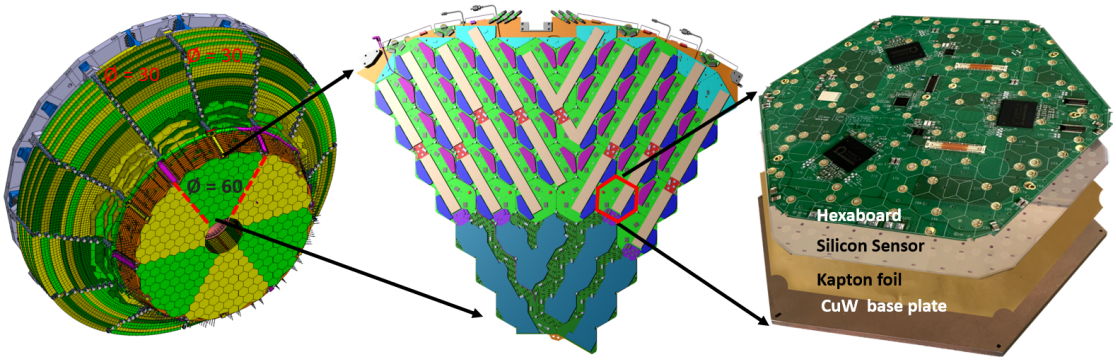


Figure 2.3: Representative HGCAL layers: (Left) A CE-E silicon-only layer with graded sensor thicknesses optimized for fluence. (Right) A CE-H mixed layer featuring silicon in high-radiation zones and scintillator tiles in low-radiation regions.

detector layers.

Figure 2.4 illustrates the hierarchical structure: the detector model (a), a cassette with silicon modules (b), and a silicon Hex-Module (c). The modules are further classified into high-density (HD) and low-

density (LD) configurations. HD modules, with smaller 0.51 cm^2 pad-size sensors, are deployed in high-fluence regions, while LD modules, featuring larger 1.18 cm^2 pad-size sensors, are used in lower-fluence regions.



(a) The 47-layer HGCAL model (b) A cassette (c) A silicon Hex-Module

Figure 2.4: Illustration of the HGCAL structure: (a) The 47-layer HGCAL model showing the segmentation of the detector into hexagonal modules, (b) a detailed view of a cassette from the silicon-only layer, and (c) a silicon Hex-Module comprising a CuW base plate, Kapton foil, silicon sensor, and hexaboard for readout.

System performance and operational conditions: HGCAL's granular structure, comprising millions of readout channels, delivers exceptional spatial resolution for precise shower separation. Its ability to measure timing with a resolution of approximately 30 ps enables effective pileup mitigation, addressing one of the key challenges of HL-LHC operations. The dense layering enhances the detector's capability to reconstruct complex event topologies, substantially contributing to the CMS physics programme.

The entire HGCAL is maintained at a cryogenic temperature of $-30°C$ using a bi-phase CO_2 cooling system. This approach not only ensures the radiation hardness of silicon sensors but also improves the performance of SiPMs in the scintillator layers. Detector calibration, performed using minimum ionizing particles (MIPs), requires a high signal-to-noise ratio (> 5) to be sustained over an operational lifespan exceeding 3000 fb^{-1}. Utilising HD sensor with smaller sensor pads in high-radiation zones further enhances sensitivity to single MIPs.

The HGCAL readout electronics integrate HGCROC ASICs, combining analog and digital signal processing. The ASICs support a large dynamic range (0.2 fC to 10 pC) and precise time-of-arrival measurements for events with charge deposited greater than 12 fC. Further details on the readout system are provided in Chapters [4] and [5].

The HGCAL represents a state-of-the-art solution to the challenges of CMS pahse-II operation. By combining silicon sensors and scintillator tiles in a highly granular 47-layer architecture, HGCAL ensures precise spatial, energy, and timing measurements, enhancing the overall performance of the CMS detector. The following sections will delve deeper into the design choices for HGCAL, addressing critical questions such as why silicon was chosen as the primary active material in hexagonal shape, the rationale behind the use of different sensor thicknesses and cell sizes, and how these elements collectively contribute to achieving the unprecedented precision required at the HL-LHC.

2.4 Silicon sensors

Silicon sensors play a critical role in modern particle detection systems due to their superior energy resolution, fast timing capabilities, compact size, and radiation hardness. These sensors are fabricated from semiconductor-grade silicon, a material with a lattice structure that enables precise charge collection under high electric fields. The details about si sensor can be read from references [71–73]

Why Intrinsic Semiconductors Are Not Used: Intrinsic silicon, or pure silicon, has a low free charge carrier concentration ($n_i \sim 1.5 \times 10^{10}\,\mathrm{cm}^{-3}$ at 300 K). This concentration is not feasible for detector applications, as the signal generated by incident particles, such as MIPs, would be indistinguishable from the background thermal noise. The average energy required to create an electron-hole pair in silicon is approximately 3.6 eV [72], and an MIP typically deposits around 3.6 MeV per cm of silicon, producing $\sim 10^6$ electron-hole pairs per cm. However, this charge signal would be overwhelmed by the thermal noise from intrinsic carriers, making intrinsic silicon unsuitable for particle detection. To overcome this limitation, silicon is doped with impurities to enhance its conductivity and tailor its electrical properties. The doping process introduces controlled amounts of donor or acceptor atoms, creating extrinsic semiconductors with higher free charge carrier concentrations.

PN Junction and Depletion Region: Doped silicon can be configured into a PN junction by combining p-type and n-type materials. At the junction, electrons from the n-type region diffuse into the p-type region, filling holes and leaving behind positively charged donor ions. Similarly, holes from the p-type region diffuse into the n-type region, leaving behind negatively charged acceptor ions. This process creates a depletion region at the interface, devoid of free charge carriers.

The depletion region forms the active volume of the silicon detector. Applying a reverse bias voltage across the PN junction increases the width of the depletion region (W), enhancing the detector's ability to collect charge. The depletion width is governed by:

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_r V_{\text{eff}}}{e}\left(\frac{N_a + N_d}{N_a N_d}\right)}, \tag{2.1}$$

where ε_0 and ε_r are the permittivity constants, e is the elementary charge, N_a and N_d are the acceptors and donors doping concentrations, and V_{eff} is the effective voltage, given by $V_{\text{eff}} = V_{\text{bias}} + V_j$, with V_j being the built-in potential.

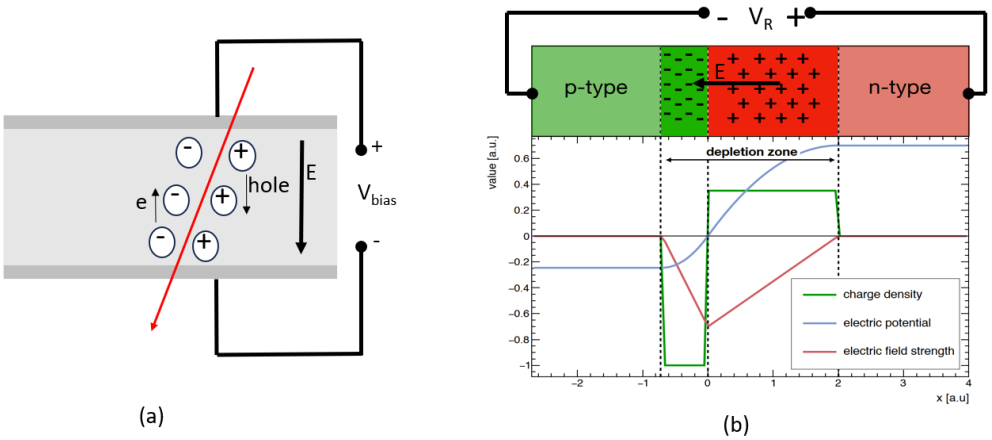


Figure 2.5: (a) charge generation principle at silicon detector. (b) A pn-junction wita depletion region, charge densities, an electric field and junction potential.

Charge Generation in the Depletion Region: When an incident particle traverses the depletion region, it generates electron-hole pairs proportional to the energy deposited. These charge carriers are quickly separated and collected by the electric field within the depletion region. The drift velocity of the carriers is given by $v = \mu E$, where μ is the carrier mobility and E is the electric field. At room temperature (300 K), the electron and hole mobilities in silicon are approximately $1350\,\mathrm{cm}^2/\mathrm{Vs}$ and $450\,\mathrm{cm}^2/\mathrm{Vs}$, respectively. Under high electric fields, carrier velocities saturate, ensuring rapid charge collection.

Radiation Damage in Silicon Sensors: Radiation exposure introduces defects into the silicon lattice, creating deep-level traps within the bandgap. These traps act as recombination centers, reducing charge collection efficiency (CCE) and increasing leakage current. The leakage current rises linearly with fluence (Φ_{eq}) and can be expressed as:

$$\Delta I = \alpha \Phi_{\mathrm{eq}} V, \tag{2.2}$$

Where α is the proportionality constant dependent on the material. Silicon's radiation tolerance is a critical consideration for high-radiation environments like the HL-LHC, necessitating optimized fabrication techniques and doping strategies [73].

Fabrication Techniques, FZ and EPI Processes: Silicon sensors for particle detectors are typically fabricated using two primary methods, with details available in [74–76]:

1. **Float-Zone (FZ) Process**: This method produces high-purity silicon by melting and recrystallizing a silicon rod in a zone refining process. FZ silicon is characterized by its low impurity concentration and high resistivity, making it suitable for thick sensors (e.g., 200 μm and 300 μm) used in low-to-moderate fluence regions.

2. **Epitaxial (EPI) Process**: In this method, a thin silicon layer is grown on a low-resistivity silicon substrate. EPI sensors are well-suited for high-fluence regions due to their superior radiation hardness. The thin active layer minimizes bulk damage, ensuring sustained performance in harsh environments.

2.4.1 Silicon sensors for HGCAL

The CMS collaboration selected silicon sensors for HGCAL due to their exceptional radiation tolerance and fast response. Fluence levels in the endcap, projected at $3000\,\mathrm{fb}^{-1}$, were assessed using FLUKA simulations, revealing fluence values ranging from 2×10^{14} to $10^{16}\,n_{\mathrm{eq}}/\mathrm{cm}^2$ (Figure 1.19). The radiation hardness of silicon, demonstrated in CMS Tracker Phase-II R&D [77, 78], was further validated by the HGCAL collaboration [15], ensuring reliable particle detection and precise energy measurements.

Hexagonal Sensor Design: The HGCAL utilizes planar DC-coupled hexagonal silicon sensors fabricated on 8-inch circular wafers. The hexagonal design, compared to square or rectangular alternatives, maximizes the utilization of wafer surface area, minimizes wastage, and reduces the overall number of sensors required, thereby decreasing costs [6].

Three Thicknesses for Optimized Performance: The silicon sensors are deployed in three thicknesses: 120 μm, 200 μm, and 300 μm, shown in figure 2.3 (left), tailored to the expected radiation levels across the detector volume. Thinner sensors are more robust against higher fluence and offer better charge collection efficiency (CCE) and reduced leakage current. Figure 2.6 (left) demonstrates that thinner sensors outperform thicker ones in high-fluence regions. Thus, the HGCAL employs thinner sensors in higher radiation regions while utilizing thicker sensors in areas with lower fluence to maximize the signal-to-noise ratio.

Why n-on-p DC-Coupled Sensors?: Extensive testing led to the selection of n-on-p silicon sensors for the HGCAL. Figure 2.6 (right) illustrates that n-on-p sensors exhibit superior CCE at high fluences

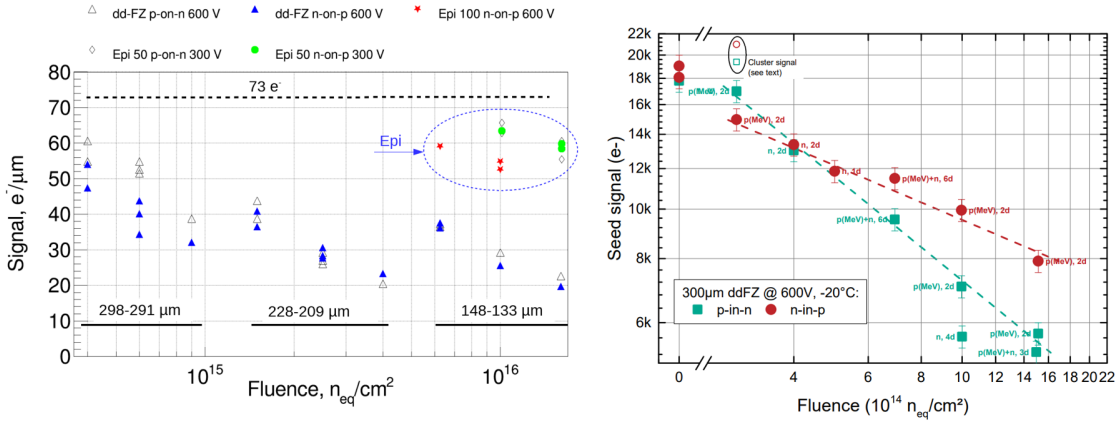


Figure 2.6: (Left) Signal ($e^-/\mu m$) measured from TCT (Transient Current Technique) tests for diodes at 600 V and 300 V in 50-μm epitaxial silicon [15]. (Right) Collected charge on a seed strip for sensors with 300-μm nominal thickness after short annealing (2–6 days) at room temperature. Error bars represent a 5% uncertainty, accounting for statistical and gain variations. Symbols denote irradiation types: 'p' for protons (MeV/GeV) and 'n' for neutrons, with annealing at 21°C [16].

compared to p-on-n sensors. The n-on-p configuration is preferred for its resistance to type inversion and enhanced charge collection under extreme radiation, ensuring reliable long-term performance [16].

Final Sensor Types: The HGCAL employs a variety of silicon sensors tailored to meet the requirements of different fluence regions. Table 2.2 summarizes the key specifications of the sensors.

High-Density (HD) sensors, featuring a thickness of 120 μm, 432 channels, and a compact pad size of 0.5 cm^2, are optimized for high-fluence regions (r<70 cm). In contrast, Low-Density (LD) sensors, with thicknesses of 200 μm and 300 μm, 192 channels, and larger pad sizes of 1.18 cm^2, are deployed in medium- and low-fluence areas. These designs ensure precise charge collection and efficient operation across varying radiation conditions.

Figure 2.7 illustrates all sensor configurations utilized in HGCAL. The top row displays the LD-Full (a) and HD-Full (b) sensors, which are hexagonal in shape and used for the majority of the detector coverage. The bottom row highlights the Multi-Geometry Sensors (MGS) for both LD (c) and HD (d) configurations. These MGS sensors are segmented using dicing lines to produce smaller, non-hexagonal shapes referred to as partial sensors. These partial sensors are specifically designed for the detector peripheries, optimizing coverage and reducing material wastage.

This comprehensive approach to silicon sensor deployment enables HGCAL to achieve high performance and cost efficiency, ensuring reliable operation in the challenging radiation environment of the HL-LHC.

d_{act} (μm)	Full-Size Channels	Pad Size (cm^2)	Φ_{neq} (cm^{-2})	TID (Gy)
120	432 (HD)	0.5	7.0×10^{15}	1×10^6
200	192 (LD)	1.18	2.5×10^{15}	2×10^5
300	192 (LD)	1.18	5.0×10^{14}	3×10^4

Table 2.2: Specifications of HGCAL silicon sensors, including active thickness (d_{act}), number of channels, pad size, maximum fluence (Φ_{neq}), and total ionizing dose (TID).

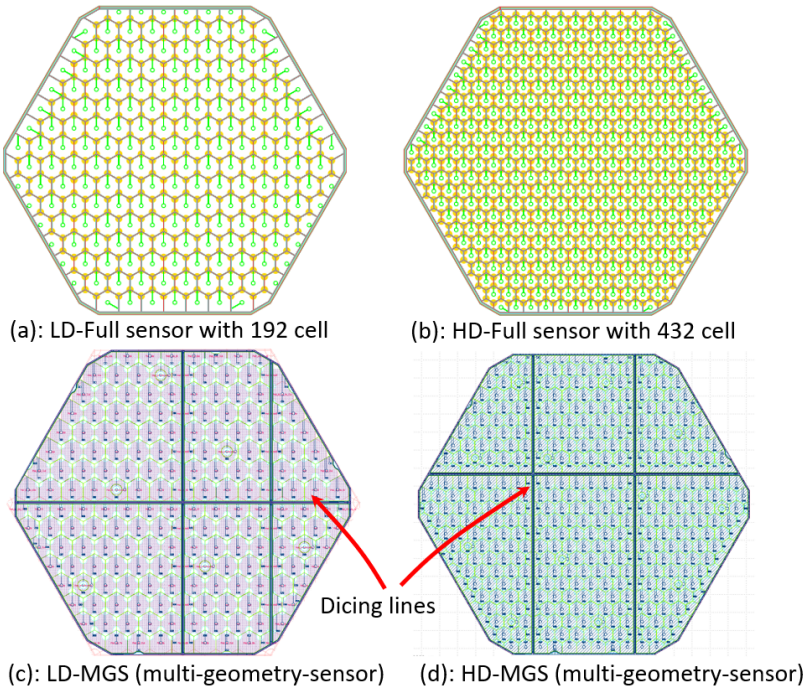


Figure 2.7: HGCAL sensors illustrating full and multi-geometry configurations. (a) LD-Full sensor with 192 cells, optimized for low-density regions. (b) HD-Full sensor with 432 cells, designed for high-density regions. (c) LD-MGS (multi-geometry sensor) and (d) HD-MGS, where dicing lines divide the hexagonal sensor into smaller, non-hexagonal shapes, referred to as partial sensors. These configurations enable efficient coverage and cost-effective fabrication.

2.5 High Granularity: longitudinal and lateral segmentation

The HGCAL introduces unprecedented longitudinal and lateral segmentation, offering significant capabilities for reconstructing physics objects. The 47-layer configuration, comprising 25 radiation lengths (X_0) and 10 interaction lengths, ensures complete containment of electromagnetic and hadronic showers. Each layer features cells with sizes ranging from 0.5 cm^2 to 1.18 cm^2 in the silicon regions and 4 cm^2 in the scintillator regions. These fine-granularity layers enable detailed shower and jet reconstruction and facilitate particle flow algorithms. Energy deposits in the calorimeter are matched with tracks in the tracker to trace particles back to their primary vertices, a critical feature for mitigating pile-up events at the HL-LHC.

Longitudinal segmentation: The strategic choice of 47 layers in HGCAL is guided by the need to maintain Higgs boson mass resolution in $H \to \gamma\gamma$ decays at a level comparable to Phase-I operations. Originally, the HGCAL design featured 50 layers, comprising 28 in the CE-E and 22 in the CE-H, corresponding to 25 X_0 and 10 interaction lengths. However, for cost optimization, three layers were removed (one double-sided layer, the final CE-E layer, and one CE-H layer). To maintain the required depth for full shower containment, the thickness of individual absorber layers was increased. This adjustment ensures robust longitudinal sampling, which is critical for accurate energy measurements and shower reconstruction.

Lateral segmentation: The lateral segmentation of the HGCAL is driven by several performance and operational considerations. Smaller cell sizes improve spatial resolution, allowing for precise energy

measurements and better separation of overlapping showers. However, finer segmentation increases the number of readout channels, leading to higher power consumption, increased cooling requirements, and greater bandwidth demands. Conversely, larger cell sizes reduce costs and complexity but can degrade performance.

The cell sizes in HGCAL are optimized to balance these trade-offs. Silicon pad sizes of 0.5 cm^2 to 1.18 cm^2 are chosen to accommodate the lateral spread of electromagnetic showers, which is characterized by a Moliere radius of approximately 3 cm. A mean cell size below this range ensures sufficient sampling for accurate energy measurements. Additionally, cell capacitance is kept within manageable limits to control electronic noise, enabling the detection of MIP signals for inter-cell calibration. Figure 2.8 illustrates the containment radii (68% and 90%) of energy deposited by photon showers in silicon layers.

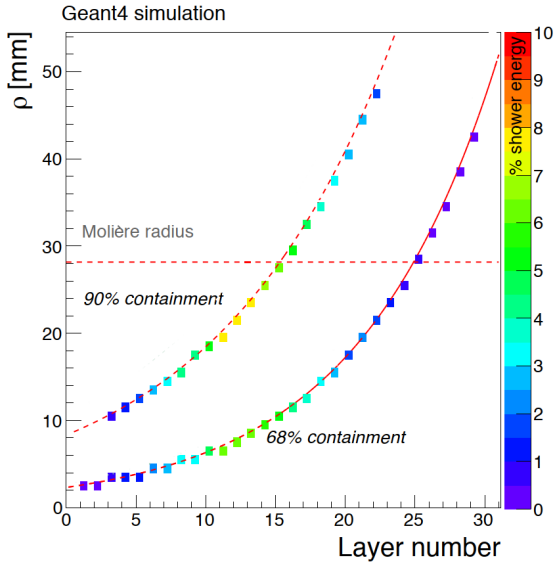


Figure 2.8: Radii, ρ, containing 68% and 90% of the energy deposited in an individual silicon layer by a photon shower, as a function of the silicon layer. The color-coded rectangles indicate the fraction of total energy deposited inside the 68% and 90% containment radii of each layer.

The combined longitudinal and lateral segmentation of the HGCAL enables precise reconstruction of physics objects and shower shapes. The 47-layer design balances performance and cost while ensuring complete containment of electromagnetic and hadronic showers. The optimized lateral cell sizes enhance spatial resolution and energy measurement accuracy while keeping system complexity manageable. These design choices make HGCAL a powerful tool for advanced physics analyses at the HL-LHC.

2.6 Modular build-up: Layer, Cassettes and Silicon Hex-Modules

The HGCAL has adopted a modular design, where each of the 47 layers consists of cassettes instrumented with silicon Hex-Modules (or a combination of silicon and tile modules), as shown in figure 2.4. The details are given below:

Layers: The CE-E includes 26 silicon-only layers (13 double-sided), spanning approximately 41 cm in thickness, equivalent to 26 X_0 and 1.7 λ. This ensures effective containment of electromagnetic showers. The CE-H comprises 21 layers with a total thickness of 10.7 λ, designed for full containment of hadronic

showers. The first seven layers (27–33) are silicon-only, while the remaining 14 layers (34–47) are mixed, incorporating scintillator tiles in the outer regions. Two layers, a silicon only layer from CE-E and a mix layer from CE-H is shown in figure 2.3.

Cassettes: Each layer is further divided into modular cassettes to facilitate assembly and integration processes. In the CE-E region, each layer is segmented into six cassettes, covering 60° sectors of the detector as shown in figure 2.4 (middle). In the CE-H region, due to the larger diameter, each layer is divided into 12 cassettes, covering 30° sectors. The cassettes are equipped with silicon Hex-Modules in high-radiation regions and scintillator tiles in lower-radiation areas. This modular design ensures efficient assembly, cost-effectiveness, and adaptability to varying geometric constraints.

Silicon Hex-Modules:

The silicon Hex-Module (usually known by silicon module or Hex-Modue) is the fundamental unit of the HGCAL silicon region. Approximately 28,000 modules, encompassing 11 variants, are used to equip the CE-E region and high-fluence areas of the CE-H region. These modules are designed to withstand fluences ranging from 2×10^{14} to 10^{16}neq/cm^2. A silicon Hex-Module is a glued assembly of a thermally conductive base plate, a Kapton^{TM}-laminated copper foil, a silicon sensor, and an eight-layer hexagonal PCB known as the Hexaboard, as shown in figure 2.9 (left). The base plate in the CE-E region is fabricated from a CuW (75:25) alloy to enhance radiation length, while the CE-H region utilizes cost-effective carbon-fiber or recently Titanium chosen, to provide similar thermal and mechanical properties. The Kapton foil ensures electrical insulation and serves as a noise shield for the silicon sensor.

The bonding scheme for the silicon Hex-Module is depicted in figure 2.9 (right). Silicon sensors are securely bonded to the Hexaboard via stepped holes to maintain reliable connections while avoiding obstructions for additional connecting components. The bias voltage (BV) is bonded to the backplane of the sensor through a notch in the base plate, ensuring efficient operation. Following the sensor types shown in figure 2.7, the silicon Hex-Modules are available in two primary types: High-Density (HD) modules with pad sizes of 0.51 cm^2, and Low-Density (LD) modules with pad sizes of 1.18 cm^2. To ensure optimal coverage, the modules include 11 variants, comprising both full and partial modules. Partial modules are used to cover the peripheries of the detector.

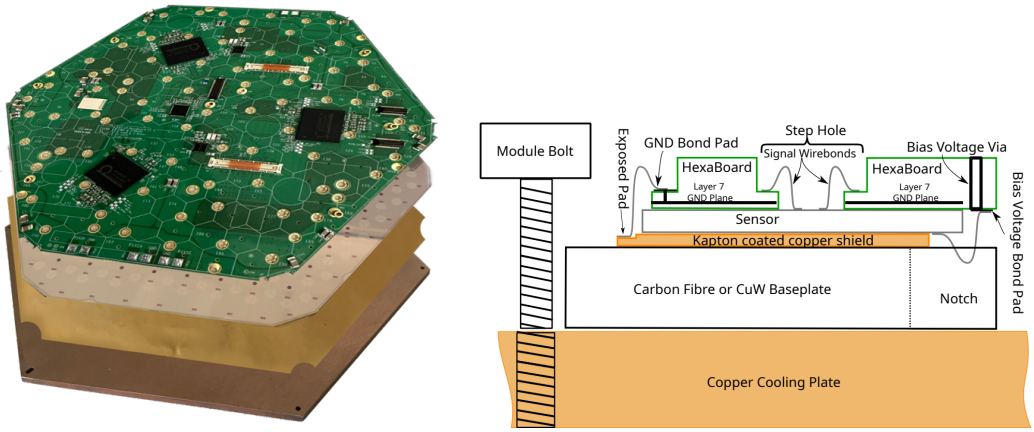


Figure 2.9: (Left) Exploded view of a silicon Hex-Module: showing the glued assembly of the base plate, Kapton foil, silicon sensor, and Hexaboard. (Righ) Block diagram depicting the bonding scheme, including BV connections and Kapton shielding.

2.7 Physics goals with the upgraded Endcap Calorimeter

The High Granularity Calorimeter (HGCAL) enhances the CMS detector's capability in high-luminosity conditions, providing fine spatial and timing resolution. Its unprecedented transverse and longitudinal segmentation improves the reconstruction of physics objects, facilitating precision measurements. The following examples, based on HGCAL TDR [6], illustrate key performance aspects.

2.7.1 Lepton and Photon reconstruction

Electrons and photons are reconstructed by correlating energy deposits in the calorimeter with charged tracks from the tracker. The HGCAL significantly enhances photon reconstruction, particularly in the forward region of the CMS. Figure 2.10 presents the fractional energy resolution and mass resolution of photon pairs in simulated high-luminosity conditions.

The left panel of Figure 2.10 shows the fractional energy resolution (σ/E) as a function of transverse momentum (p_T) for unconverted photons at three pseudorapidity values: $\eta = 1.7$ (300 µm Si), $\eta = 2.0$ (200 µm Si), and $\eta = 2.4$ (100 µm Si). A summing radius of 2.6 cm is applied in the reconstruction. The results indicate that HGCAL maintains robust performance under an average pileup of 200 interactions per bunch crossing.

The right panel illustrates the reconstructed invariant mass of photon pairs from Higgs boson decays ($H \to \gamma\gamma$), where both photons are detected in the endcap region. The simulation assumes a pileup of 200 events per bunch crossing and excludes pre-calorimeter photon conversions. The measured mass resolution, $\sigma_M/M = 1.61 \pm 0.02\%$, corresponds to approximately 2 GeV, affirming the high precision of HGCAL in Higgs boson measurements at the HL-LHC.

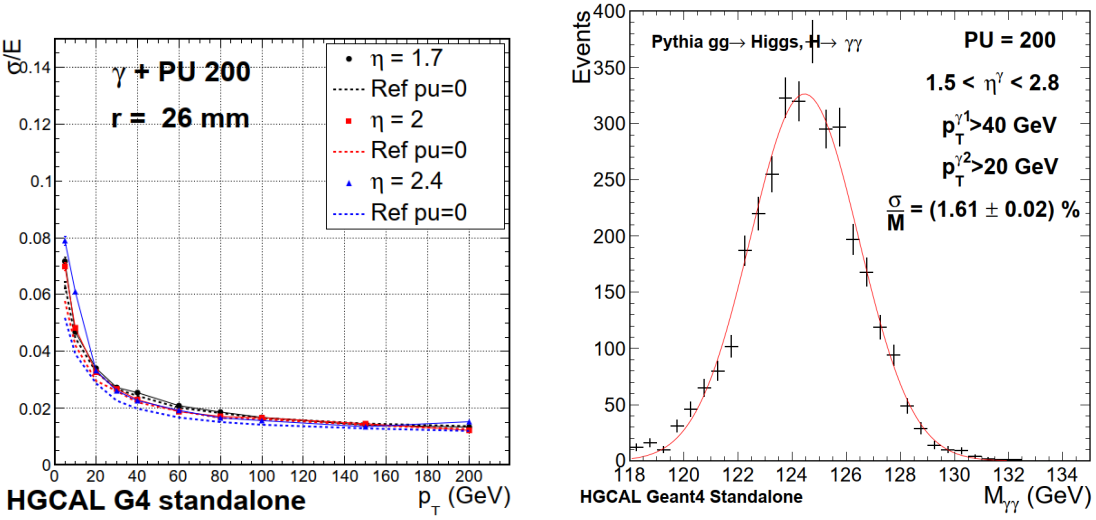


Figure 2.10: (Left) Fractional energy resolution (σ/E) as a function of p_T for unconverted photons at $|\eta| = 1.7$ (300 µm Si), $|\eta| = 2.0$ (200 µm Si), and $|\eta| = 2.4$ (100 µm Si) using a 2.6 cm summing radius. (Right) Reconstructed invariant mass of photon pairs from $H \to \gamma\gamma$ decay with an average pileup of 200 interactions per bunch crossing. Both plots emphasize the capability of HGCAL to perform in challenging high-luminosity environments, adopted from HGCAL TDR [6].

2.8 Relative positioning of HGCAL among LHC Calorimeter systems

The CMS High Granularity Calorimeter (HGCAL) has been developed to meet the extreme performance requirements imposed by HL-LHC operations: average pileup of 200 collisions per bunch crossing, radiation doses exceeding 200 Mrad in the endcaps, and the need for 4D reconstruction to suppress pileup and improve object identification. This section compares HGCAL against representative LHC calorimeters, with a focus on the following five performance parameters, aligned with the benchmarking methodology outlined in internal correspondence [79]:

- **Energy Resolution**: Both stochastic and constant terms.
- **Transverse Granularity**: Size of readout cells in the transverse plane.
- **Longitudinal Granularity**: Number of sampling layers.
- **Timing Capability**: Intrinsic timing resolution of EM layers.
- **Radiation Hardness**: Resistance to ionizing and non-ionizing damage.

Unless otherwise stated, the comparative values in this section are extracted from the official technical design reports (TDRs) of CMS [6, 80], ATLAS [81], LHCb [41], and ALICE [82], and consolidated with internal CMS knowledge and private technical exchanges [79].

Calorimeter Technologies at a Glance

Each LHC experiment employs a distinct calorimeter architecture optimized for its physics goals and experimental layout:

- **CMS ECAL/HCAL**: Employs $PbWO_4$ crystals (ECAL) with excellent energy resolution and brass–scintillator tiles (HCAL) for hadronic measurements. ECAL is compact, fast, but sensitive to radiation damage.
- **ATLAS LAr**: Uses ionization in liquid argon between copper or lead absorbers. It provides good radiation hardness and longitudinal segmentation, though cryogenic operation and slower pulse shaping limit timing resolution.
- **LHCb Shashlik**: Based on a sandwich of scintillator and lead plates, read out via wavelength-shifting (WLS) fibers. Offers simple, low-cost construction but suffers radiation-induced degradation in high-rate environments.
- **ALICE FoCal**: A forward electromagnetic calorimeter prototype using high-resolution silicon pads and Monolithic Active Pixel Sensors (MAPS) pixels. Designed for precision spatial granularity in low-pileup, low-radiation heavy-ion conditions.

Energy Resolution

HGCAL has a relatively high stochastic term of approximately $22\%/\sqrt{E}$, compared to $3\%/\sqrt{E}$ for CMS ECAL ($PbWO_4$), $10\%/\sqrt{E}$ for ATLAS LAr, and LHCb Shashlik. However, in the forward region where energy deposits are large, the constant term dominates. HGCAL targets $\sim$0.3%, comparable to CMS barrel ECAL (0.3%) and ATLAS LAr (0.2%). LHCb has observed in situ degradation to $\sim$3% due to upstream material and fiber aging.

Transverse and Longitudinal Granularity

HGCAL offers the highest transverse segmentation among all LHC calorimeters, with 0.5 cm^2 silicon pads. CMS ECAL cells range from 5–10 cm^2, ATLAS LAr typically uses 2–3 cm bins in η, and Shashlik modules in LHCb are significantly coarser.

Longitudinally, HGCAL employs 47 sampling layers, enabling detailed shower profiling and improved angular reconstruction. In contrast, CMS ECAL and LHCb have no longitudinal segmentation, and ATLAS LAr offers three EM layers including a presampler.

Timing Performance

HGCAL aims for a timing resolution of 20–30 ps in high-charge regions. Beam tests have demonstrated a performance of approximately 40 ps, while the laser setup (see Section 6.6.6) has measured values around 30–35 ps, though this result currently applies to only three channels. The upgraded CMS ECAL (Phase-2) targets $\sim$30 ps timing in the barrel. ATLAS LAr is slower due to signal shaping and cryogenic drift times. LHCb's Shashlik design claims potential 20 ps precision through dual-end WLS fiber readout, but this remains to be proven in operational settings.

Radiation Tolerance and Thermal Operation

HGCAL sensors are designed for $>$ 200 Mrad dose and $10^{16}\,n_{eq}/cm^2$, with passive cooling at $-30°C$ ensuring stability. CMS ECAL endcaps degrade due to radiation-induced loss of transparency in $PbWO_4$ crystals. ATLAS LAr is intrinsically radiation hard, but requires cryogenics at 87 K. LHCb's Shashlik has poor radiation tolerance; WLS fibers and scintillators degrade significantly in high-fluence regions, prompting plans for crystal fiber replacements at low radii.

Hadronic Calorimetry Context

HGCAL CE-H has similar hadronic resolution to the current CMS HCAL ($\sim 90\%/\sqrt{E} \oplus 5\%$), but with improved granularity and radiation resistance in the inner silicon layers. In contrast, the ATLAS TileCal achieves better resolution ($\sim 52\%/\sqrt{E} \oplus 3\%$), owing to higher sampling fraction, though lacking fine spatial or timing granularity.

Table 2.3: Comparison of HGCAL with representative calorimeter technologies at the LHC.

Parameter	CMS HGCAL	CMS ECAL/HCAL	ATLAS LAr	LHCb Shashlik	ALICE FoCal
Active Medium	Si + Scintillator	$PbWO_4$ + Scintillator	Liquid Argon	Scintillator + WLS Fibers	Si (MAPS + Pads)
Timing Resolution	20–50 ps	$\sim$30 ps (Phase-2)	—	$\sim$20 ps (claimed)	Not a design goal
Energy Resolution (EM)	$22\%/\sqrt{E} \oplus 0.3\%$	$3\%/\sqrt{E} \oplus 0.3\%$	$10\%/\sqrt{E} \oplus 0.2\%$	$10\%/\sqrt{E} \oplus 0.8\%$	$\lesssim$3% (test beam)
Longitudinal Layers	47	1 (ECAL), 17 (HCAL)	3 (EM)	None	18 (2 pixel + 16 pad)
Transverse Granularity	0.5 – 1 cm^2	5–10 cm^2	2–3 cm (η)	$\sim$25 mm^2	$\sim$1 mm^2
Radiation Hardness	$>$200 Mrad	$\sim$10 krad (ECAL)	Very High	Low (upgrade planned)	Low–Moderate
Cryogenics	No ($-30°C$ passive)	No	Yes (87 K)	No	No

Summary: While legacy LHC calorimeters deliver excellent intrinsic electromagnetic energy resolution, the CMS HGCAL sets a new benchmark in granularity, radiation tolerance, and precision timing. These attributes are critical for effective 4D event reconstruction and pileup mitigation in the HL-LHC environment. A comparative overview of these performance aspects across representative LHC calorimeter systems is presented in Table 2.3.

2.9 Conclusion

The HGCAL represents one of the main upgrades to the CMS detector for phase-II operation, for meeting the unprecedented challenges posed by the HL-LHC. This chapter has highlighted the motivation for replacing the existing endcap calorimeters, underscoring the critical need for precision and resilience under extreme radiation and pileup conditions.

The HGCAL's 47-layer architecture integrates fine longitudinal and lateral segmentation, complemented by advanced timing capabilities and a modular design. The adoption of silicon sensors in varying thicknesses ensures high performance in regions of intense radiation, while the hybrid use of scintillator tiles in lower-radiation zones optimizes cost-effectiveness. The use of absorber materials such as copper-tungsten and stainless steel enhances the detector's efficiency for both electromagnetic and hadronic shower containment.

A key feature of the HGCAL is its precision timing capability, enabling robust pileup mitigation and vertex identification, valuable for reconstructing physics processes. Combined with its granular spatial resolution, the HGCAL delivers unmatched accuracy in energy, position, and time measurements, ensuring that the CMS detector maintains its sensitivity for Higgs boson studies and beyond.

This chapter has provided a foundation for understanding HGCAL's innovative design and its important role in the HL-LHC physics program. The next chapter will explore the electronics and readout systems, with a particular focus on the HGCROC readout chip.

Chapter 3

The Front-End Electronics System of the HGCAL

3.1 Introduction

The HGCAL electronics system is meticulously crafted to address the demanding data acquisition and processing needs of the CMS detector at the HL-LHC. At the heart of this system lies the HGCROC (High-Granularity Calorimeter Readout Chip), the primary readout ASIC hosted on the hexaboard. This chapter focuses on the HGCROC, its functionality, and its integration within the HGCAL framework, while also providing insights into other critical components that ensure the seamless operation of the data path.

This chapter begins with an overview of the front-end electronics (FE) chain corresponding to the Low-Density (LD) region, as detailed in Section 3.2. Section 3.3 introduces the HGCROC application-specific integrated circuit (ASIC), outlining its role within the CMS HGCAL readout architecture. A comprehensive description of the HGCROC readout channel is presented in Section 3.4, covering the sequence of signal processing stages including the charge-sensitive preamplifier, shaping amplifier, analog-to-digital converter (ADC), and time-to-digital converters (TDCs) for both time-of-arrival (TOA) and time-over-threshold (TOT) measurements. The corresponding data flow for digitised output is also described. In addition, the section highlights the packaging design of the HGCROC, underscoring its relevance for thermal management, signal integrity, and mechanical integration on the Hexaboard.

Beyond the HGCROC, this chapter introduces additional components essential to the HGCAL data path. The ECONs (Concentrators), detailed in Section 3.5, perform critical tasks of data compression, aggregation, and bandwidth optimization before transmitting processed data to the back-end systems. Similarly, the lpGBT (Low-Power Gigabit Transceiver), discussed in Section 3.8, enables high-speed data transmission between the front-end and back-end systems, completing the data path architecture.

To support the HGCROC and ensure synchronisation and power stability, two additional ASICs hosted on the hexaboard are examined. The Rafael Clock Fanout Chip, described in Section 3.6, distributes high-precision clock and control signals across the front-end electronics. The Low-Dropout Voltage Regulator (LDO), discussed in Section 3.7, is a custom radiation-hardened component designed to deliver stable and efficient power to the HGCAL electronics, even in the harsh radiation environment of the detector.

By systematically exploring the HGCROC as the central component of the hexaboard, along with supporting ASICs and key modules in the data path, this chapter provides a comprehensive understanding

of the HGCAL electronics system's design, functionality, and integration.

3.2 Front-end electronics system overview

The front-end (FE) electronics system is designed to meet the stringent data acquisition and processing requirements of the HGCAL in the HL-LHC. Figure 3.1 provides a detailed overview of the HGCAL front-end electronics chain for the low-density region. The Hexaboard, which serves as the primary readout board, hosts the HGCROC, Rafael, and LDO application-specific integrated circuits (ASICs). At the core of the system is the HGCROC ASIC, specifically designed for the HGCAL. This radiation-resistant ASIC is responsible for reading the charge generated by particles impacting the silicon sensors and determining the arrival time of particles that exceed a predefined threshold of 12 fC, as specified in the Technical Design Report (TDR) [6].

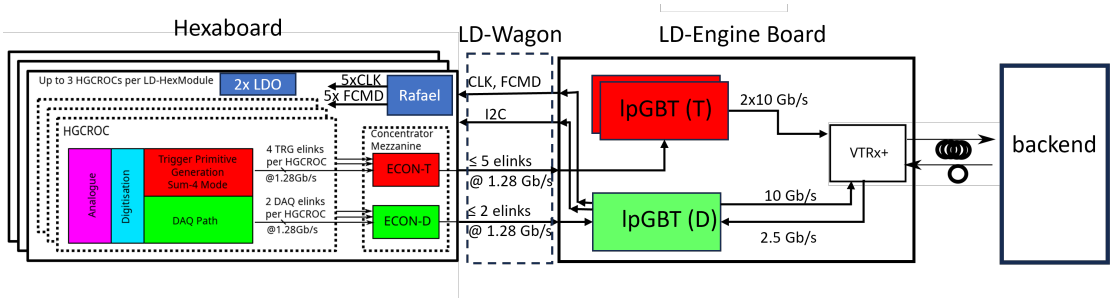


Figure 3.1: HGCAL front-end electronics chain for the low-density region: This diagram provides an overview of the key ASICs and boards used in the front-end electronics system. The Hexaboard hosts the HGCROC, Rafael, and LDO ASICs, serving as the primary readout board. The ECON-D and ECON-T concentrators are integrated into the Concentrator Mezzanine board, while the lpGBT and VTRX+ are assembled on the Engine board, which manages both on- and off-detector communication and control. The Wagon board acts as an interface, connecting multiple Hexaboards to the Engine board.

After the HGCROC processes the charge and timing information, the data is transmitted to the ECON-D and ECON-T concentrators. These concentrators play an essential role in data reduction by applying zero-suppression techniques to eliminate redundant information. The processed data is then sent to the lpGBT (Low-Power Gigabit Transceiver), which transmits it over high-speed electrical lines at a rate of 1.28 Gbps.

The lpGBT forwards the processed data to the VTRX+, an optical transceiver designed for high-bandwidth data transmission at 10 Gbps. The VTRX+ ensures reliable communication with the control room located at the back end via optical uplinks. Additionally, the lpGBT, through the VTRX+, receives clock signals, fast control, and slow control information from the back end via a 2.56 Gbps downlink and distributes them across the front-end electronics.

This integrated front-end electronics system ensures robust and efficient data handling, enabling the HGCAL to meet the demanding operational requirements of the HL-LHC.

3.3 HGCROC, the front-end readout ASICS for HGCAL

The HGCROC is the readout ASIC integrated into the front-end readout boards, referred to as Hexaboards. It is available in two specialized variants, tailored to read data from two distinct sensor types:

silicon sensors and silicon photomultipliers (Si-PMs).

The stringent design specifications for HGCROC are shown in table 3.1 and are driven by the Phase-II operational conditions, such as the high radiation level and large pileup. To cope with these challenges, it must be radiation-hardened and should handle up to 200 Mrad absorbed Dose and a 1 MeV neutron equivalent fluence of 10^{16} n_{eq} cm^{-2}.

Requirement	Specification
Dynamic range	0.2 fC to 10 pC (equivalent to 16 bits)
Noise	0.4 fC
Radiation tolerance	200 Mrad, 10^{16} n_{eq} cm^{-2}
Power consumption	20 mW per channel
Pileup Mitigation	Fast shaping (peak $<$ 25 ns), precise timing capability (25 ps)
Linearity	Better than 1% over the full range
Timing Precision	Better than 100 ps for pulses above $\approx$ 12 fC
Shaping Time	Peaking-time $\leq$ 20 ns
On-Detector Digitization and Data Processing	Included for zero suppression, linearization, and summing of trigger data
Latency	$\leq$ 36 bunch crossings for trigger primitives at the output of the detector
Buffering	To accommodate the 12.5μ s latency of the L1 trigger
High-Speed Readout Links	Interface with 10 Gb/s low power GBT (lpGBT) serializer

Table 3.1: The target design specifications of the HGCROC are taken from TDR [6].

As this ASIC is for calorimetric purposes, the design should support a very wide dynamic range, capable of measuring charges from 0.2 fC to as high as 10 pC in the silicon region. For the Si-PM-based version, this capability is further extended to manage up to 300 pC while maintaining a noise threshold below 0.4 fC, equivalent to around 2500 electrons at 65 pF detector capacitance.

The chip design requires a fast shaping time with a peak time of less than 25 ns to handle out-of-time events effectively. It is designed to ensure that the residual signal contribution to the next bunch crossing remains below 20%. The chip features precise timing capabilities, with binning intervals of 25 ps. This enables a timing precision of approximately 100 ps for charges around 10 fC and improves to less than 25 ps for charges near 100 fC or higher [27, 83].

Figure 3.2 provides an overview of the HGCROC-V3b architecture, showcasing its FE readout block and dual-path design for trigger generation and data acquisition. This finalized version of the HGCROC, as presented in this thesis, features 78 analog channels categorized into three types: 72 channels for reading charge and Time-of-arrival (TOA) information from the silicon sensors, 2 calibration channels designed for low noise and connected to smaller cells for MIP calibration throughout the detector's life-time, and 4 common mode (CM) channels to monitor and subtract noise caused by variations in bias voltag.

Every channel consists of a low-noise, charge-sensitive preamplifier (see section 3.4.1). The HGCAL will use silicon sensors in three different thicknesses 300 µm, 200 µm and 120 µm, and MIP signal produces different amounts of charges ($\sim$ 74 electrons hole pair per micron thickness); therefore, the gain is to be adjusted so that the MIP produces a measurement of 10 ADC counts. In the preamplifier's linear range, the signal is read by the 10-bit Successive Approximation Register Analog-to-Digital Converter (SAR-ADC) (see section 3.4.3) via the shaper (see section 3.4.2), which enhances the signal-to-noise ratio. Over the preamplifier saturation, the charge measurement is conducted using a discriminator connected to a 12-bit Time-to-Digital Converter (TDC) (see section 3.4.5). The TDC measures the

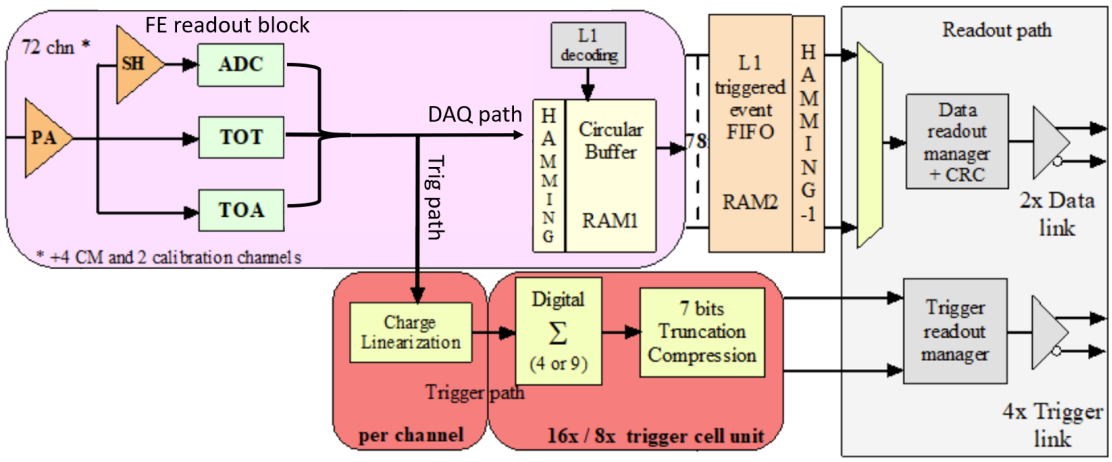


Figure 3.2: HGCROC-V3b simplified block diagram: The diagram illustrates the FE readout block and the dual-path architecture of the HGCROC. The trigger path processes charge data by linearizing, summing over 4 or 9 channels, and compressing it into a 7-bit format, transmitted via four trigger links for each bunch crossing (Bx). The DAQ path temporarily stores data in a circular buffer (RAM1) to handle L1A trigger latency before transferring selected events to FIFO (RAM2) for transmission via two DAQ links. The main figure is adapted from [17], with minor modifications to illustrate the concept of the Trigger and Data Acquisition (DAQ) path.

Time-over-Threshold (TOT) with a binning of 50 ps, allowing for a measurement range of up to 200 ns. Another discriminator associated with an additional 10-bit TDC accurately determines the TOA with a binning resolution of 25 ps.

The HGCROC processes charge and timing information for each bunch crossing (BX) at a frequency of 40 MHz, with data being read through ADC, TOT, and TOA measurements. The information is managed via two distinct paths: the trigger path and the DAQ path. In the trigger path, the ADC and TOT data from each BX are processed through a charge linearization unit, where the charge is linearized. Subsequently, the sum of charges from 4 or 9 contiguous channels is calculated to generate a trigger primitive. This data is then compressed into a 7-bit format using logarithmic and mantissa encoding and transmitted via four 1.28 Gbps links for each BX (operating at 40 MHz). This trigger data contributes to the Level-1 Accept (L1A) decision, which determines if a BX contains useful information for further analysis. The L1A decision, made by the CMS Level-1 trigger system, can take up to 12.5 microseconds. To accommodate this decision delay, the DAQ path temporarily stores data in a circular RAM buffer with 512 memory locations, each capable of holding 32 bits. Upon receiving an L1A command, the relevant data is transferred from the buffer (RAM1) to a FIFO (RAM2). From there, the data is transmitted through two 1.28 Gbps DAQ links at the L1 trigger rate for further processing. This dual-path architecture ensures both real-time trigger generation and efficient data acquisition, enabling the HGCAL to meet the stringent requirements of the HL-LHC.

The I2C protocol is used to configure more than 7900 parameters of the HGCROC. The Fast Command block takes a 320 MHz clock and a fast control command as input and configures HGCROC in different operation modes like link synchronization, reset, calibration and L1A request etc.

A 40 MHz clock, extracted from the 320 MHz fast command link, is phase-locked to the LHC clock to ensure synchronization. This clock is distributed to the digital sections of the HGCROC, as well as the Phase-Locked Loop (PLL). The PLL generates the additional clocks required for the chip's operation: a 640 MHz clock for the 1.28 Gbps links, an adjustable-phase 40 MHz clock for the ADCs, and a 160 MHz

clock for the TDCs.

The chip features a symmetrical design, with identical components replicated across its two halves. Apart from the 1.28 Gbps links, I2C, fast command, and PLL blocks, all other elements, such as 39 analog channels, bias circuits, reference voltages, a bandgap, data storage, and trigger sum calculator circuitry, are mirrored in both halves to ensure balanced and reliable performance [26, 27, 83].

3.4 Internal structure of a single channel

A single analog channel of the HGCROC consists of several key components, as illustrated in figure 3.3. These include a preamplifier, a shaper, a 10-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC), and two discriminators, each paired with TDCs of 12-bit and 10-bit resolutions, respectively.

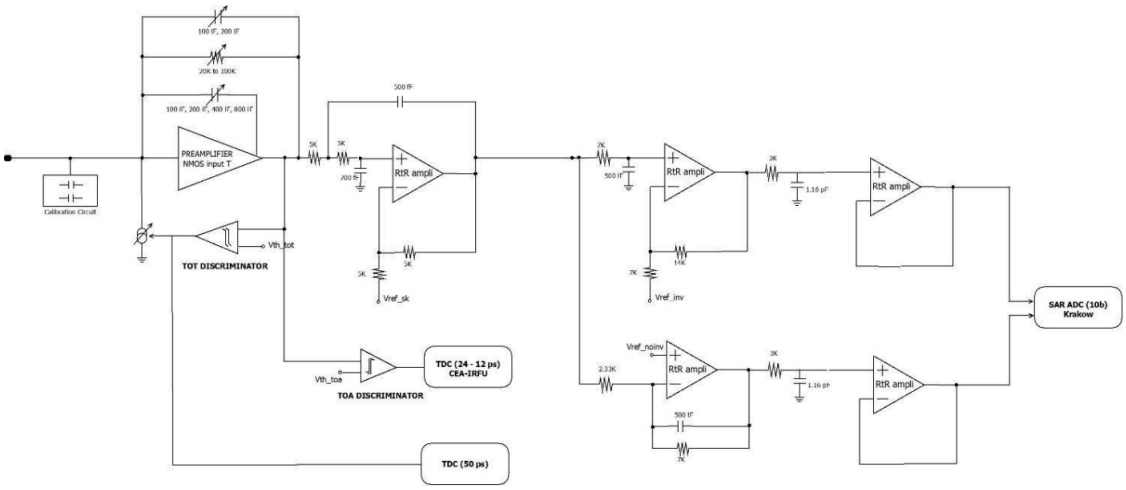


Figure 3.3: Schematic of a single HGCROC analog channel. Adapted from [18], the diagram shows the preamplifier, shaper, 10-bit SAR ADC for charge readout, and two discriminators, each paired with a TDC of 12-bit and 10-bit resolution for TOT and TOA measurements, respectively.

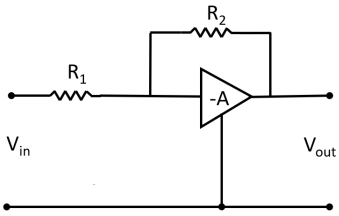
3.4.1 Preamplifier

The preamplifier is the first reading circuitry element coupled with the silicon detector to convert the input charge coming from the silicon diode to an output voltage. The preamplifier provides the first amplification of the signal with the best noise performance and forwards it to the shaper or discriminators for further processing. The preamplifier has mainly two types: *voltage-sensitive preamplifiers* and *charge-sensitive preamplifiers*. The former is shown by a simplified block diagram in figure 3.4 (a) and is used for scenarios where the detector capacitor 'C' is fixed and the input voltage 'V_{in}' is proportional to the charge 'Q' deposited in the detector as shown by equation 3.1, and the output voltage V_{out} is proportional to the input voltage and represented by equation 3.2.

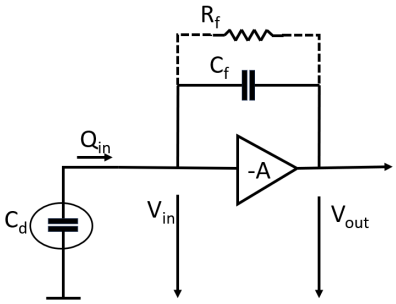
$$V_{in}(max) = \frac{Q}{C}. \tag{3.1}$$

$$\text{Assuming thr open loop gain } A \gg R_2/R_1$$
$$V_{\text{out}} \cong -\frac{R_2}{R_1} V_{\text{in}} \,. \tag{3.2}$$

In semiconductor devices, the detector capacitance is dependent on operating parameters like the depletion level of the diode, and usually, the signal generated by incident particles is very weak compared to the scintillator or GM (Geiger–Müller) tube [84]. Then, the second type, *Charge Sensitive preamplifier (CSA)* is recommended, where the feedback capacitor C_f is used to integrate charge from the sensor and the output voltage is independent of the detector capacitance [19]. A simplified block diagram is shown in figure 3.4 (b). For high-resolution applications and the detector to be operated at low temperatures like HGCAL, the *DC coupling* method is recommended as it's reduced the stray capacitance in the input circuitry, enhances the signal-to-noise ratio and provides an option to measure the leakage current at the output of preamplifier [85].



(a) Voltage Sensitive Preamplifier



(b) Charge Sensitive Preamplifier

Figure 3.4: A basic model of the voltage-sensitive preamplifier (a) and charge-sensitive preamplifier with detector capacitance C_d and feedback components C_f and R_f (b) are shown and adopted from [19].

The detailed derivation for the gain of the charge-sensitive preamplifier is explained in [73]. For the inverting amplifier, the configuration is shown in figure 3.4 (b), the voltage gain is given by

$$dV_{out}/dV_{in} = -A \Rightarrow V_{out} = -AV_{in}, \tag{3.3}$$

where "V_{in}" is the input voltage, "V_{out}" is the output voltage, and "A" is the open-loop gain of the amplifier. Assuming the input impedance is $= \infty$, i.e., no signal current flows into the amplifier input, so the voltage across the feedback capacitor C_f is the voltage difference of V_{in} and V_{out}, given by

$$V_f = V_{in} - V_{out} \Rightarrow V_f = (A+1)V_{in}. \tag{3.4}$$

And "Q_f" the charge deposited on the feedback capacitor C_f is

$$Q_f = C_f V_f = C_f(A+1)V_{in}. \tag{3.5}$$

$$Q_{in} = Q_f \quad \text{(since } Z_i = \text{ infinite, then } Q_{in} \text{ input charge remain same as } Q_f) \,. \tag{3.6}$$

The effective input capacitance, known as *dynamic input capacitance*, is given by the following equation 3.7:

$$C_{in} = \frac{Q_{in}}{V_{in}} = C_f(A+1). \tag{3.7}$$

The gain of the ideal charge-sensitive preamplifier is given by equation 3.8:

$$A_Q = \frac{dV_{out}}{dQ_{in}} = \frac{A \cdot v_{in}}{C_{in} \cdot v_{in}} = \frac{A}{C_{in}} = \frac{A}{A+1} \cdot \frac{1}{C_f} \approx \frac{1}{C_f} \quad (A \gg> 1). \tag{3.8}$$

The total charge Q_s generated by the detector is split between the detector capacitance C_d and input capacitance C_{in}. The input charge Q_{in} flows into C_{in}, while the remaining charge Q_d flows into C_d. The relationship is:

$$Q_s = Q_{in} + Q_d. \tag{3.9}$$

The voltage across C_{in} and C_d is the same since they are connected in parallel; therefore

$$V_{in} = \frac{Q_{in}}{C_{in}} = \frac{Q_d}{C_d} \Rightarrow Q_d = Q_{in} \cdot \frac{C_d}{C_{in}}. \tag{3.10}$$

Substitute Q_d into 3.9 :

$$Q_s = Q_{in} + Q_{in} \cdot \frac{C_d}{C_{in}} = Q_{in}\left(1 + \frac{C_d}{C_{in}}\right). \tag{3.11}$$

The fraction of the input charge 'Q_{in}', flowing into the preamplifier to the total charge 'Q_s' generated in the detector with capacitance C_d, is given below.

$$\frac{Q_{in}}{Q_s} = \frac{1}{1 + \frac{C_d}{C_{in}}} \approx 1 \quad (\text{if } C_{in} \gg C_{\text{d}}). \tag{3.12}$$

The above equation 3.12 recommends that the dynamic input capacitance C_{in} » C_{det}, to have all generated charges integrated by C_f.

The HGCROC uses a charge-sensitive preamplifier, dc-coupled to a silicon sensor. The gain, as shown by equation 3.8, has an inverse proportion to the feedback capacitance 'C_f' . The feedback resistor R_f contributes to the shaping of the output pulse as its product with C_f decides the time constant for the circuit. By modifying the feedback resistance and capacitors, the amplifier's gain and time constant can be adjusted. The available values of feedback components for the silicon version of the HGCROC are listed in Table 3.2. The feedback capacitor is divided into two components, namely Cf and Cf_{comp}. The gain of the preamplifier is determined by the combination of both capacitors and the feedback resistance. The Cf_{comp} is connected in a modified manner to enhance the stability of the preamplifier. The arrangement of the feedback resistor and capacitors is tuned such that the product of R_f' and C_f' remains constant, resulting in a signal with consistent duration throughout the data-taking process. Figure 3.5 illustrates the simulation results of the preamplifier, showcasing various gains while keeping the $Rf \times Cf$ product constant.

The preamplifier has two outputs:

1. *Outpa* is linked to the shaper and TOT discriminator with a DC operating point ranging from 160 to 200mV.

2. $OutCf_{pa}$ is linked to the TOA discriminator, and the DC operating point is around $'Outpa' + Vgs$, which is roughly 500mV.

The whole dynamic range can be read in three different stages:

1. A linear stage, the preamplifier's output is directly proportionate to the input charge, this goes till 300 mV.

$R_f(\Omega)$	25 K, 50 K, 66.66 K, 100 K	In parallel, these resistors provide 15 values to be adjusted with the C_f and Cf_{comp} values to get a decay time constant around 10 ns.
C_f (fF)	50, 100, 200, 400	Combined with the Cf_{comp} capacitors, provide the gain of the preamplifier.
Cf_{comp} (fF)	100, 200	Same purpose as Cf capacitors, but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with C_f capacitors.

Table 3.2: Different combinations of C_f, Cf_{comp}, and R_f for different gain settings of HGCROC, taken from HGCROC's datasheet [18].

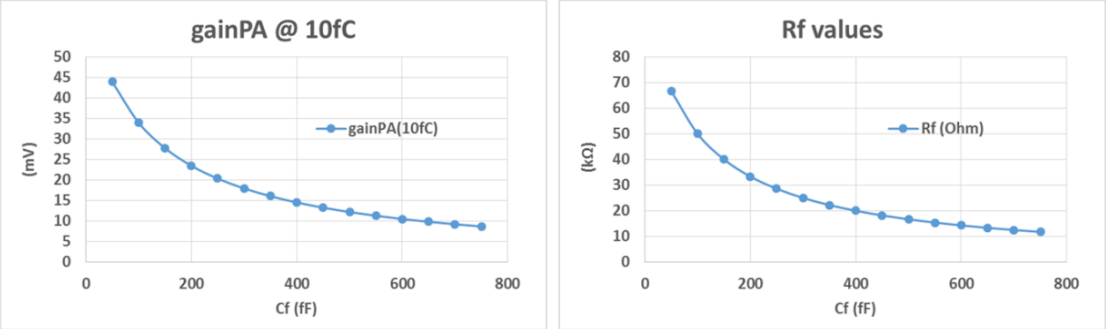


Figure 3.5: Gain and feedback resistance as functions of feedback capacitance (C_f): The left plot shows the preamplifier gain (gainPA) at an input charge of 10 fC, demonstrating a decrease in gain as C_f increases. The right plot illustrates the feedback resistance (R_f) values relations with the feedback capacitance C_f, adopted from HGCROC's datasheet [18].

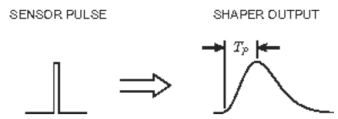
2. A non-linear stage, where the preamplifier is not-linear, but not yet saturated and it goes till 600 mV.

3. Saturated Mode, where an increase in input charge does not increase the amplitude of the output pulse, instead, the pulse gets wider and wider, at this point, the charge measurement is controlled by *the Time over threshold* mechanism.

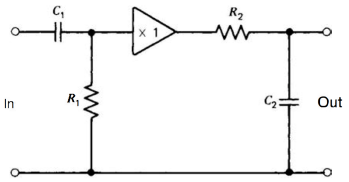
3.4.2 Shaper

The shaper circuit is used for enhancing the signal-to-noise ratio. The output from the preamplifier is a time-varying pulse, and by analyzing its Fourier transform, the frequency spectrum can be used to distinguish the signal from noise. A filter designed to select specific frequency bands of interest improves the signal-to-noise ratio. This process, which also modifies the time-domain response and alters the shape of the pulse, is referred to as pulse shaping [73]. Figure 3.6 (a) illustrates this process, where a sharp pulse broadens after being processed by the shaper.

Figure 3.6 (b) shows a *CRRC* (Capacitor-Resistor-Resistor-Capacitor) shaping network, which consists of multiple components: a *CR stage* (differentiator circuit) acting as a high-pass filter to eliminate high-frequency noise, followed by an *RC stage* (integrator circuit) functioning as a low-pass filter to suppress low-frequency noise. In practice, the CR stage is often combined with several RC stages to form a higher-order CRRC network, typically referred to as CRRC^n. For practical applications, four RC stages



(a) A sharp pulse processed by a shaper.



(b) A CRRC shaping network.

Figure 3.6: (a) illustrates a sharp current pulse and its processed output with peaking time T_p. (b) represents a CRRC shaping network.

($n = 4$) are sufficient to produce an output pulse with a Gaussian shape [19]. The time required for the shaped pulse to reach its peak amplitude, known as the peaking time, is given by $T_p = n\tau$, where n represents the n^{th} order and τ is the time constant of the shaping network, determined by the RC values in each stage. The output response E_{Out} of the CRRC^n circuit at instant time t to an input pulse E is expressed as:

$$E_{\text{Out}} = \frac{E}{n!}\left(\frac{t}{\tau}\right)^n e^{-t/\tau}. \tag{3.13}$$

In the HGCROC, the shaper design consists of three stages: a Sallen-Key filter, an RC^2 filter, and a unity gain buffer to drive the ADC. This fourth-order RC shaper typically exhibits a peaking time of approximately 23 ns. The shaping time can be adjusted by ±20% to account for process variations, ensuring that out-of-time pileup remains below 20%. The primary goal of the shaper is to optimize the signal-to-noise ratio across the full dynamic range (approximately 1 V) while minimizing pulse overlap between consecutive bunch crossings. To achieve this, the pulse must decay sufficiently so that its tail does not exceed 20% of the next bunch crossing. The ideal shaping time, maintained in the range of 20 to 25 ns, is closely tied to the preamplifier feedback, which governs both gain and decay time. As shown in figure 3.7, the preamplifier and shaper outputs for an input charge of 10 fC illustrate how the two-bit RC shape register adjusts different peaking times.

The inverting and non-inverting shapers provide flexibility for handling signals with differing polarities, ensuring compatibility with various sensor configurations. Their global DC threshold levels are controlled using 10-bit DACs (`inv_vref` and `noinv_vref`) to configure the ADC pedestal levels. To further enhance uniformity and minimize channel-to-channel dispersion, a 6-bit DAC is employed for per-channel fine adjustments.

The differential outputs of the inverting and non-inverting shapers (SH-noinv − SH-inv) are then digitized by a per-channel 10-bit ADC.

3.4.3 Analog-to-Digital Converter (ADC)

The ADC (Analog-to-Digital Converter), is a key component used to convert analog signals, characterized by their continuous-time and continuous-amplitude nature, into discrete-time and discrete-amplitude digital data. This conversion process is required to make the analog signals suitable for further processing within digital systems. There are various types of ADCs, a few of which are listed below and their detail description can be found in references [86–89]:

- **Flash ADC**: Known for its high-speed operation, the Flash ADC employs a bank of comparators to determine the input voltage range and produce a corresponding digital output. It is primarily used in applications requiring very high-speed conversions but at the cost of high power consumption.

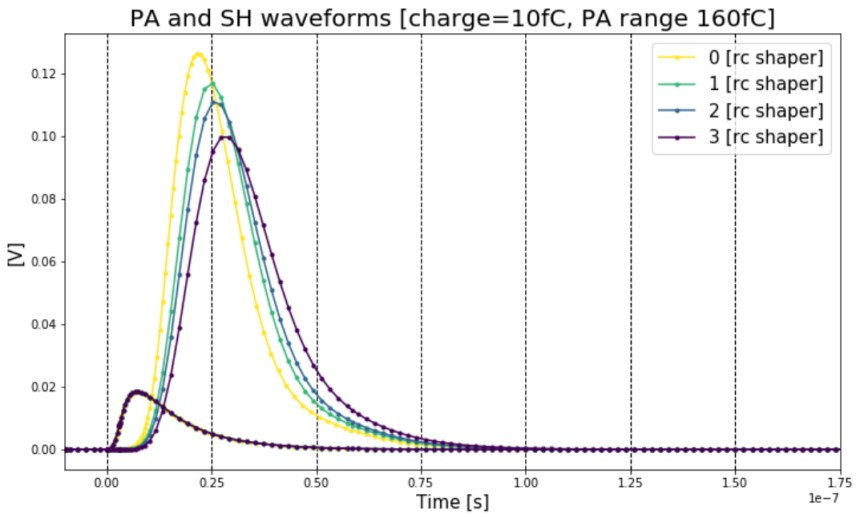


Figure 3.7: Preamplifier and shaper output pulses for a 10 fC input at a typical ADC gain range of 160 fC. Different colors represent different peaking time configurations set by the two-bit RC shape register, adopted from HGCROC's datasheet [18].

- **Sigma-Delta ADC**: This type of ADC utilizes oversampling and noise shaping techniques to achieve high resolution over a narrow bandwidth, making it ideal for audio and precision instrumentation applications.

- **Pipeline ADC**: By dividing the conversion process into multiple stages, the Pipeline ADC handles portions of the signal sequentially. It offers a balance between speed and resolution, making it suitable for medium-to-high-speed applications.

- **Successive Approximation Register (SAR) ADC**: The SAR ADC employs a binary search algorithm to approximate the input voltage step-by-step. It is recognized for its high resolution, low power consumption, and moderate speed, making it well-suited for energy-constrained and high-density systems.

Selection of SAR ADC for HGCAL

In the HGCAL, where millions of readout channels must operate within stringent power budgets, the SAR ADC stands out as the optimal choice. Figure 3.8 compares the energy efficiency (P/Sampling Rate in pJ/Hz) and Effective Number of Bits (ENOB) for various ADC architectures, including SAR, Flash, Pipeline, and Sigma-Delta ADCs. The plot highlights that SAR ADCs occupy the most power-efficient region for 8–10-bit resolutions, outperforming other architectures in balancing power efficiency and resolution [20, 90, 91].

This efficiency is particularly important for HGCAL, where the power budget per channel is limited to approximately 20 mW as specified in the design requirements [6]. SAR ADCs provide high resolution, linearity, and accuracy while minimizing power consumption, making them the ideal choice for this high-density system.

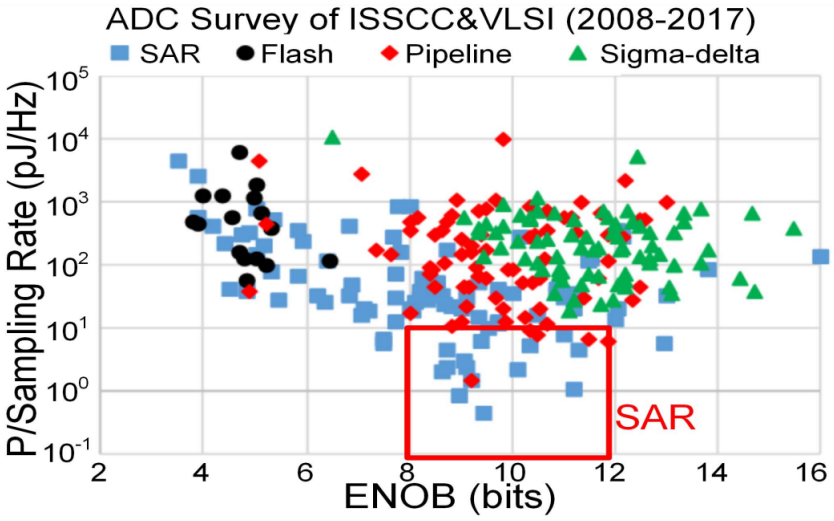


Figure 3.8: Energy efficiency (P/Sampling Rate) versus Effective Number of Bits (ENOB) comparison of ADC architectures, including SAR, Flash, Pipeline, and Sigma-Delta ADCs. SAR ADCs demonstrate superior energy efficiency in the 8–10-bit resolution range [20].

SAR ADC architecture in HGCROC

The HGCROC integrates a 10-bit SAR ADC designed with ultra-low and frequency-scalable power consumption, developed by AGH in Krakow [21]. This ADC is tailored for high-performance data acquisition in multi-channel readout systems. Its compact design, with a pitch of 146 µm and an area of 0.088 mm^2, makes it ideal for the dense channel layout of the HGCAL.

The basic architecture of the SAR ADC is illustrated in figure 3.9, with additional functional details available in references [21] and [92]. The architecture consists of three primary components:

1. **Track-and-Hold Circuit**: This stage samples the input signal (V_{in}) and holds it constant during the conversion process. Bootstrapped switches are employed to ensure precise sampling and minimize distortions caused by variations in the input signal.

2. **Digital-to-Analog Converter (DAC)**: The DAC generates an analog output voltage (V_{DAC}) corresponding to the current digital approximation of the input voltage. The HGCROC's DAC utilizes a binary-weighted capacitor array, which efficiently performs charge redistribution and reference voltage generation. The DAC output voltage is calculated using Equation 3.14:

$$V_{\text{DAC}}^{i} = \begin{cases} 0 & \text{for } i = 0, \\ \frac{V_{\text{ref}}}{2^{N-1}-1} \cdot \sum_{k=1}^{i} (2 \cdot D_{N-k} - 1) \cdot 2^{N-1-k} & \text{for } 0 < i < N-1. \end{cases} \tag{3.14}$$

   where N is the resolution (10 bits for the HGCROC ADC), i is the comparison step index, and D_{N-1-i} is the comparator output at the i^{th} step.

3. **Dynamic Comparator**: This component compares V_{in} with V_{DAC} at each step, determining whether the input voltage is higher or lower. The comparator output guides the SAR logic, which adjusts the DAC for the next approximation. The process iterates for 10 cycles, resolving one bit per cycle.

The SAR ADC's asynchronous and dynamic control logic optimizes speed and power efficiency. Its performance is evaluated through static metrics like Integral Non-Linearity (INL) and Differential

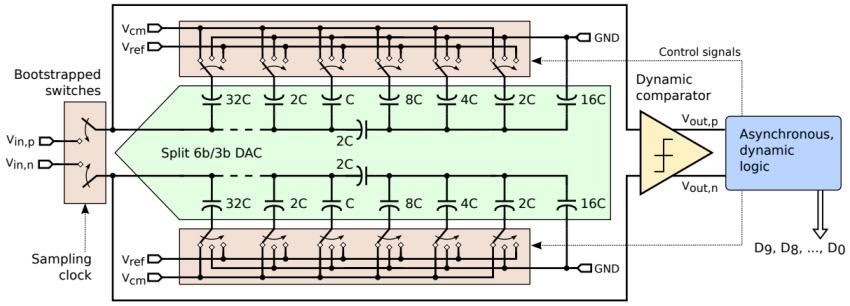


Figure 3.9: Block diagram of the 10-bit SAR ADC architecture implemented in the HGCROC. It includes bootstrapped switches for signal sampling, a binary-weighted capacitor DAC, a dynamic comparator, and asynchronous control logic for efficient signal conversion [21].

Non-Linearity (DNL), both approximately 0.5 least significant bit (LSB), and dynamic metrics such as Signal-to-Noise and Distortion Ratio (SINAD) and Effective Number of Bits (ENOB). Equations 3.15 and 3.16 define these parameters:

$$\mathrm{SINAD}_{\mathrm{idcal}}(\mathrm{dB}) = 10\log_{10}\left(\frac{P_S}{N_q}\right) = 6.02\cdot N + 1.76\,(\mathrm{dB}). \tag{3.15}$$

$$\mathrm{ENOB} = \frac{\mathrm{SINAD}_{\mathrm{real}} - 1.76}{6.02}. \tag{3.16}$$

The HGCROC SAR ADC achieves SINAD values of ∼58 dB and ENOB values ranging from 9.2 to 9.35 for dynamic signals, improving to 9.42–9.5 for DC signals. The ADC supports a scalable sampling frequency from 10 kHz to 40 MHz, with linear power consumption scaling at 22 μW/MS/s. The power efficiency of the ADC is evaluated using the figure of merit (FoM), which is defined in Equation 3.17 and illustrated in figure 3.10. The FoM provides a quantitative measure of the ADC's efficiency by correlating power consumption with resolution and sampling frequency [21, 90].

$$\mathrm{FoM} = \frac{\mathrm{Power}}{2^{\frac{\mathrm{SINAD}-1.76}{6.02}}\cdot f_{\mathrm{sample}}}. \tag{3.17}$$

Figure 3.10 depicts the relationship between FoM and sampling frequency for the HGCROC SAR ADC. The recorded FoM values, ranging from 33 to 50 fJ per conversion step, underline the ADC's ability to balance power efficiency and resolution effectively. The figure demonstrates that the ADC maintains stable efficiency at lower sampling frequencies, with a slight increase in FoM observed as the sampling frequency nears 40 MHz. This trend highlights the ADC's capability to deliver reliable performance even at higher operating frequencies, aligning with the stringent power constraints of the HGCAL system.

3.4.4 Descriminators

The discriminators are electronic circuits used to convert the analog pulse information to a digital signal. It is a comparator that compares the input signal amplitude at one of its input ports to a voltage threshold set on the other input port. If the input signal amplitude is greater than a certain threshold, the discriminator responds by issuing a standard 'High' logic signal, otherwise, the output is false or zero. It can be considered a one-bit ADC. Some main features of a discriminator are:

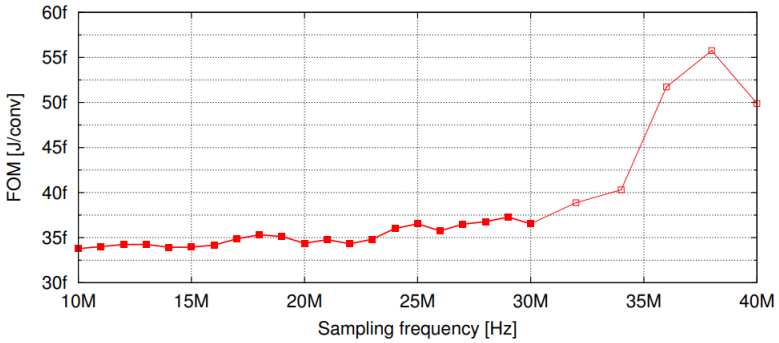


Figure 3.10: Power efficiency versus sampling frequency for the 10-bit SAR ADC implemented in HGCROC [21]. The figure illustrates the relationship between the figure of merit (FoM), measured in femtojoules per conversion (fJ/conversion), and sampling frequency, ranging from 10 MHz to 40 MHz. The SAR ADC demonstrates consistent power efficiency at lower sampling frequencies, with a gradual increase in FoM observed as the frequency approaches 40 MHz, underscoring its capability to sustain energy-efficient operation across a wide frequency range.

- *Sensitivity*: The lowest signal that a discriminator can detect, mainly depends on the circuit noise level.
- *Delay*: The time delay between the input signal and discriminator output.
- *Speed*: the highest frequency of the input signal for which a discriminator can response.
- *Jitter*: The time fluctuation in the threshold crossing, which mainly depends on incoming pulse amplitude.
- *Dual-pulse resolution*: The minimum time between two incoming signals that can be resolved.

In the HGCROC, each channel is equipped with two discriminators as shown in figure 3.3, serving distinct purposes: one measures the TOT, while the other determines the TOA. The TOT discriminator is connected to the preamplifier's output *Outpa*, which has a DC operating point ranging between 160 and 200 mV, as detailed in the section 3.4.1. Conversely, the TOA discriminator is linked to the preamplifier's secondary output, $OutCf_{pa}$, whose DC operating point is approximately $Outpa + V_{gs}$, typically around 500 mV.

The thresholds for the TOT and TOA discriminators are controlled by two global 10-bit DACs: `Tot_vref` and `Toa_vref`, each offering a resolution of 0.25 mV per LSB. To address channel-to-channel variations and improve uniformity, two local 5-bit trimming DACs, Trim_dac_tot and Trim_dac_toa, are employed, with a resolution of 1 mV per LSB. These trimming DACs ensure precise adjustments for individual channels, reducing per-channel dispersion.

The thresholds for the discriminators are configured using the following equations, as derived from the HGCROC datasheet [18]:

$$\text{Toa\_threshold} = \text{Toa\_vref} < 9:0 > - \text{Trim\_dac\_toa} < 4:0 >, \tag{3.18}$$

$$\text{Tot\_threshold} = \text{Tot\_vref} < 9:0 > - \text{Trim\_dac\_tot} < 4:0 > . \tag{3.19}$$

This architecture enables precise and independent control of the TOT and TOA thresholds, critical for optimizing the performance of each channel in the HGCROC system.

3.4.5 Time to digital converters (TDCs), TOT, and TOA

The HGCROC employs two specialized *Time to Digital Converters* (TDCs) to digitize the timing data from the discriminators. These TDCs, developed by the CEA IRFU group at Saclay, operate on the principle of amplifying time residuals. The TDC architecture is divided into three main blocks, as illustrated in figure 3.11:

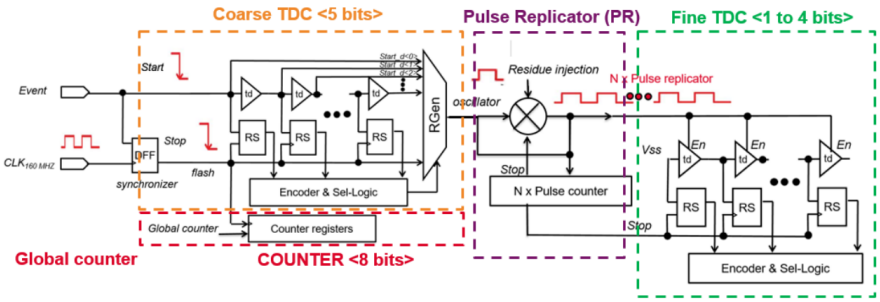


Figure 3.11: Block diagram of the three-stage TDC architecture in HGCROC. A 8 bits global counter clocked at 160 MHz provides two Msbs for timing of each channels. The 5-bit CTDC starts with a discriminator event ('Start') and stops at the next rising edge ('Stop'). The Pulse Replicator refines the measurement, and the 3 bits FTDC provides sub-cycle timing precision (taken from datasheet [18]).

1. An 8-bit global Gray counter, which determines the two most significant bits (MSBs) shared across all channels.
2. A 5-bit Coarse TDC (CTDC), responsible for the middle portion of the measurement.
3. A 3-bit Fine TDC (FTDC), which encodes the least significant bits (LSBs).

The Gray counter operates with a 160 MHz clock derived from the PLL. Its 2-bit resolution covers one bunch crossing (25 ns) in four clock ticks. The CTDC is equipped with 32 delay lines (CDL) that split the 160 MHz clock period into 32 intervals of 195 ps, extracting pulse residues that are further expanded into a series of pulses using a Pulse Replicator (PR). An in-channel discriminator within the CTDC locks the phase of the STOP signal to the 40 MHz reference clock.

For higher precision, a Time Amplifier (TA) is employed to amplify the interval between the hit and the next CDL step by a factor of 8 or 16, depending on the required resolution. This amplified interval is encoded into three bits by the FTDC. The outputs from the Gray counter, CTDC, and FTDC are combined into a digital block, producing TDC data with up to 11-bit resolution (12.5 ps) or 10-bit resolution (24.4 ps). Figure 3.12 illustrates the working principle of TOA and TOT TDCs.

Time of Arrival (TOA) TDC

The Time of Arrival (TOA) TDC in HGCROC measures the arrival time of signals exceeding a predefined threshold (12 fC, as specified in the TDR [6]). When the TOA discriminator detects an event, it generates a START signal. This signal halts the propagation in the CTDC's 5-bit delay lines upon the next rising edge of the 160 MHz clock, as depicted in figure 3.12. To enhance precision, the FTDC further resolves the timing by measuring the fine interval ΔT, encoding it into three bits. The combined thermometer codes from the CTDC and FTDC are then converted into binary format for digital processing. TOA data is temporarily stored in the on-chip RAM for further analysis but does not contribute directly to the Level-1 trigger decision.

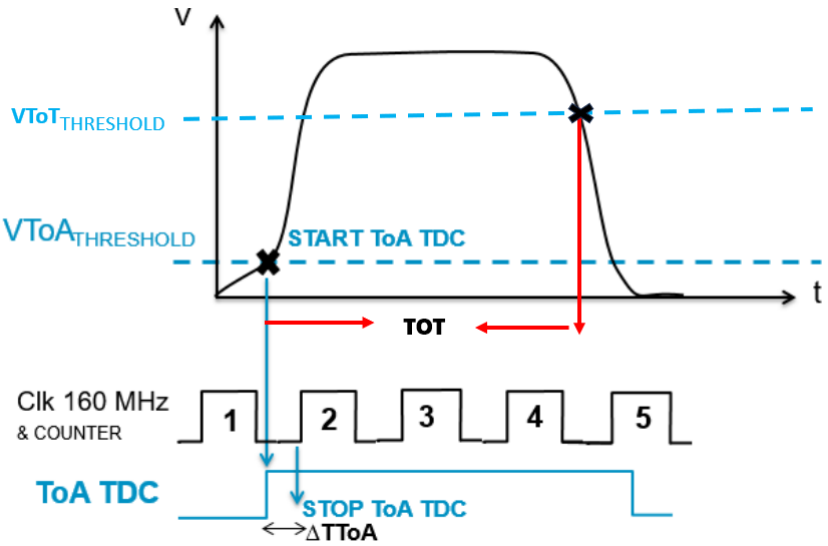


Figure 3.12: Detailed illustration of TOA and TOT TDC principles. The TOA measurement is initiated when the TOA discriminator triggers upon the rising edge of the signal crossing the V_{TOA} threshold. This initial timing is captured by the 5-bit Coarse TDC (CTDC), which measures the interval up to the next rising edge of the 160 MHz clock. For enhanced resolution, the timing is further refined by the 3 bits FTDC. Concurrently, the TOT measurement starts and stops when the signal's falling edge crosses the V_{TOT} threshold. The TOT duration is calculated as the difference between the TOT and TOA measurements, (taken from datasheet [18]).

Time Over Threshold (TOT) TDC

When the preamplifier saturates, the amplitude of the output pulse ceases to maintain linearity with respect to the input charge. Under these conditions, the charge information is extracted from the pulse width by exploiting the timing characteristics of the signal. The TOT TDC is specifically designed to measure the pulse width of such saturated signals, thereby providing information about the deposited charge.

The measurement process is initiated by the TOA trigger, which marks the *START* time. A dedicated TDC measures the duration between the rising edge (*START*) and the falling edge (*STOP*) of the signal, as detected by the TOT discriminator. This process is illustrated in figure 3.12, ensuring precise timing and charge extraction even under preamplifier saturation.

The TOT duration is derived by subtracting the TOA TDC measurement from the TOT TDC measurement.The calculated TOT values are stored in the on-chip RAM, remaining valid for a single 40 MHz clock cycle. For non-TOT events, the corresponding memory address is populated with a zero code, ensuring unambiguous differentiation in the recorded data.

Master DLL and channel calibration

The HGCROC features two MASTER DLL (Delay Lock Loop) blocks, one for each half of the chip. Each MASTER DLL calibrates its respective 36-channel group to ensure precise timing synchronization and uniformity. Calibration occurs in three stages:

1. Adjusting the primary DLL reference voltage to stabilize the timing reference.
2. Fine-tuning the CTDC for coarse timing adjustments.

3. Calibrating the FTDC for precise timing resolution.

This hierarchical calibration process ensures reliable and accurate time measurements across all channels, a critical requirement for HGCAL operations [93].

Specifications of TOA and TOT TDCs

The specifications for the TOA and TOT TDCs are summarized in Table 3.3, highlighting their resolution, range, power consumption, and other critical parameters.

Specifications	TOA TDC	TOT TDC
Resolution	∼25 ps RMS	<50 ps RMS
Range	10 bits over 25 ns	12 bits over 2–200 ns
Conversion Rate	>40 MHz (bunch clock)	...
Power Consumption	<2 mW/channel	<2 mW/channel
Min. Time Between Hits	25 ns	200 ns
Area	Pitch: 120 µm	Pitch: 120 µm
Technology	TSMC 130 nm	TSMC 130 nm
Temperature Range	−30°C	−30°C
Fixed Latency	...	12 bunch crossings

Table 3.3: Specifications of TOA and TOT TDCs from the HGCROC datasheet [18].

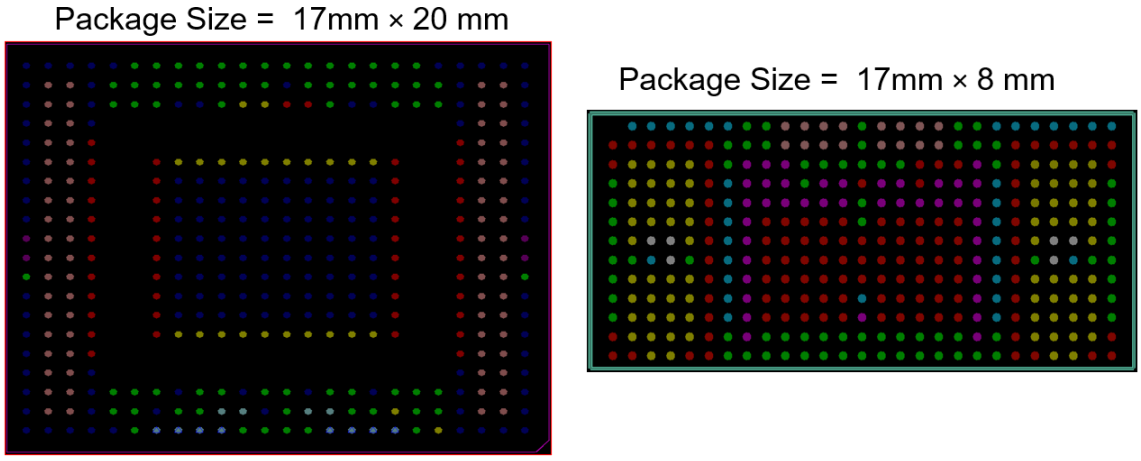
3.4.6 HGCROC packaging

The HGCROC packaging employs advanced bonding techniques to improve power distribution and mitigate noise and cross-talk. Unlike conventional wire-bonded approaches, the HGCROC connects the silicon die to the Ball Grid Array (BGA) package via C4 (controlled collapse chip connection) bumps [94]. The transition from traditional wire-bonding to Flip Chip C4 bump bonding, significantly reduced the coherent noise fraction from 80% in earlier wire-bonded packages to 10% in the BGA configuration and as low as 5% in Flip-Chip BGA packaging [83]. Two distinct BGA packaging configurations have been developed, as shown in figure 3.13:

1. *Low-Density Package*: The Low-Density (LD) substrate, measuring 20 mm × 16.8 mm with 376 bumps, incorporates a 0.8 mm BGA pitch. This configuration is specifically designed for low-density Hexaboards, facilitating the readout of LD silicon sensors having a cell size of 1.1 cm^2. The LD package accounts for approximately 80% of total Hexaboard production, ensuring cost efficiency and streamlined manufacturing processes.

2. *High-Density Package*: The High-Density (HD) substrate, measuring 17 mm × 8 mm with 345 bumps, utilizes a 0.6 mm BGA pitch. This package is optimized for high-density Hexaboards, supporting the readout of the HD silicon sensors with a cell size of 0.5 cm^2.

The design of the packaging is governed by several critical parameters, including the pin count, fan-out, and pitch dimensions, all of which directly impact the printed circuit board (PCB) technology. The Low-Density (LD) package, which dominates Hexaboard production, incorporates a relaxed pitch design to expedite manufacturing while maintaining sufficient electrical performance. This approach ensures high yields and cost-efficiency for large-scale production, aligning with the requirements of the CMS HGCAL upgrade.



(a) LD package BGA with 0.8mm pitch (b) HD package BGA with 0.8mm pitch

Figure 3.13: (a) Low-Density HGCROC package with a 0.8 mm BGA pitch, primarily used for LD Hexaboards. (b) High-Density HGCROC package with a 0.6 mm BGA pitch, utilized in HD Hexaboards for high-fluence regions.

3.4.7 Data paths and data formats

After the FE readout block, the charge (ADC and TOT) and TOA data has two paths: DAQ path and TRIG paths. Details are below:

DAQ data path

The ADC and TDCs outputs are fed into the Latency manager block, which delays the ADC output by fixed delay (ADC+ Align_buffer delay = 13*Bx*) to align with the TDCs value, as the TOT TDC could be busy in conversion for up to 200 ns to measure charges up to $\sim$ 10 pC. The TOT-encoding block compresses the 12-bit TOT to 10 bits to have equal numbers of bits as ADC and TOA. This information is continuously buffered into 512 positions of deep circular buffer memory '*RAM1*' and waits for "L1 A command" that comes from the CMS Level 1 Trigger after analyzing the relevant Trigger data.

For each channel, including both normal and calibration channels, the data is formatted into 32-bit words. The content of the 30 bits is determined by the charge amount and the threshold crossed, as outlined in Table 3.4. This framing ensures that all relevant information about the event is compactly organized for efficient processing. The "Characterization" mode is used primarily for debugging purposes. In this mode, all ADC, TOA, and TOT data for the same event are buffered in RAM1. The two MSBs are reserved for critical flags: *tp* and *tc* which are used for data packet validation. The *tp* flag indicates 'TOT in progress,' signaling that ADC value can be corrupted. The *tc* flag signifies that the TOT process is completed, marking the end of the pulse measurement and ensuring that the second 10 bits in the data frame are TOT data not ADC. These flags play important role for data integrity and its implementation ensures that no critical timing or charge information is lost during acquisition.

The ADC data for the DAQ path is without pedestal subtraction. The common mode channels only provide ADC data. The Latency Manager includes both the align buffer and a portion of TDC digital processing, which together contribute to the functioning of the DAQ path. These synchronized ADC, TOA, and TOT information are sent onto RAM1 using a phase-adjustable 40 MHz clock.

Table 3.5 and figure 3.14 show the details contents for DAQ frame. There are two DAQ links, one for

	ADC (BX-1)	ADC (BX)	TOT (BX)	TOA (BX)	Charge collection	Data type
1	x	x		x(= 0)	Q < TOA_th	Normal
2	x	x		x	Q < TOT_th	Normal
3	x		x	x	Q > TOT_th	Normal
4		x	x	x		Characterization

Table 3.4: DAQ word contents based on TOA and TOT thresholds. An 'x' in the table indicates that the corresponding field is included in the frame. When the charge is below the TOA threshold, the frame includes ADC (BX-1), ADC (BX), and TOA (BX) with TOA = 0. When the TOA threshold is crossed but the TOT threshold is not, the frame includes ADC (BX-1), ADC (BX), and TOA (BX). When the TOT threshold is exceeded, the frame consists of ADC (BX-1), TOT (BX), and TOA (BX). In characterization mode, all ADC, TOT, and TOA values are included in the frame.

# DAQ link	2 (no sharing, 1 per side)
Idle word	4 b header +28 bits configurable by SC (Slow control, I2C)
# 32b-word send by single L1	39 + 1 CRC-32
# of Idle packet after each & frame »	1
Bits order	MSB first
Word (W) order / half chip	1w with header / counters 1w with $2 \times CM$ 18w with channels 0 to 17 1w Calib 18w with channels 18 to 35 1w CRC-32
Header	0101+ BxCounter + EventCounter + OrbitCounter + HammingErrors +0101
Checksum	CRC-32bits
Link type / speed	CLPS @ 1280Mbps

Table 3.5: DAQ frame structure for each DAQ link.

each half of the HGCROC, with a link speed of 1.28 Gbps. The DAQ frame has 40x32bit words, starting with a header word, then 38 words (36 normal channel, 1 x calibration, 1 x32bit word for presenting the data for 2 CM channels), and then a word for the 32-bit CRC of all earlier data words. The data frame is followed by at least 1 idle frame whose pattern is programable via slow control. The DAQ header contains different counters and error flags.

When the chip receives the L1A command, the data of the event that occurred a programmed number of bunch-crossings (Bx) earlier (value defined by slow control: typically 12.5 us) is put into RAM2 together with the time tag and Event Counter (EC) values. The latter EC is then increased. Due to the pipelined nature of the internal architecture, the system can manage consecutive L1A. The chip transmits the data provided that RAM2 is not vacant; otherwise, it transmits the IDLE pattern. In this manner, RAM2 functions as a FIFO circular buffer.

TRIG path and data formats

The ADC and TOT data of each channel are fed into the TRIG path. The data processing for the TRIG path includes the following steps:

- *Charge linearization*: This stage involves the deduction of ADC and TOT pedestals and the conversion of TOT values into ADC units by utilizing a multiplication factor derived during the calibration process. It is decided at this step to whether send ADC or TOT for further trigger processing.

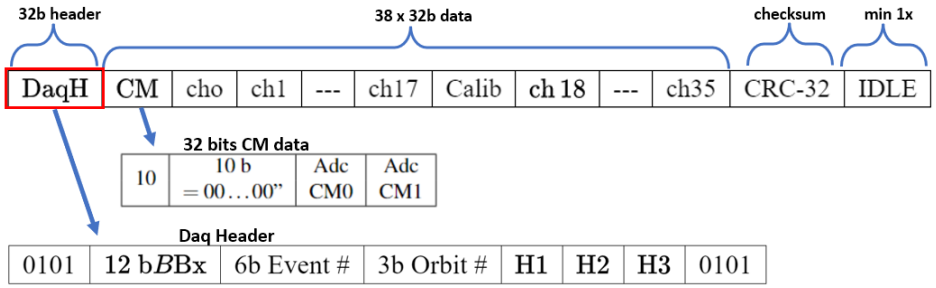


Figure 3.14: The 40 words DAQ frame followed by at least a single idle word is shown

- *Trigger sum*: This segment calculates the sum of 4 cells (for Low-density sensors) or 9 cells (for high-density sensors), referred to as Trigger primitive generation.
- Data compression: The value of the trigger sum is compressed to 7-bit data format (Floating point with 4-bit exponent and 3-bit mantissa) format to reduce the bandwidth of the data.

The Trigger data format consists of four Trigger links, 2 for each half of HGCROC. Each link operates at a speed of 1.28 Gbps, as shown in Table 3.6. A Trigger frame is broadcast for each bunch crossing event. The frames are composed of groupings called Trigger cells (TC), which come in two sizes: either 4 cells (TC4) or 9 cells (TC9), selectable by slow control. A Trigger link consists of a collection of 4 TC. The data is organized in 32-bit words, with the first 4 most significant bits (MSB) acting as the header and the following 28 bits serving as the payload. Each 7 bits within this 28-bit payload corresponds to encoded data for a single trigger cell. Figure3.15 visually represents the mapping of all trigger links, their corresponding Trig-link numbers, and the channel numbers they cover.

# Trig-link	2 or 4 (configurable)
Link type / speed / Bits order	CLPS @ 1280Mbps with MSB first
Possible to switch-off unused link	Yes (partially)
Serialisation factor	32 (i.e. 32 bits per 25 ns)
Packet composition	header (4 bit)+ payload (28 bits) 4 header = packet $[31:28]$ 28 payload = packet $[27:0]$
Header	- During startup : 4'b1010 on all links (enabled or disabled) - During run phase : - LINKRESETROCT procedure: 4'h9 @ BCT else 4'hA on all links (enabled or disabled) - else : 4'h9 @ BCT else 4'hA for enabled links, 4'h0 for disabled links
Payload	- During startup: configurable idle word (default 28 'hCCC_CCCC) on all links (enabled or disabled) - During run phase: - LINKRESETROCT procedure: configurable idle word (default 28'hCCC_CCCC) on all links (enabled or disabled) - else: 4 consecutive Trigger Cells (TC) for enabled links, 28 'h000_0000 for disabled links
Trigger cell (TC) encoding	Floating point with 4 bits exponent and 3 bits mantissa Exponent= TC[6:3] Mantissa = TC[2:0]

Table 3.6: Trigger link data frame details from HGCROC datasheet [18].

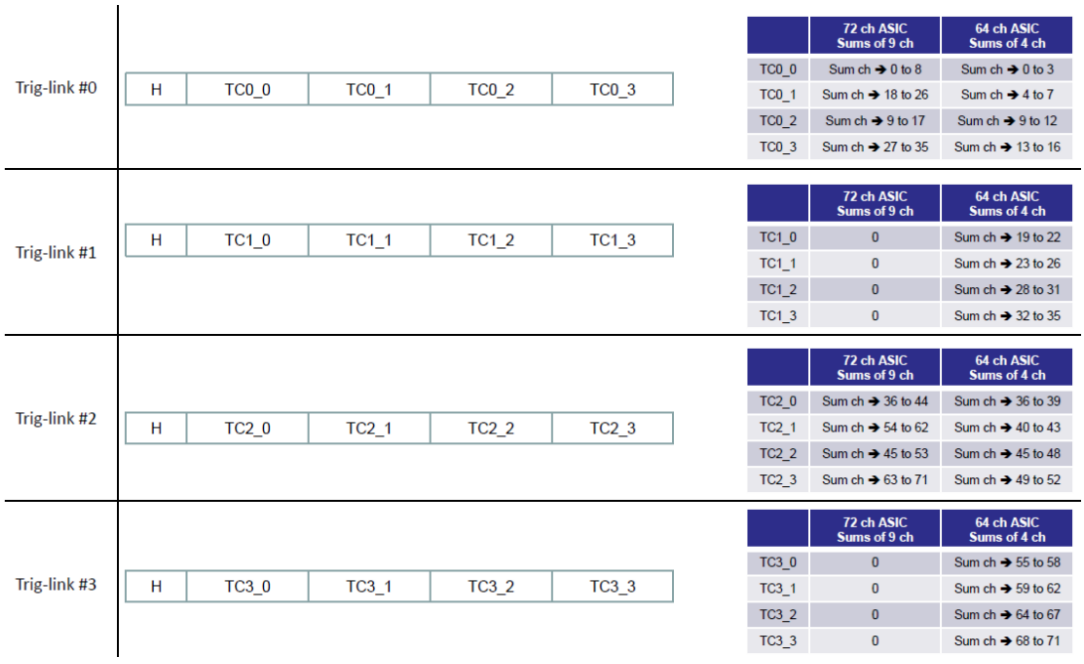


Figure 3.15: 28-bit payload for all Trigger links "$Trig-link[0..3]$" with all Trigger cells (TCs) for 4 and 9 cell sums, adopted from HGCROC datasheet [18].

3.5 ECONS: Concentrator ASICs for HGCAL Data Processing

The ECONs (Concentrators) are custom-designed ASICs engineered for on-detector data compression and selection, ensuring efficient data processing and transmission under the stringent constraints of the HGCAL. These constraints include limited power and bandwidth resources, as well as the radiation tolerance required for operation in the high-radiation environment of the CMS detector at the HL-LHC.

The concentrator ASICs, ECON-D and ECON-T, play a critical role in validating data quality and reducing data bandwidth through the application of several sophisticated algorithms. The resulting data stream is directed to the lpGBT module, which subsequently transmits it to the back-end (counting room) via optical fiber connections. Hosted on the Concentrator Mezzanine Board in the low-density regions and on the HD-Wagon Board in the high-density regions. Although not directly integrated into the Hexaboard, the ECONs are discussed here to provide an overview of all components essential for HGCAL operations.

Two distinct ASICs, ECON-T and ECON-D, are specifically tailored to address the requirements of the Trigger and Data Acquisition (DAQ) paths, respectively.

3.5.1 ECON-T: Concentrator for Trigger Data

The ECON-T is responsible for receiving and processing trigger data. Each HGCROC ASIC transmits four trigger elinks at 1.28 Gbps for every bunch crossing, which are processed by the ECON-T. It selects or compresses the trigger data and prepares it for off-detector transmission at 40 MHz. The ECON-T supports five user-programmable algorithms for data selection and compression: *Threshold Sum (TS) Algorithm*, *Super Trigger Cell (STC)*, *Best Choice (BC)*, *Repeater Algorithm*, and *Autoencoder (AE) Algorithm*. Detailed descriptions of these algorithms and their application are available in references [95, 96].

3.5.2 ECON-D: Concentrator for DAQ Data

The ECON-D is designed for the Data Acquisition (DAQ) path, receiving two DAQ elinks per HGCROC at a data rate of 1.28 Gbps for the L1 trigger rate (750 kHz). The ECON-D performs several critical operations:

- *Zero Suppression*, with programmable corrections for common mode noise and BX-1 pileup.
- *Error Condition Analysis*, generating and transmitting reset requests to the back-end.

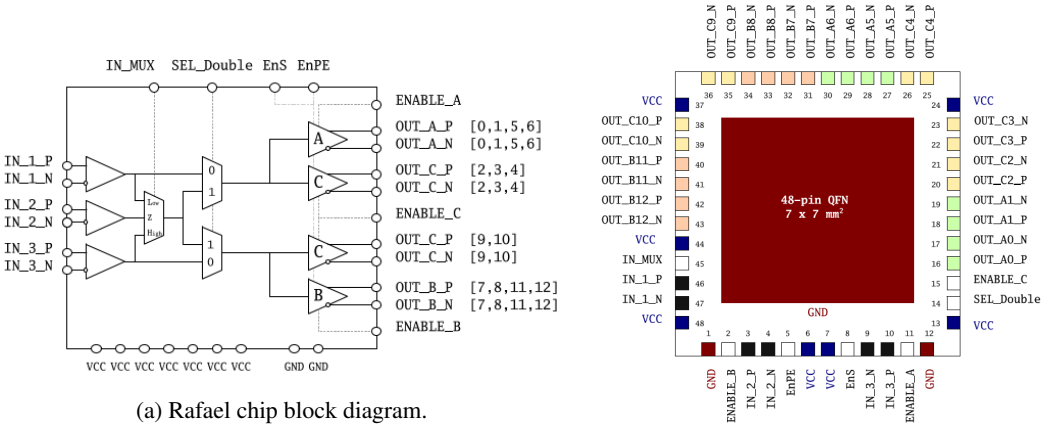
Further details about the ECON-D are available in [97, 98].

3.5.3 Specifications of ECON ASICs

Table 3.7 summarizes the key specifications of both ECON-T and ECON-D ASICs.

Specification	**Details**
TID tolerance	220 Mrad
SEE tolerance	$3 \times 10^6/\text{cm}^2/\text{s}$ hadrons with $E \geq 20$ MeV
Low power consumption	5 mW/channel (total ECON-T+D: 500 mW each for ECON-T and ECON-D)
Power-optimized design	Clock/data gating
Inputs/outputs	12 inputs, 6-13 outputs (most modules use 1-2 outputs) with 1.28 Gbps data rate
Package	128-pin LQFP

Table 3.7: Design specifications for ECON-T and ECON-D ASICs.



(a) Rafael chip block diagram.

(b) 48 pin QFN 12x12 package.

Figure 3.16: (a) The block diagram of Rafael fanout chip (b) the 7×7 QFN package of Rafel chip.

3.6 Rafael fanout chip

The Rafael is a radiation-tolerant ASIC designed for the clock and fast command fanout of the HL-LHC experiment. It is hosted by the LD-Hexaboard in the Low-Density region, and due to space constraints on the HD-Hexaboard, necessitates its mounting on the HD-Wagon board. Its operating voltage is 1.2 V with +- 10 % tolerance and could withstand up to 200 Mrad radiation levels. It has 3 differential inputs and 13 differential outputs. The block diagram and the package information of the chip are shown in figure 3.16. It can be configured as a single fan-out buffer distributing one of the three inputs to up to 13 outputs or a double buffer distribution of one input to six outputs and the 2^{nd} input to 7 outputs. The detail specifications of Rafael ASICs are listed in table 3.8.

3.7 Low dropout voltage regulator (LDO)

The `SGC773000-CRN01` is a custom-designed, radiation-hardened low-dropout regulator (LDO) optimized for the HGCAL project. This LDO combines rapid response, robust regulation, and enhanced stability, making it ideal for the demanding requirements of the CMS HGCAL front-end electronics. It offers exceptional power supply rejection ratio (PSRR), soft-start functionality, over-current protection, and thermal safeguarding, operating seamlessly with ceramic output capacitors ranging from 33 μF to 62 μF across a temperature range of -40°C to $+125^{\circ}$C.

Within the HGCAL power tree, a 10 V input is supplied externally to the detector and stepped down to 1.5 V by a BPOL12-based DC-DC converter. The 1.5 V output is distributed as separate sources for the analog and digital subsystems of the front-end electronics. The `SGC773000-CRN01` further regulates this supply to the required 1.2 V point-of-load voltage for the HGCROCs, ECON-T, and ECON-D ASICs.

The `SGC773000-CRN01` supports advanced functionality, including a 2-bit DAC for digital adjustment of the output voltage in ± 50 mV steps via the P50 and M50 pins. Additional features include:

- Power Enable (EN): Allows digital switching of the LDO *on* and *off*.
- Power Good (PG): Indicates logic high when the output voltage exceeds 95% of V_O and logic low when it falls below 90%.
- Over-current Protection: Identified by the OCZ-tab pin for currents exceeding 5 A.

Feature	Specification
Configuration choices	Single buffer or dual buffer
Fan-out factors	$1:13$ or $(1:6$ and $1:7)$
Signaling	CLPS for differential input/output signals; LVCMOS for control
Frequency range	DC to 400MHz
Channel to channel output skew	50ps
Part to part output skew	300ps
Propagation delay	1.5 ns
Additive jitter	Less than 2ps over 1 Hz – 100MHz range
Driver current setting per group of outputs	1 mA, 2 mA
Pre-emphasis settings per group of outputs	1 mA, 2 mA
Power supply voltage	1.2 V
Power consumption standby state	11 mW
Technology	130 nm TSMC
Package	7 mm $\times$ 7 mm 48-pin QFN
Radiation hardness	Tolerant to 200 Mrad cumulative dose
Temperature range	-30°C to $+40^{\circ}$C guaranteed, with graceful degradation above

Table 3.8: Rafael ASIC design specifications

- Thermal Safeguards: Ensures reliability for temperatures exceeding 85°C.

The LDO's intrinsic bandgap allows fine-tuning of V_O by adjusting resistor divider values (R1 and R2). While the default output is 1.2 V, minor variations can be applied to optimize production binning. Approximately 70,000 units will be deployed within HGCAL, where they are expected to endure radiation doses up to 200 Mrad and hadron fluences reaching 8×10^{15} n/cm^2 (1-MeV Si equivalent) [99].

Figure 3.17 illustrates the basic configuration of the `SGC773000-CRN01`, and Table 3.9 summarizes its critical design specifications.

Symbol	**Description**	**Min**	**Typ**	**Max**
V_I (V)	Input voltage	1.20	1.50	2.00
V_O (V)	Regulated output voltage	1.15	1.20	1.30
I_{max} (A)	Maximum output current	-	-	3
P_{dQFN24} (mW)	QFN power dissipation	-	-	800

Table 3.9: Key design specifications of `SGC773000-CRN01`.

For additional details, consult the LDO datasheet [100].

3.8 lpGBT: Low-Power Gigabit Transceiver and VTRX+

The Low-Power GigaBit Transceiver (lpGBT) and the VTRX+ module are critical components of HGCAL's high-speed, bidirectional optical networks, specifically designed to meet the demands of high-energy physics experiments. The lpGBT functions as a serializer and deserializer (SERDES) ASIC,

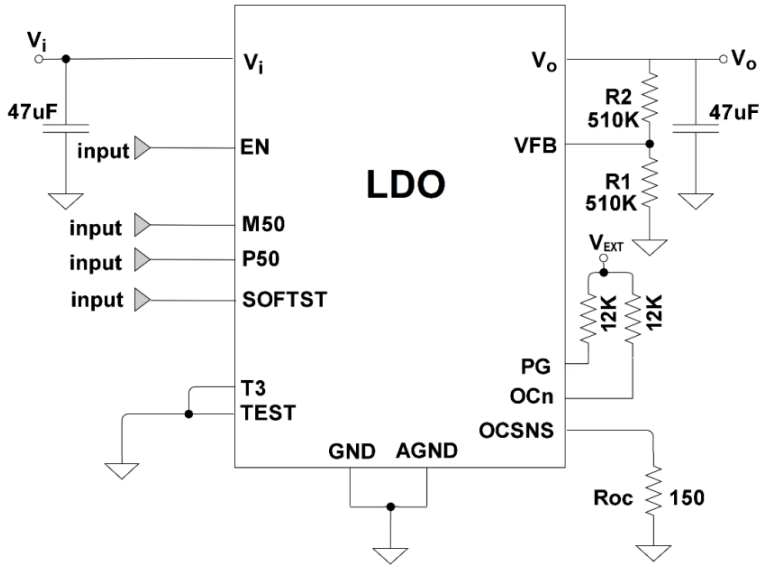


Figure 3.17: Simplified application configuration of the LDO.

while the VTRX+ is a radiation-hardened optical module comprising a laser diode driver (LDD), a transimpedance amplifier (TIA), and commercial VCSEL and PIN photodiode components. Together, these components enable robust communication between the detector's front-end electronics and off-detector back-end systems via optical fibers and COTS (Commercial Off-The-Shelf) transmitters and receivers.

Data Communication architecture: The lpGBT communicates with the back-end using two high-speed links:

- **Uplink**: Operates at 5.12 or 10.24 Gbps, transmitting data from the detector to the back-end. Forward Error Correction (FEC) options (FEC5 or FEC12) ensure data integrity. The FEC5 configuration supports up to seven eLinks per lpGBT at a link speed of 1.28 Gbps.
- **Downlink**: Operates at 2.56 Gbps, distributing control signals, clock synchronization, and configuration data to the front-end electronics.

Each link is divided into three fields:

- **IC-field (80 Mbps)**: Transmits ASIC control information.
- **EC-field (80 Mbps)**: Dedicated to external control data.
- **D-field**: Allocated for data transmission, supporting up to 1.28 Gbps for the downlink and 8.96 Gbps for the uplink, depending on the configuration.

Integration with HGCAL Electronics: In the HGCAL electronics hierarchy, lpGBTs are hosted on Engine boards, which serve as intermediaries between the back-end and the detector front-end electronics. The LD-Engine board employs three lpGBTs (one receiver and two transmitters) with one VTRX+ module, while the HD-Engine board uses six lpGBTs (two receivers and four transmitters) with two VTRX+ modules. These boards distribute clocks, control signals, and fast commands to Hexaboards via interconnects like the Wagon board, which is passive in the LD region but an active and complex board in the HD region, hosting ASICs such as Rafael and ECONs.

Key functionalities: The lpGBT provides several critical functionalities to enable efficient data communication and system control:

- Supports up to 7 eLinks for uplink and 4 eLinks for downlink communication.
- Incorporates 10-bit ADCs for monitoring voltages, currents, and temperatures across detector modules.
- Integrates programmable GPIOs to control and monitor power states (e.g., Power Enable, Power Good).
- Distributes slow control data using an I2C interface in a star topology to serve multiple HGCROCs and ECONs on a single Hexaboard.

Role in data transmission: The lpGBT aggregates HGCROC output data, including DAQ and trigger links, and serializes it for transmission via VTRX+ modules to the back-end. Analog monitoring signals, such as voltage levels from the DCDC and LDO converters, and control signals like reset and power enable for HGCROCs and ECONs, are also routed through the lpGBT's GPIO and ADC interfaces. This ensures seamless integration of digital data and critical control information within the HGCAL system.

3.9 Conclusion

In this chapter, we have gone through all the ASICs used in the front end of HGCAL electronics. These ASICs, including HGCROC, ECON-D, ECON-T, lpGBT, VTRX+, Rafael, and LDO, play pivotal roles in the functionality of the HGCAL electronics system. The HGCROC, functioning as the core readout chip, has been studied in detail, delving into the sub-part level of individual channels. Its function is to capture and process the charge deposited by incident particles within the detector, along with measuring the time of arrival of charges exceeding a predetermined threshold. Subsequently, this processed data is forwarded to ECON-D and ECON-T through dedicated Data Acquisition (DAQ) and Trigger (TRIG) links.

The concentrators ASICs, ECON-D, and ECON-T are responsible for applying several algorithms to validate data quality and reduce data bandwidth. The resulting data stream is then directed to the lpGBT module, which, in turn, transmits it to the back end (counting room) via optical fiber connections. lpGBT receives the clock, fast, and slow control commands from the back end. The clock and fast commands are distributed to front-end ASICs through the Rafael chip. The slow control commands are managed through an I2C link, employing a star topology with one common link serving all HGCROCs and ECONs on the Hexaboard.

It is important to stress that the specifications of these ASICs, especially HGCROC, Rafael, and LDO, will be the main factors driving the design constraints of the Hexaboards (Next chapter).

Chapter 4

Hexaboards, readout boards for the HGCAL Si-Module

4.1 Introduction

The Hexaboard is an 8-inch readout board designed for the silicon layers of HGCAL at the HL-LHC. It serves as the interface between silicon sensors and data acquisition systems, reading charge and ToA signals from the sensors and transmitting DAQ and trigger data to concentrator boards. With 11 variants tailored for full coverage of the silicon layers, the Hexaboard is engineered to deliver precision and reliability in a radiation-intense environment while meeting stringent spatial and operational requirements.

The chapter begins with the formulation of a guiding research question and proceeds to examine the key drivers and design constraints in Section 4.2. Section 4.3 examines the key factors influencing its design, including the geometry of the silicon sensors, the operational constraints of readout ASICs, and the integration requirements within the detector.

The subsequent section (sec: 4.4) delves into the complexities encountered during the design and fabrication phases. Issues such as maintaining flatness, accommodating component density, and ensuring manufacturability under tight tolerances are discussed, highlighting the collaborative solutions that drove progress.

Section 4.5, provides an overview of the Hexaboard variants developed to meet diverse sensor configurations. These include designs tailored for both low-density and high-density silicon sensors, as well as partial boards engineered for specialized geometric regions within the HGCAL detector.

Further, section 4.6 details the integration schemes for power distribution, clock and control signal routing. It describes how these systems were meticulously designed to support efficient and reliable operation under the physical and electronic constraints of the detector environment.

Finally, section 4.7 showcases the finalized Hexaboard versions, including the V3-LD and V3-HD designs, which represent the culmination of iterative refinements and validation efforts. These boards embody the advanced engineering solutions necessary to meet the high demands of the HL-LHC.

4.2 Research Motivation and Design Specification for Hexaboard

The Hexaboard design is to mark a pivotal phase in the realization of the HGCAL front-end readout system. This section is to provide a unified foundation to define the motivation, integration challenges, and performance constraints that are to guide the Hexaboard design strategy.

4.2.1 Research Motivation and Key Design Question

The primary research question that steer the Hexaboard development is:

> *How can a modular, sensor-compliant, and electronically stable readout PCB be architected to integrate within the strict 5.1* mm *vertical space available above the Hexaboard surface, while meeting all signal, power, grounding, and high-speed communication demands for tiled deployment in the HGCAL cassette environment, ensuring manufacturability and bondability with silicon modules, achieving good yield for mass production and assembly, and being verifiably qualified through lab measurements and beam tests to ensure its operational performance prior to production.*

This question is to reflect the complex, multidimensional design space involving electrical, thermal, mechanical, and integration constraints. The Hexaboard is to ensure the safe, noise-resilient, and performance-stable operation of all hosted ASICs, bonded silicon sensors, and connected mezzanine boards throughout its lifecycle. Even a robust ASIC such as HGCROC is to risk significant underperformance if exposed to PCB-level flaws such as poor grounding, excessive crosstalk, or routing noise. Therefore making meticulous electrical design, simulation, and iterative validation in both lab and beam-test environments absolutely essential.

4.2.2 Design drivers and constraints

Sensor-driven requirements: The board is to be compatible with all 11 sensor variants (6 low density (LD) and 5 high density (HD)), including full and partial geometries. Sensor pad density is to dictate the ASIC configuration and analog routing density. The cell size is to influence the choice between LD or HD HGCROC. Mechanical safety is paramount—the board is to mechanically support the sensor while ensuring minimal capacitance to ground. This is to be achieved by keeping the bottom-most copper layer clear of any electrical connections.
HGCROC integration: Each board is to accommodate 2 to 6 HGCROC chips. Each HGCROC is to support 72 analog channels, 4 common-mode channels, and 2 calibration channels. The HGCROC is to transmit DAQ and trigger data through two high-speed DAQ links and up to four trigger links (reduced to two in HD configurations). It is also to include dedicated interfaces for Fast Command, a 320 MHz Clock, and I^2C for slow control. Reset lines and analog parameter monitoring are also to be supported. Preserving the analog dynamic range requires careful routing, minimal crosstalk, and robust grounding
Powering and Grounding: Power is to be delivered as 10 V from the PP0 (cassette outer edge) interface, converted locally to 1.5 V using BPOL12-based DCDC converters, and then regulated to 1.2 V using low dropout regulators (LDOs). Due to space and the harsh radiation environment of HD region, the DCDC modules are to be deported to LD regions. Each HGCROC is to require approximately 1 W, so the cumulative load is to be considered in the DCDC and LDO design. A common-grounding topology is to be employed with, while maintaining separate analog and digital power domains, in order to facilitate noise isolation and ensure stable performance
Signal routing requirements: Up to 460 analog channels are to be routed symmetrically in the group of 4 (for LD) or 9 cells (for HD hexaboard) to form trigger primitives. These signals are to be routed on the mid-layer, with shielding provided by adjacent GND planes. Digital high-speed signals (DAQ, Trig at 1.28 Gbps and 320 MHz Clock and Fast Command) are to be routed on dedicated 100 Ω differential layers. For the complex case, like the full HD board, 12 DAQ, 12 Trig, 3 Clock320, 3 Fast Command, and 3 I^2C links are to be supported. Layer planning is to be optimized to minimize switching and ensure clean signal return paths.
High voltage clearance: Sensor biasing is to reach up to 1000 V at end-of-life. To ensure safety and reliability, all high-voltage nodes are to maintain at least 2 mm clearance from any low-voltage or signal routing.

Mechanical integration and thermal management: The complete assembly to be built above the Hexaboard—including all mounted components, DCDC converters, mezzanine boards (such as Engine and Concentrator), and service passage for ground, 10 V power, and high voltage—is to remain within the strict 5.1 mm vertical envelope. The PCB is to be fabricated with halogen-free materials and limited to a maximum thickness of 1.3 mm. Provisions are to be included for wire bonding, pick-and-place tooling, and service routing (including power, HV, and optical fibers). Mezzanine modules are to connect through dedicated DF12-series connectors, which are also to contribute to the mechanical integrity of the assembly.

Thermal dissipation is to be strategically managed via the connectors of the connecting boards, such as the wagon and concentrator mezzanine, which are intended to function both as signal interfaces and as thermal pathways. The primary source of heat—originating from the DCDC converters—is to be transferred to the Hexaboard through a combination of thermally conductive adhesive tape and connector interfaces. All heat, whether from components directly mounted on the Hexaboard or from connected mezzanine boards, is to be spread laterally across internal copper planes, typically using at least one-ounce copper layers. From there, heat is to be conducted downward toward the sensor and then routed through the sensor to the baseplate interface, ultimately reaching the thick copper cooling plate embedded in the cassette infrastructure.

Table 4.1: Summary of Target Specifications for Hexaboard

Feature	**Specification / Target**
Sensor Type	Hexagonal Si (11 variants: 6 LD, 5 HD); full LD (192 pads), full HD (432 pads); up to 6 guard rings.
Analog Channels	Up to 460 analog signals with shielded layers, are to be routed in a specific pattern to form trigger primitives of 4 or 9 cells.
HGCROC Support	2–6 per board; each with 2 DAQ + 4 (LD) or 2 (HD) Trig links.
Fast Control	1 Fast Command + 1 CLK320 per chip.
Powering	10 V $\rightarrow$ 1.5 V (DCDC) $\rightarrow$ 1.2 V (LDO); HD region to be powered via deported DCDC located in LD regions.
Stack-Up	Multi-layer; analog routed on shielded mid-layer; 1.28 Gbps and 320 MHz on dedicated layers.
PCB Thickness	1.3 mm with 10% tolerance (halogen-free); 8-inch board format, with stephole structures.
Signal Integrity	100 Ω differential routing; separate layers for analog and digital signals.
High Voltage Isolation	$\geq$2 mm spacing from sensor HV pads to other traces.
Noise Target (ENC)	$<$2000e (LD 300 μm), $<$2700e (LD 200 μm), 2250e (HD 120 μm)
Performance Verification	Laser TOA setup, lab tests, beam tests.
Vertical Envelope	Total 5.1 mm above the Hexaboard surface.
Integration Compatibility	Wagon, Concentrator mezzanines and DCDC board to connect via connectors; Engine board requires 0.7 mm clearance above HB.
ASIC Radiation Hardness	All onboard ASICs (HGCROC, Rafael, LDOs) are to pass radiation qualification
EMC Compliance	DCDC modules are to meet EMC standards and be individually verified.

Timing and Noise Performance: Target Equivalent Noise Charge (ENC) is $< 2000\,e$ for 300 μm LD sensors, $< 2700\,e$ for 200 μm LD sensors, and 2250 e for 120 μm HD sensors. Timing performance is to be verified using a precise laser-based injection setup and beam test setup.
Verification and Qualification: The entire design is to be verified using signal integrity and power integrity simulations. Functional validation is to include bare board testing, sensor-attached modules, and beam test measurements. All ASICs hosted by the Hexaboard—such as HGCROC, Rafael, and any LDOs—are to qualify for radiation hardness. Moreover, external boards, particularly DCDC modules with switching elements and coils, are to comply with EMC requirements and are to be individually validated to ensure they do not compromise Hexaboard performance.
Summary of Target Specifications: The summary specification for the Hexaboard design and validation is given in table 4.1. This comprehensive specification framework defines the boundary conditions for the Hexaboard architecture and forms the basis for the layout and component choices elaborated in the design strategy section that follows.

4.3 The strategy for the Hexaboard

The Hexaboard is a specialized printed circuit board (PCB) developed for the silicon region of the HGCAL. Its primary functions are to measure charge signals from silicon pads and determine their time of arrival with high precision, low noise and a large dynamic range. With its unique hexagonal geometry, the Hexaboard integrates multiple HGCROC ASICs, designed to minimize electronic noise and handle a broad dynamic range and operate reliably in radiation-hard environments. Processed data is transferred to the concentrator board and subsequently to the engine board for off-detector processing.

This section examines the critical aspects of the Hexaboard design, including influencing factors such as the characteristics of the silicon sensors, constraints of the readout chips, and the geometric and baseline requirements of the detector. The design objectives are defined to align with the needs of HGCAL, and the strategy to achieve these goals is outlined.

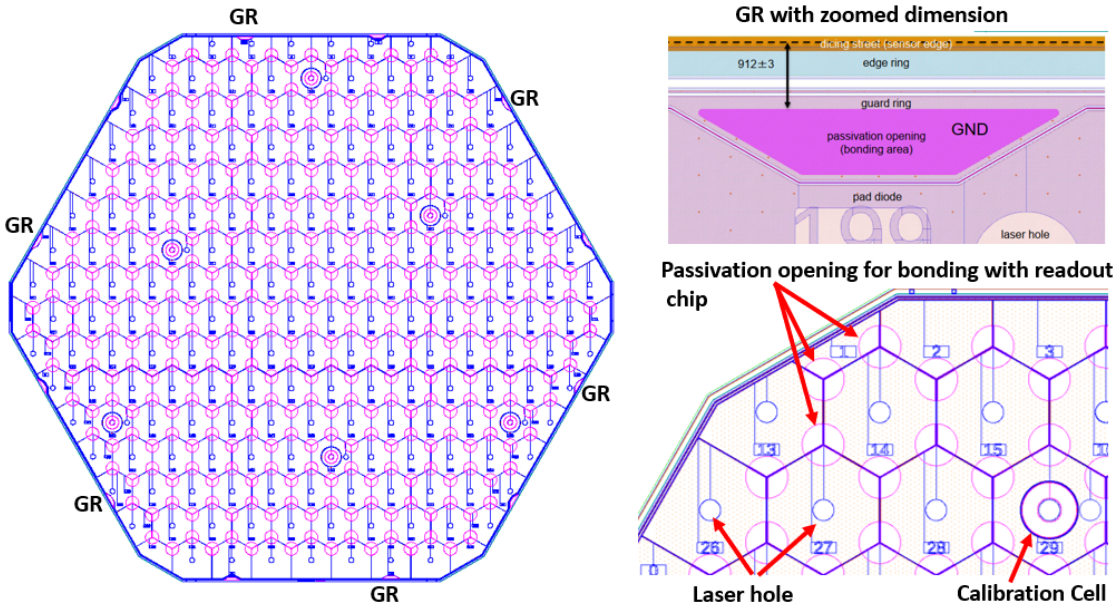
4.3.1 Key Influencing factors in Hexaboard design

The architecture of the Hexaboard is shaped by multiple critical factors, stemming from the characteristics of the silicon sensors, the attributes of the readout chips, and its integration within the detector structure. These considerations collectively influence the physical layout, electronics design, and interfacing requirements of the Hexaboard.

The silicon sensor, which the Hexaboard is designed to read out, is a critical factor influencing the design of the readout board. Key parameters such as cell size, cell count, physical geometry, and connectivity scheme significantly impact the Hexaboard's layout and functionality.

Figure 4.1 illustrates the low-density (LD) silicon sensor, consisting of 192 normal cells, guard rings (GR), and calibration cells. The complete layout is shown in (a), while (b) provides a zoomed-in view of key features. Passivation openings at hexagonal cell junctions facilitate bonding with HGCROC pins, ensuring efficient readout. Dedicated GR openings enable grounding to the Hexaboard, minimising noise and enhancing electrical stability in high-radiation environments. Calibration cells, optimised for signal-to-noise performance, support detector calibration using the MIP signal. Centrally positioned laser holes enable sensor characterisation through controlled optical excitation.

Beyond the sensor characteristics, the Hexaboard design is significantly influenced by the attributes of the HGCROC ASICs. These ASICs are optimized for low noise ($\sim 2000e$) and large dynamic range (0.2 fC to 10 PC), but their packaging and physical constraints impose specific requirements on the Hexaboard. The pin count and configuration of the ASICs dictate the density of connections on the board, while stable power rails with defined ripple margins are essential to maintain reliable operation. Further-



(a) LD si-sensor with 192 normal cells, 6 Calibration cells with 06- passivation opening for Guard Ring (GR) grounding.

(b) The main features, important for Hexaboard design are in zoomed view.

Figure 4.1: LD silicon sensor layout with key design features. (a) The complete sensor consists of 192 normal cells, 6 calibration cells, and 6 passivation openings for Guard Ring (GR) grounding. (b) The zoomed-in view highlights passivation openings for bonding with HGCROC pins, laser holes for sensor characterization, and dedicated calibration cells.

more, low-impedance return paths are critical to minimize signal interference and ensure robust analog and digital performance.

The Hexaboard design must accommodate region-specific variations within the detector while ensuring seamless electrical and mechanical integration with adjoining PCBs, such as DCDC, concentrator, Wagon, and engine boards. Vertical space constraints further dictate component heights and alignment, necessitating careful design to maintain compatibility in high-speed data transfer, power delivery, and mechanical mounting

The Hexaboard design balances sensor geometry, ASIC constraints, power integrity, and mechanical integration, requiring a meticulous approach to ensure precise signal readout and reliable operation in the HGCAL environment

4.3.2 Objectives of the Hexaboard design

The primary objective of the Hexaboard design is to function as the active element of the silicon module, where the Hexaboard is glued together with the silicon sensor, Kapton-shielded copper plate, and baseplate. It must facilitate the precise readout of every sensor cell, provide essential electrical connections such as bias voltage (upto $\sim$ 1 KV) delivery and robust grounding for the guard ring and copper shield and incorporate apertures aligned with the sensor's laser holes to enable light injection for characterization and validation during experimental testing.

Given the stringent 5.1 mm vertical space constraint in the HGCAL detector, a modular design approach is essential. The Hexaboard serves as the base or foundational component, permitting the integration of additional mezzanine boards for extended functionality and provide passage for services inluding

power distribution and optical links.

Similarly, the Hexaboard design needs to be extended beyond the sensor edges to provide physical protection for the delicate silicon sensors, thereby enhancing system longevity and reducing the risk of damage during assembly. Integrated alignment features further facilitate automated assembly, minimizing manual handling and potential errors.

Finally, the Hexaboard must comply with the project's electrical specifications by delivering a clean, well-decoupled power distribution network to the HGCROC and ensuring robust signal integrity for high-speed signals of 320 MHz clock and fast commands and 1.28 Gbps DAQ and Trigger links.

The following sections detail the strategies employed to achieve these objectives.

4.3.3 Hexaboard design strategy

To achieve the outlined objectives, the Hexaboard design strategy focuses on precise integration with the silicon sensors and optimal functionality within the HGCAL detector environment. This involves addressing critical design aspects such as sensor compatibility, signal integrity, mechanical robustness, and manufacturability, all while adhering to stringent spatial constraints.

Figure 4.1 illustrates the layout of the silicon sensors, where each diode pad features passivation apertures at its corners. At the vertices of the hexagonal cells, three adjacent pads are typically accessible, while edge cells are restricted to two. Additionally, six trapezoidal guard ring passivations are distributed along the sensor's perimeter, enabling stable electrical grounding. The application of bias voltage is facilitated through a dedicated passivation opening on the backside of the sensor. These sensor features dictate the key structural and functional elements of the Hexaboard.

Design concept and geometry replication: With these considerations in focus, the Hexaboard was conceptualized to replicate the sensor's hexagonal shape, defining its outline and boundary to align precisely with the sensor edges. To ensure complete protection, the board's outline is extended by 100 μm beyond the sensor edge, as depicted in figure 4.2. This extension by 100 μm reduces the probability of

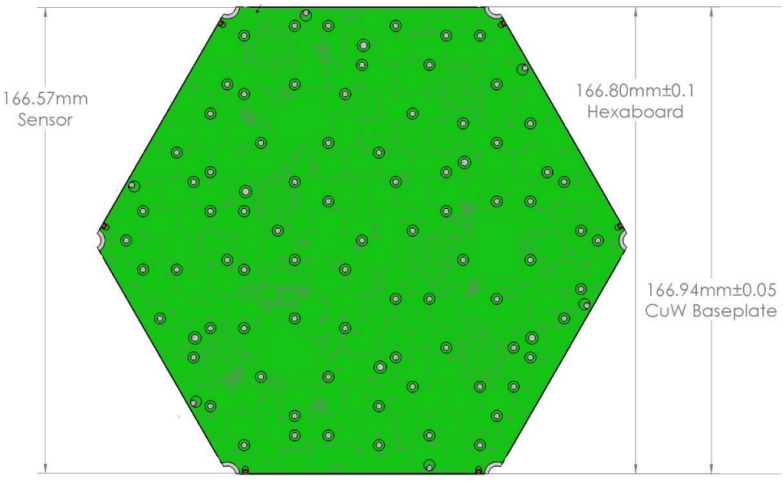


Figure 4.2: The outline of the Hexaboard is 166.80 mm, is extracted from the silicon sensor design, incorporating a manufacturing and placement tolerance of $\pm$0.1 mm. This design ensures that the Hexaboard remains within the baseplate boundary of 166.94 mm $\pm$0.05, providing protection to the sensor while avoiding conflicts with adjacent modules, provided by the University of California Santa Barbara (UCSB) , the pilot Module Assembly center (MAC) for HGCAL.

exposing the sensor edge during module assembly, to 0.18%, confirmed by a statistical analysis for silicon module tolerance shown in figure 4.3 (left), adopted from [22]. Moreover, the analysis in figure 4.3 (right) demonstrates that this extension does not cause the Hexaboard to exceed the baseplate boundary, the probability of such an occurrence is only 0.0006%.

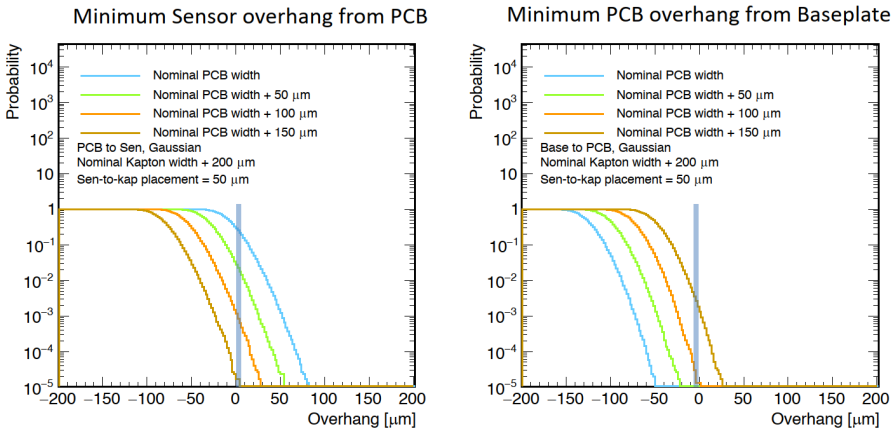
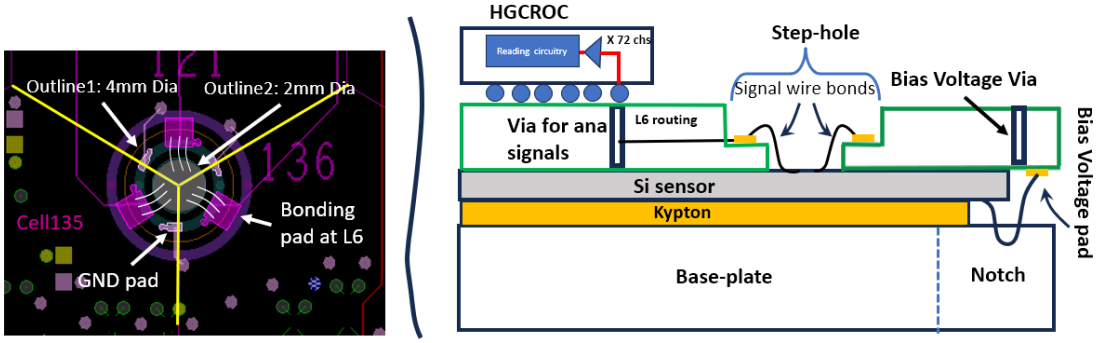


Figure 4.3: A simulation study for outline tolerance performed by UCSB (the University of California Santa Barbara, the pilot MAC) found that considering tooling error in PCB fabrication and placement margin of Hexaboard on silicon sensor, with a 100 μm hangover, a chance to expose silicon sensor on one side is $\sim$ 0.18%, adopted from [22].

By maintaining this alignment, the Hexaboard ensures mechanical stability, minimizes the risk of physical damage to the sensors, and provides robust integration with other detector components.

To facilitate electrical connectivity with each diode cell, the design incorporates a step-hole structure, positioned at the intersections of three adjacent hexagonal cells. This configuration allows access to the passivation opening of the sensor pads, enabling secure wire bonding to the bonding pads located on layer 6 of the Hexaboard, as shown in figure 4.4 (a). For edge cells and guard rings, offset step-holes are

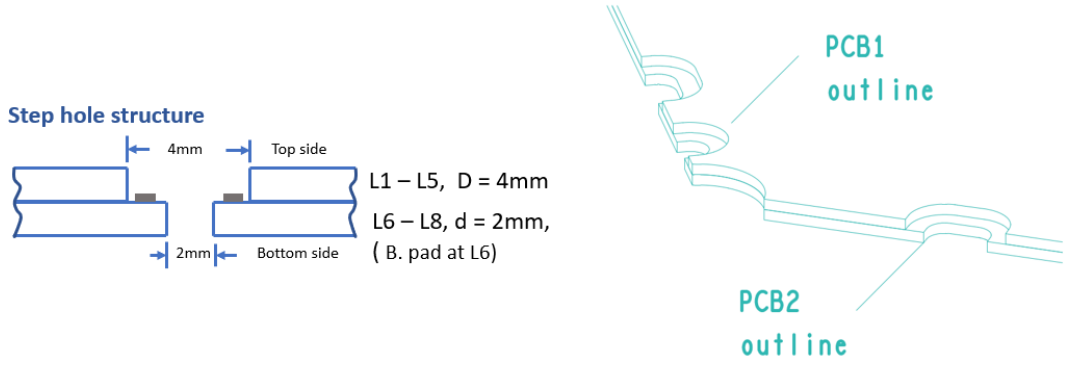


(a) The step hole design view with a 4 mm Diameter in L1-L5 and 2 mm dia in L6-L8. Three adjacent cells 135,136 and 121 are accessed by a single step hole.

(b) Cross-section view of a step-hole, wire-bonding scheme for signal and bias voltage. A pad is bonded to a silicon pad on one side, while the other side is routed on L6 and goes to one channel HGCROC chip.

Figure 4.4: A design and cross-sectional view of step-hole and bonding strategy for signal and bias voltage pads for the module is shown.

introduced, ensuring effective grounding of the guard ring. Notches at the board's edges are included to ground the copper shield of the Kapton-laminated cover layer. Dedicated bonding pads on the backside of the Hexaboard are provided to establish a reliable connection between the bias voltage (BV) and the sensor's backplane passivation as shown in figure 4.4 (b) which depicts the diagram for the bonding and connectivity with analog channels and Bias voltage pads.



(a): Step-hole structure (b): Step structure fabrication

Figure 4.5: Depicting the Hexaboard's step-hole feature (a) and its two-stage fabrication method (b), with the first five layers constituting PCB1 and the final three layers forming PCB2, each with distinct outlines.

The realization of this step-hole structure relies on a two-stage lamination process, as depicted in figure 4.5. The top five layers (PCB1) are shaped with a 4 mm-diameter hole, while the bottom three layers (PCB2) feature a reduced 2 mm-diameter hole. These two sub-assemblies are laminated using no-flow glue to form the complete step-hole architecture, followed by thru-holes, via plating, and outer layers processing. This step-hole structure not only ensures reliable connectivity for each sensor cell but also prevents conflicts between bonding wires and adjacent boards or service cables, thereby upholding the precision and safety of the Hexaboard's connectivity features, a critical aspect of the HGCAL detector.

Modular integration and assembly considerations: The Hexaboard design adopts a modular approach to address the stringent 5.1 mm vertical space constraint in the HGCAL detector, ensuring seamless integration with on-detector electronics and efficient utilisation of available space. Serving as the primary base component, the Hexaboard supports multiple mezzanine attachments tailored to specific functions. These include the DCDC mezzanine for on-detector power regulation, the Concentrator mezzanine for data and trigger concentration, and the Wagon board, which connects the Hexaboard to the Engine board. The Engine board, equipped with lpGBT and VTRx+ modules, facilitates essential tasks such as I2C-based slow control, fast control, and clock distribution. This modular configuration ensures reliable operation, precise control, and smooth integration with the detector infrastructure.

To support automated assembly and maintain mechanical compatibility, the Hexaboard incorporates designated free areas as no-component and no-drill zones, enabling the use of vacuum pick-and-place tools for accurate alignment and handling of components. These features reduce manual intervention and assembly errors while ensuring proper alignment of the Hexaboard with the sensor and baseplate during the module assembly process. By combining modular integration with thoughtful assembly considerations, the Hexaboard design achieves robust functionality and reliability while addressing the tight spatial

constraints and high precision requirements of the HGCAL environment.

Design with signal and power integrity considerations: The Hexaboards are designed with rigorous signal and power integrity to support the system's wide dynamic range (0.2 fC to 10 pC) and meet a stringent noise limit of ∼2000 electrons. They handle high-speed fast commands and clocks with a 320 MHz range, as well as multiple 1.28 Gbps DAQ and trigger links, with all high-speed signals routed as 100 Ω±10% differential lines. These strict noise and data quality requirements demand meticulous attention to signal and power integrity, ensuring consistent performance under the demanding operational conditions of the HGCAL system.

Incorporating sensor geometry replication, a two-stage step-hole architecture, modular integration, and stringent signal and power integrity measures, the Hexaboard design fulfills the HGCAL detector's spatial and electrical requirements.

4.4 Hexaboard challenges

The Hexaboard faces numerous stringent requirements stemming from its intricate design and the demanding operational environment. These challenges span the entire development process, from initial design to module assembly and final integration into the detector cassette. Addressing these challenges requires careful consideration of constraints from multiple sources, which are discussed in the following subsections.

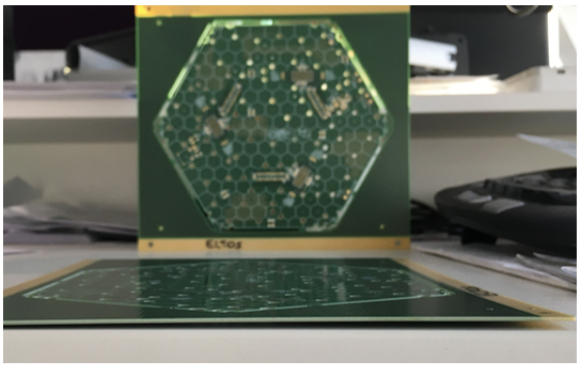
4.4.1 Fabrication challenges

The fabrication of an `8in` large Hexaboard with 100s of step-holes, bonding pads with the stringent requirements of flatness and surface quality makes it a very difficult task to achieve. The complexity comes from the stepped structure of the step-hole implemented at Layer 6 as shown in figure 4.5, which leads to an asymmetrical PCB stack-up. Having to accommodate numerous bonding pads for both the LD and HD configurations requires a significant number of step-holes, making it challenging to ensure board flatness, a crucial factor for functionality and stressless integration with the silicon sensor into the module assembly. Figure 4.6 (a) illustrates a board with a flatness issue. An uneven board is not ideal for assembly as it could put unnecessary pressure on the sensor, raising the chances of potential damage.

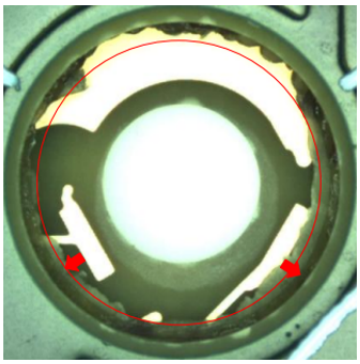
Furthermore, during the final compression cycle of two sub-PCBs (PCB1 and PCB2) to have a step structure, there are often issues with the adhesive non-flow glue, that might seep into the step-hole, accidentally overlapping with sections of the bonding pads, and cause a hindrance in the bonding process. This glue seepage issue is shown in figure 4.6 (b). The frequency of the occurrence of these issues was high at the initial prototyping phase, but with continued contact between the designer and manufacturer, these issues have been solved and the yield has improved.

4.4.2 Module assembly center (MAC) constraints

The Hexaboard is the active part of the silicon module and necessitates meticulous attention during the design phase to meet the MAC constraints. Hexaboards need to be assembled as modules with a silicon sensor, a Kapton-laminated copper shield, and a base plate, which demands micron-level alignment accuracy for the sensor and different features of the Hexaboards. Key design elements include ensuring the Hexaboard's outline extends by 100 um beyond the sensor for sensor protection, placing step-holes exactly at the center of the vertices of the hexagonal pads for uniform coverage of adjacent cells, and positioning analog channel bonding pads tangentially to the sensor's passivation region, right at the step-hole's inner edge, for optimized bonding automation.



(a): Hexaboard with twist and bow (non-flat).



(b): A step-hole with glue seepage over the bonding pad, serious issue for bonding.

Figure 4.6: A few of the Hexaboard fabrication challenges: (a) the non-flat PCB, could not be assembled with a silicon sensor in the module, (b) The glue seepage issue on the bonding pad poses a significant challenge for bonding of the partially covered pad.

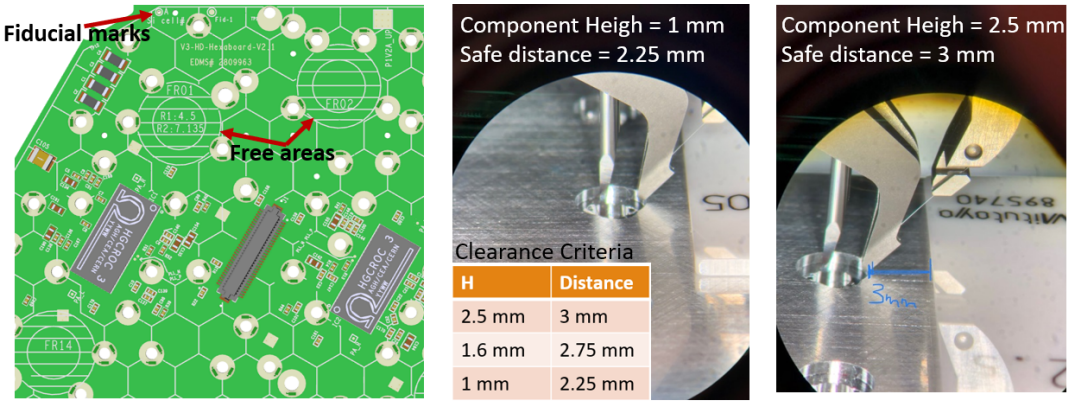
Hexaboard flatness is another critical requirement from MAC, deviations could apply undue pressure on the silicon sensor, risking damage. Therefore, design specifications demand strict flatness with a bow and twist under 0.75% of the PCB diagnal length. Alignment features such as fiducial marks and the "Free areas" shown in figure 4.7 (a) are crucial for precise assembly. Four fiducial marks are placed symmetrically at the four corners of the Hexaboard, providing reference points for the gantry tool. The free areas are designated no-go zones for components and vias, essential for the vacuum cups of pick-and-place tools. Accommodating these free areas (7 in LD and 10 in HD designs), each of the areas with an outer diameter of $\sim$ 14.27 mm, amidst hundreds of step holes, represents a considerable challenge that has been resolved through iterative efforts, validations by UCSB, and design adjustments.

The MAC also imposes stringent requirements to ensure all bonding pads are accessible for bonding procedures. Sufficient clearance must be maintained in front of each bonding pad to accommodate the bonding tool's backside angle structure, as depicted in figure 4.7 (b). The figure shows the experiments conducted at UCSB's MAC, which determined the necessary clearances for components of varying heights from the outer edge of the step-hole in the area in front of a bonding pad. It was found that for components with heights of 1 mm, 1.6 mm, and 2.5 mm, the safe distances from the step-hole's outer edge are 2.25 mm, 2.75 mm, and 3 mm, respectively. Furthermore, it is crucial to pay special attention to aligning the bias voltage and shield bonding pads with the corresponding slots in the base plate and Kapton shield.

The constraints essential for proper module assembly are addressed during the design phase and subsequently verified through an iterative validation procedure involving continuous communication between the design team and the Module Assembly Centres (MAC). This collaborative approach has proven effective in refining and confirming the design guidelines with each new iteration, beginning from the prototyping phase.

4.4.3 Electronics constraints

The readout board design is heavily influenced by the HGCROC specifications, available in two packaging options. The LD version utilizes a 17 mm $\times$ 20 mm BGA with a pitch of 0.8 mm, designed for the LD variant of the Hexaboard. In contrast, the High Density (HD) version features a 17 mm $\times$ 8 mm BGA



(a): A part of Hexaboard showing many MAC constraints.

(b): Bonding pad front-clearance criteria: There should be at least 2.25 mm clearance from outer edge of step-hole in-front of pad

Figure 4.7: A few constraints of MAC validation: (a) Part of Hexaboard displaying the fiducial mark for gantry alignment, many 14.27 mm Free areas for pick and place tool vacuum cups, (b) the bonding pad's font-area clearance and its criteria is shown, The bond-ability of a pad require a minimum of 2.5 mm space in front region, from the edge of step hole to 1 mm heighten components.

with a more compact pitch of 0.6 mm, as illustrated in figure 4.8. The fabrication technology choice, PCB layer stack-up, and BGA fanout scheme are customized to meet the unique needs of each package type.

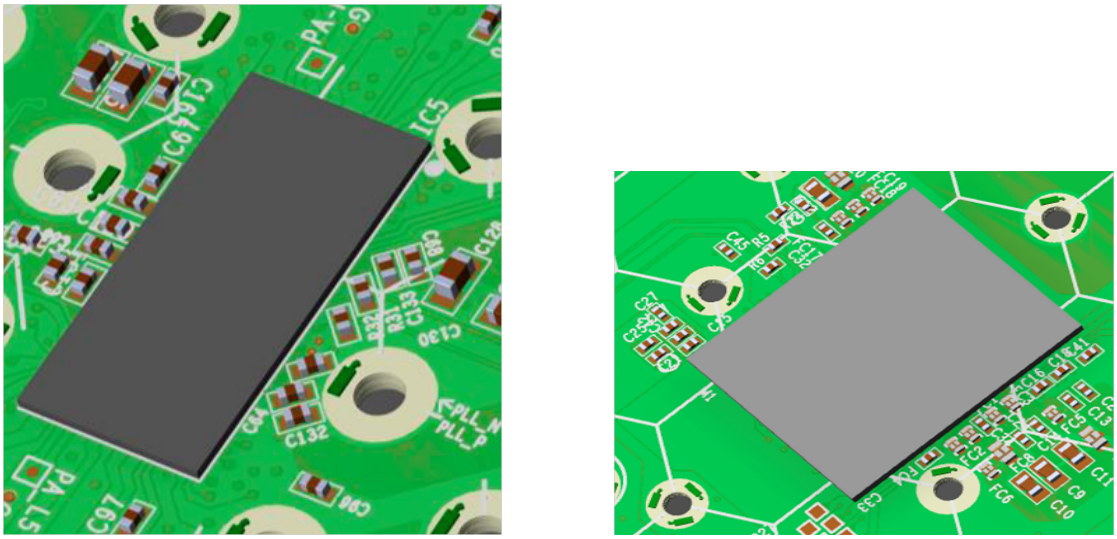


Figure 4.8: The HGCROC V3 packages: HD-package in the V3-HD-Hexaboard (left) and LD-package in the V3-LD-Hexaboard (right), with decoupling capacitors placed in proximity for optimized performance.

The primary design objective of the Hexaboard is to enable low-noise readout of the silicon sensor while allowing the time-of-arrival (TOA) threshold to be set as low as 12 fC, with a full dynamic range spanning from 0.2 fC to 10 pC, as specified in [6]. To meet these stringent requirements, the Hexaboard

is developed following high-speed electronic design principles, with particular emphasis on signal and power integrity. This includes meticulous component placement, strict separation of analog and digital domains, shielding of analog traces within dedicated ground layers, isolation of power domains by subdividing the power plane into separate regions to minimize coupling, and the implementation of low-inductance return paths. Simulation is also incorporated into the design workflow to validate and optimize each aspect, ensuring compliance with the TOA precision targets.
Building upon the overarching design objectives, the following constraints define the core layout and routing strategies implemented across all Hexaboard versions.

Control impedance and shielding of analog signals: One of the key aspects of the electronics specifications is ensuring the integrity of high speed 100 Ω differential signals and shielding of analog routing. To achieve precise impedance control, it is essential to carefully manage the geometry of the differential pair, including the track width and spacing, and to avoid parallel routing when the pairs are on adjacent planes. For all versions of Hexaboards, two layers are designated for differential signal routing. By implementing controlled impedance routing, guarantees signal accuracy and reliable communication between the HGCROC and other detector components.

The analog signals, channels connected to silicon sensor pads, are carefully routed on Layer 6, which is double-sided shielded by ground layers Layer 5 and Layer 7. Avoid layer transitions whenever possible, and bring the signals to the vicinity of BGA and connected to the BGA pins using vias.

Trigger primitive generation: A key requirement of the silicon modules is their contribution to the CMS Level 1 trigger, which involves combining signals from four or nine neighboring sensor cells (trigger cells) to create a trigger primitive. This demands a very tough and constrained routing scheme for analog channels, where it is restricted so that the designer cannot swap the signals across the trigger cell and should have a uniform pattern for all HGCROC across the Hexaboard. This is one of the most challenging nightmares for designers, especially when routing HD designs with 440 analog signals. A trigger cell pattern of 09 cells for HD-hexadboard is shown in figure 4.9.

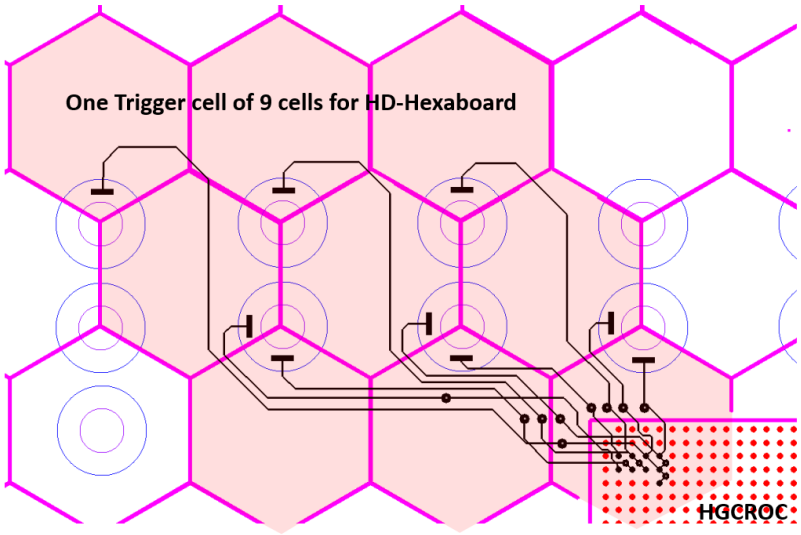


Figure 4.9: The group of 9 or 4 contiguous cells to be routed to specific pins group of HGCROC to form a Trigger cell.

4.4.4 On-detector vertical space constraints

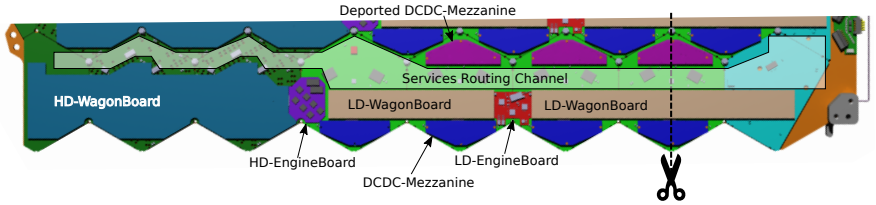
In the context of the HGCAL, the silicon modules design is a complex combination of electronics, mechanics, and spatial constraints. The baseline architecture imposes very tough space constraints with many connecting mezzanine boards, together with a challenging vertical space of 5.1 mm.

In every layer, the silicon modules are sandwiched between absorber lead and stainless steel, together with a copper cooling plate that contains a built-in channel for coolant circulation. The gap between the absorber and the cooling plate is $\sim$ 8.8 mm. Out of this, the silicon and base plate take up around 3.7 mm, leaving 5.1 mm of space for the required readout electronics, such as the readout train, service mezzanine cards, and wires. This intricate arrangement is captured in figure 4.10 (b), which provides a cross-sectional view of an LD silicon module, detailing how the various components fit within the confined vertical space.

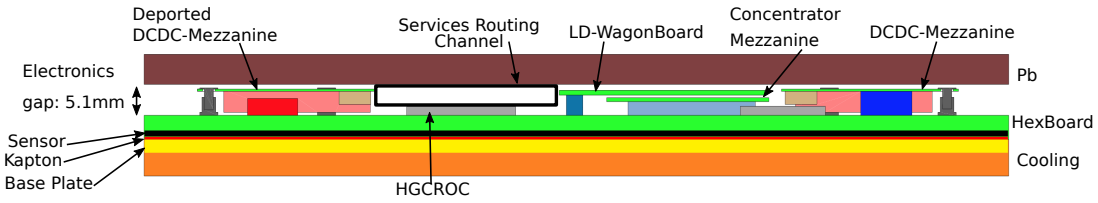
To optimise the use of this limited volume, a strategic approach is employed, involving close collaboration between electronics and mechanical engineering teams. Key to this optimisation is the organisation of LD and HD trains, a series of modules interconnected by a wagon board to an engine board, designed to facilitate service channel access to the innermost silicon modules. This configuration is shown in figure 4.10 (a), illustrating the thoughtful placement of different connecting boards to maintain the continuity of the service routing channel.

Figure 4.10 (c) illustrates the Hexaboard design, incorporating all spatial constraints. The design layout accounts for the placement of various mezzanine boards to fit within the vertical height limitations while allowing sufficient space for a service channel to run throughout the module. The engine boards, highlighted in red, are positioned very close to the Hexaboard, at a distance of about 0.7 mm. This close proximity requires a zone free of components in this area to avoid any mechanical interference with adjacent boards. Similarly, the green areas represent the concentrator mezzanine board with a vertical height of 2 mm. Above these, shown in white, is the wagon board with connectors having a mating height of 4 mm. The aqua-coloured triangle shapes at the left and right corners represent DC-DC converters, each with a vertical height of 4 mm. Under these DCDC converters, numerous no-go areas are designated for the DCDC's thermal shields, where the DCDC will come into contact with the Hexaboard surface. These areas must be free of any components.

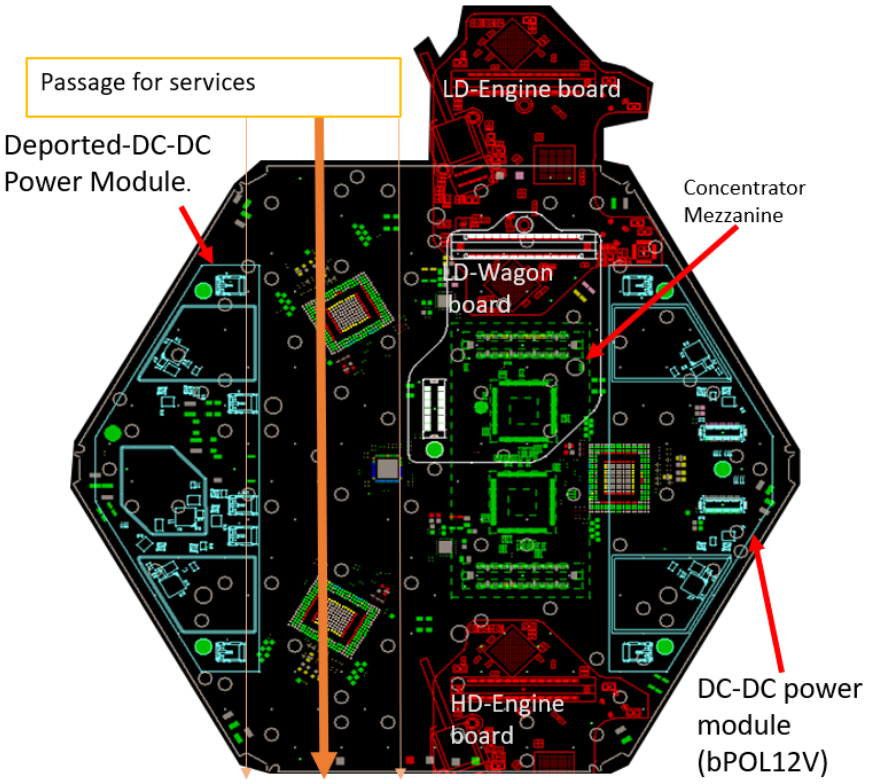
Before the manufacturing phase, a 3-D CAD program is utilised to virtually model the components layout, ensuring compatibility and avoiding any mechanical conflicts within the cassette for all possible assembly scenarios. This pre-manufacturing simulation is a testament to the rigorous planning and precision required in this high-tech engineering projects, as cited in [6, 101]. Through these measures, the HGCAL project aims to maximise the functional density of the Hexaboard within the stringent constraints imposed by the detector's architecture.



(a) The arrangement of on-cassette components to have service routing channel till the inner module of HGCAL cassette.



(b) LD-Silicon module cross-section view (cartooned).

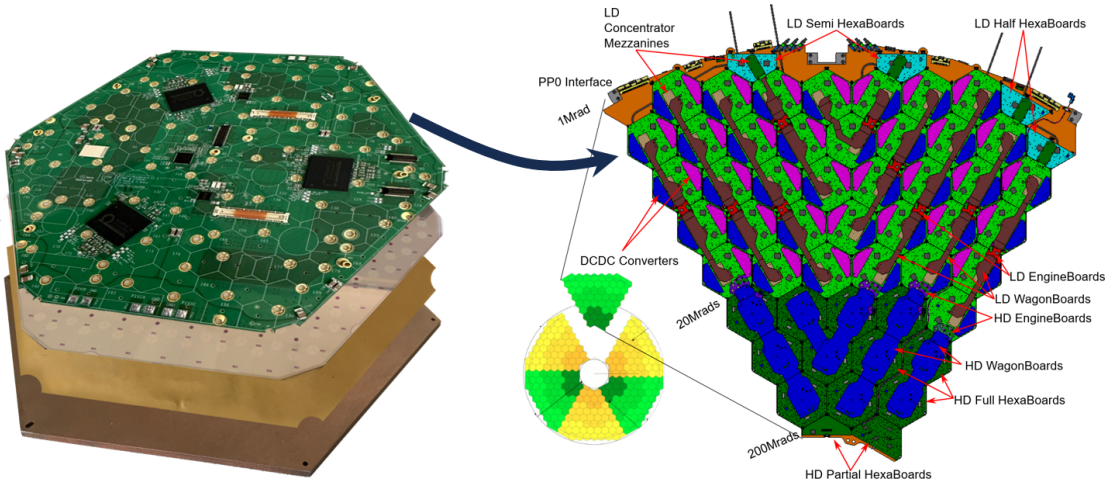


(c) The design view of LD-Hexaboard with all constrained shown.

Figure 4.10: Vertical Integration of Silicon Hex-Modules:(a) illustrates the arrangement of LD and HD trains—a series of modules linked via a wagon to an engine board—organized to ensure the service channel extends to the innermost silicon module.(b) presents a cross-sectional view of an LD silicon module, detailing the configuration of components within the limited vertical space. (c) offers a two-dimensional perspective of an LD-Hexaboard, incorporating all regions subject to design constraints.

4.5 Hexaboards and their variants

The *Hexaboard* is the front-end readout PCB for the silicon region of the HGCAL and serves as an active component of the silicon module, as illustrated in figure 4.11 (left). This modular system forms the basic building block for the readout chain in the HGCAL silicon region.



a: HGCAL Silicon Module

b: HGCAL cassette

Figure 4.11: (a) A silicon module, the basic readout unit for the HGCAL silicon region, comprising a Hexaboard, silicon sensor, Kapton foil, and baseplate. (b) A cassette, instrumented with various types of silicon modules.

To ensure full coverage of the detector, multiple Hexaboard variants have been developed, tailored to the diverse sensor configurations required for the HGCAL cassette, as shown in figure 4.11 (right). These variations are categorized based on sensor pad size and shape, allowing the Hexaboard to adapt to the geometry and radiation profile of the detector.

4.5.1 Hexaboard variants by pad Size

The Hexaboard is available in two variants, designed to match the sensor pad sizes: Low-Density (LD) and High-Density (HD). The LD Hexaboard reads out LD sensors, which have 192 pads, each with an area of 1.18 cm^2, using three HGCROC ASICs. The HD Hexaboard, on the other hand, reads out HD sensors with 432 smaller pads of 0.5 cm^2, requiring six HGCROC ASICs, as shown in figure 4.12.

These Hexaboards are arranged together to form a cassette, with their distribution determined by the radiation profile. LD modules are placed in regions with exposure levels up to 20 Mrads, while HD modules are positioned in higher radiation zones exceeding this threshold.

4.5.2 Hexaboard variants by sensor shape

To optimize coverage within the circular detector geometry, the full hexagonal silicon sensors are segmented into partial shapes. These Multi-Geometry Sensors (MGS) enhance detector coverage and necessitate unique Hexaboard designs for each segment.

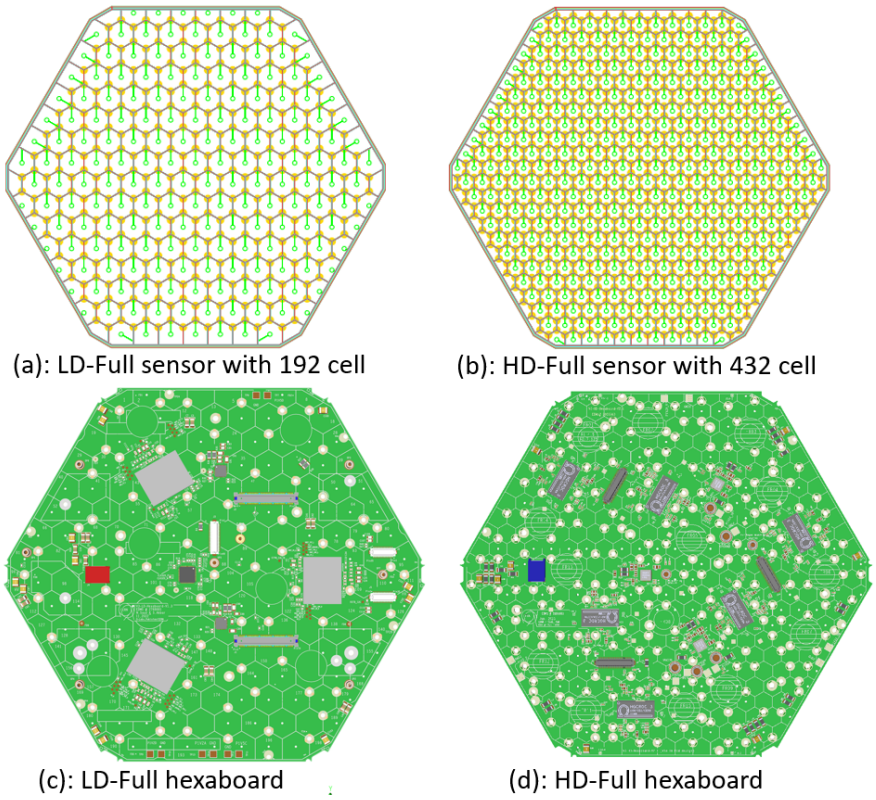


Figure 4.12: Full silicon sensor types (LD/HD) with their respective readout Hexaboards.

For LD sensors, the MGS design incorporates horizontal and vertical dicing lines that divide the sensor into sub-parts, as shown in figure 4.13. The readout boards for these non-hexagonal shapes include five partial Hexaboards: LD-Top, LD-Bottom, LD-Semi-Left, LD-Semi-Right, and LD-Five.

Similarly, HD sensors are segmented into four partial shapes using horizontal and vertical dicing lines, resulting in the HD-Top, HD-Chop-II, HD-Semi-Left, and HD-Semi-Right partial Hexaboards, as shown in figure 4.14. Each segment requires a uniquely tailored PCB to accommodate its geometry and orientation within the cassette.

In total, eleven Hexaboard variants six for LD sensors and five for HD sensors have been developed to ensure comprehensive coverage and reliable readout functionality for the HGCAL detector.

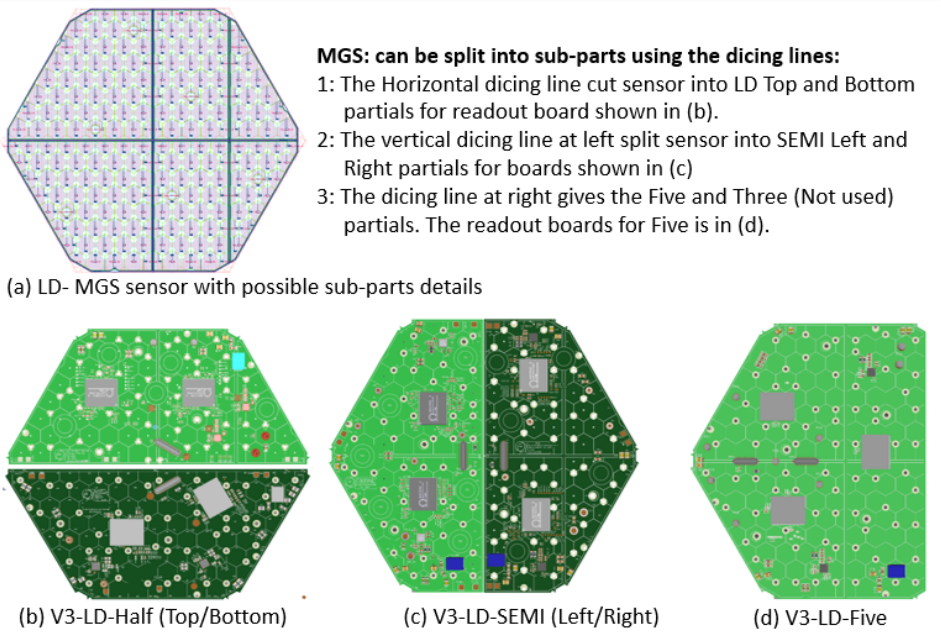


Figure 4.13: LD Multi-Geometry Sensor (MGS) with associated LD partial Hexaboards.

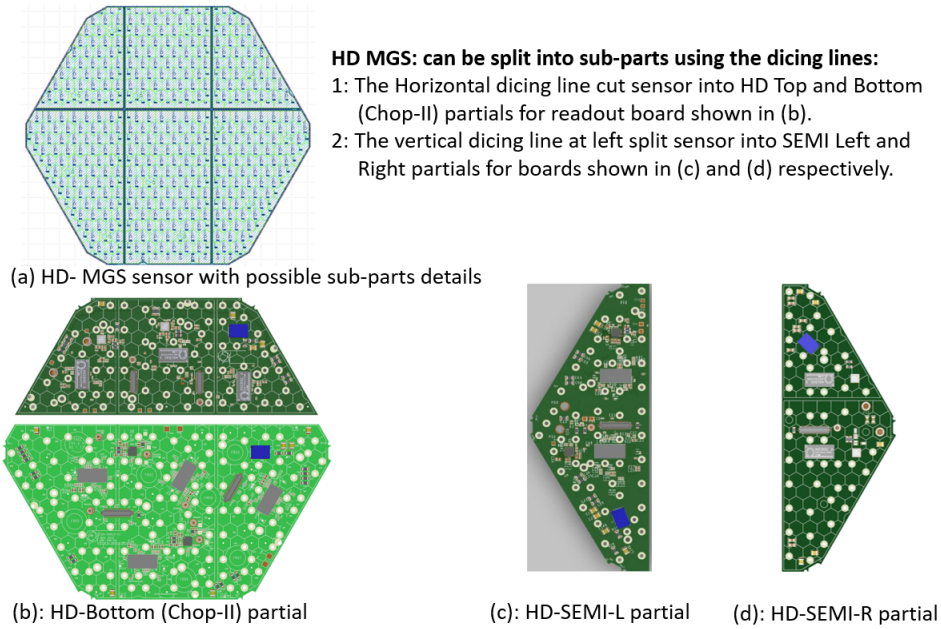


Figure 4.14: HD Multi-Geometry Sensor (MGS) with associated HD partial Hexaboards.

4.6 On-cassette integration scheme for Powering, Clock, and Control

In this section, I will go throuh the on-cassette power, clock, and control (including slow control and fast control) distribution and its realization on the different Hexaboard variants in the system.

4.6.1 On-Cassette power distribution scheme for Hexaboards

The power distribution architecture for the HGCAL's cassettes is illustrated in figure 4.15. The power is delivered at 10 V from the PP0 (outer edge of the cassette) and distributed across the cassette using custom-designed DCDC converters and CERN-designed LDOs.

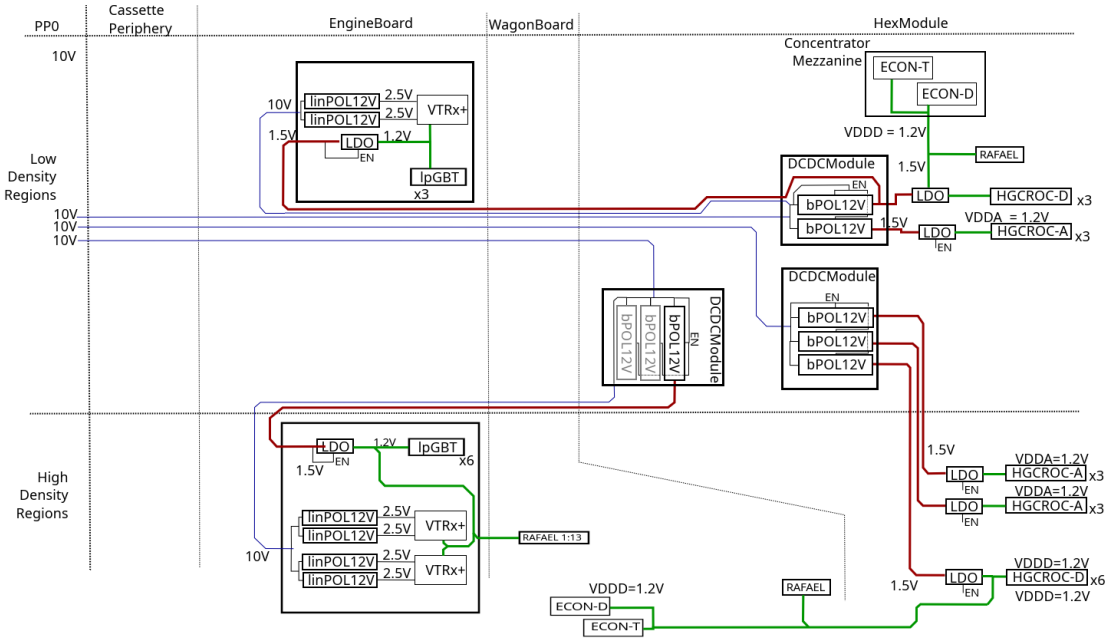


Figure 4.15: HGCAL on-cassette power distribution scheme with full Hexaboards: power distribution system starts with a 10V input from PP0, which is directed to BPOL12-based DC-DC converters that generate the 1.5V necessary for the LDOs on different boards. These LDOs then supply power to the HGCROCs, Rafael, ECONs, and lpGBTs ASICs. The diagram also illustrates how the 10V supply is regulated down to 2.5V through linear regulators for the VTRX+ on the engine boards, adopted from [23].

The block diagram in figure 4.16 outlines the power distribution strategy implemented in the latest iteration of the full Hexaboards. Figure 4.16 (a) explains the powering strategy for the V3-LD-hexadboard, where the 10 V supply is started at the PP0, located at the cassette's outer end, and brought by a dedicated flex PCB "10 V BusBar" to the DCDC converters. The DCDC is a custom-designed DC-DC board based on BPOL-12 switching regulators, which steps down the voltage to 1.5 V. Two different types of DC-DC converters are utilized within the LD region of the Hexaboard. The one type, known as "local DCDC", fulfills the power requirements of the LD Hexaboard it is connected to, by providing two voltages: 1V5C volts for analog circuits and 1V5D for digital circuits. The outputs are then regulated by two CERN-designed LDOs named LDO_D and LDO_A to ensure a consistent voltage of 1V2A and 1V2D for the

analog and digital sections of the HGCROCs, ECONs, and Rafael ASICs.

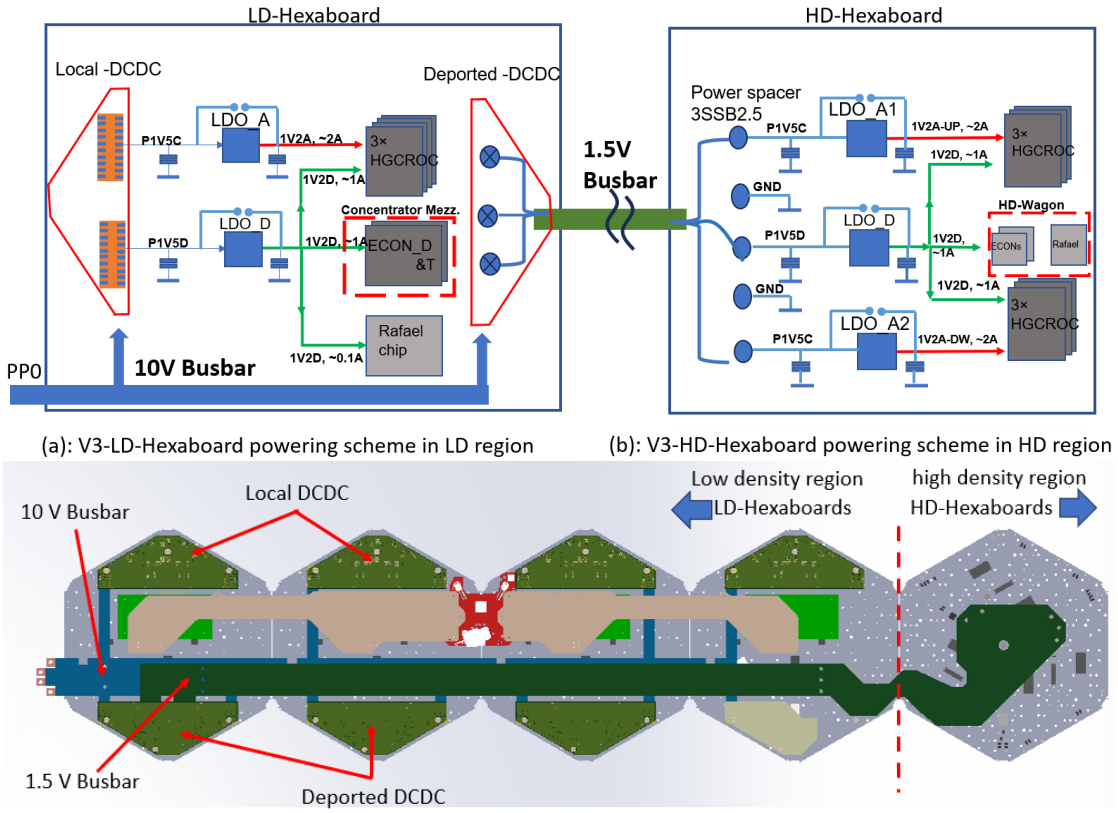


Figure 4.16: On-cassette powering scheme application to Hexaboard: (a) The local DCDC feeds 1.5VC and 1.5VD to the LD-Hexaboard via 2 x DF12-36-DS connector that further regulates 1.2VA and 1.2VD. using two LDOs. (b) For the HD-Hexaboards, the 1.5V is brought from the deported DCDC to the Hexaboard using the 1.5V Busbar, and then further regulated to 1.2VA-UP, 1.2VA-DW, and 1.2VD using the LDOs. (c) depicts the on-cassette powering scheme for LD and HD regions using the 3D CAD models.

The second type, referred to as “Deported DCDC”, is specifically designed to provide power to the HD Hexaboards. Although physically attached to the LD Hexaboard, these converters are electrically separated from their hosts and are positioned within the LD region because of their radiation tolerance profiles. The DCDC provides a 1.5V output, which is then delivered to the HD Hexaboards via a 1.5V busbar system as shown in figure 4.16 (b).

Three LDOs are utilized to regulate 1.5V to 1.2V on the HD Hexaboard. The LDO, marked as LDO-D, regulates 1.2VD to power the digital parts of the six HGCROCs on the Hexaboard, as well as the ECON-D, ECON-T, and Rafael modules situated on the HD-Wagon. Two other LDOs, known as LDO-A1 and LDO-A2, supply power to the analog sections of the HGCROCs. In particular, LDO-A1 provides 1V2A-UP to the analog circuits of the top three HGCROCs, while LDO-A2 supplies 1V2A-DW to the analog sections of the bottom three HGCROCs.

The implications of the powering scheme with 3D CAD models are shown 4.16 (c), illustrating

the concept of busbars and DCDC converters for LD and HD silicon modules. Fours V3-LD modules are situated in the LD region, each equipped with two DCDC converters, local on the upper corner and deported on the lower corner. These DC-DC converters are fed by a 10 V Busbar (in blue). The One HD module placed in the HD region is powered through a 1.5V Busbar (in green) starting from one deported DCDC.

4.6.2 On-cassette Fast Control and Clock distribution

The HGCAL deploys a highly efficient Fast Command (FC) and clock (320 MHz known as CLK320) distribution network, essential for clocking, synchronizing and controlling its electronic components. The fast commands and clock signals are generated by the back end and transmitted through VTRX+ optical receivers, which propagate through lpGBT (DAQ), which then distribute them throughout the complex front-electronics system using Rafael ASIC. The Rafael acts as a central hub for distributing signals, guaranteeing that every HGCROC, ECON-T, and ECON-D receives the required signals of good quality for proper functioning. The fast command and CLK320 distribution are different for different regions and Hexaboard variants and depend on the space available for Rafael ASIC on Hexaboard and the integration scheme.

Distribution in Low-Density (LD) region: For the LD region, the distribution of FC and CLK320 is described in figure 4.17. The fanout chip "Rafael ASIC" is mounted in an almost central location on the LD Hexaboard. The FC and CLK320 signals originate from the LD-Engine board and are conveyed to Hexaboard via the LD-Wagon board, through the Hexboard-Wagon connector. The Rafael ASIC distributes these signals among HGCROCs on the Hexaboard and ECON-T and ECON-D mounted on the Concentrator Mezzanine (CM) board. The Rafael ASIC is configured into double buffered mode, which enables it to accept two inputs and replicate them to 6 and 7 outputs, respectively, to feed 3 x HGCROCs, and 2 x ECONs (D and T) ASICs.

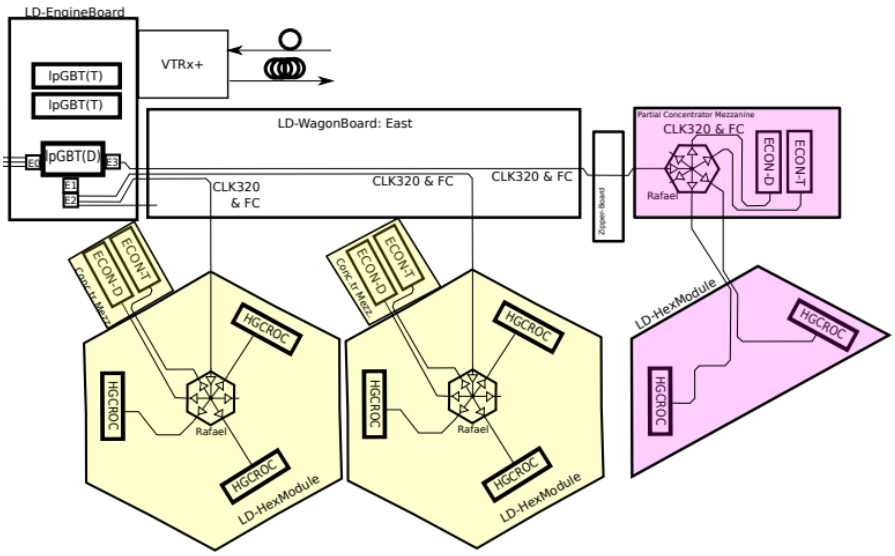


Figure 4.17: Low-Density region Fast Control (FC) and Clock Distribution using Rafael Asic, adopted from [24] figure 4.

For the LD-Partial boards, where space limitations prevent the direct mounting of the Rafael ASIC,

a different mounting strategy is utilised. Rafael is mounted on a partial concentrator mezzanine (PCM) board along with ECON-D and ECON-T. The FC and CLK320, originating at the LD-Engine, are conveyed to the PCM board through the LD-Wagon. subsequently, fan-out by Rafael to ECONS (D and T) ASICs on the PCM board and propagate to HGCROCs mounted on LD-Partials through the PCM to LD-Partial connectors. This configuration makes sure that both the quality of the signal and its distribution are kept at their best, even when space is limited.

Distribution in High-Density (HD) Region: In the HD region, the distribution of FC and CLK320 is illustrated in figure 4.18. Due to the space constraints and the extensive requirement for CLK320 and FC links by the ASICs within the HD region, a specialized configuration is implemented. The Rafael, along with the ECON-T and ECON-D ASICs are situated on the HD Wagon Board. The number of Rafael and ECONs on HD-Wagon is determined by the number of modules that particular HD-Wagon is assigned to read.

The ECLK port of lpGBT-0 (Daq) generates CLK320, which is then distributed by a Rafael chip, configured to single buffer mode, creating up to 13 copies. These copies are directed to ECON-D and ECON-T, as well as to an additional Rafael ASICs for further clock distribution to HGCROCs. The FC signals, originating from the lpGBT, are distributed by Rafael ASICs to both HGCROC and ECON ASICs. To optimise the number of Rafel ASICs some links go directly to ECONS.

The important aspect of Hexaboard design within the HD region is the placement of the Rafael ASIC on HD-Wagon, so for each full Hexaboard, it is necessary to supply six CLK320 links and six FC links to operate six HGCROCs. These signals are managed through the 03 x DF12-60 pins Hexaboard-to-wagon connectors in full HD-Hexaboard. For HD-Partial, the scheme remains the same, and a pair of FC and CLK320 per HGCROC are provided from HD-wagon to HD-Partial.

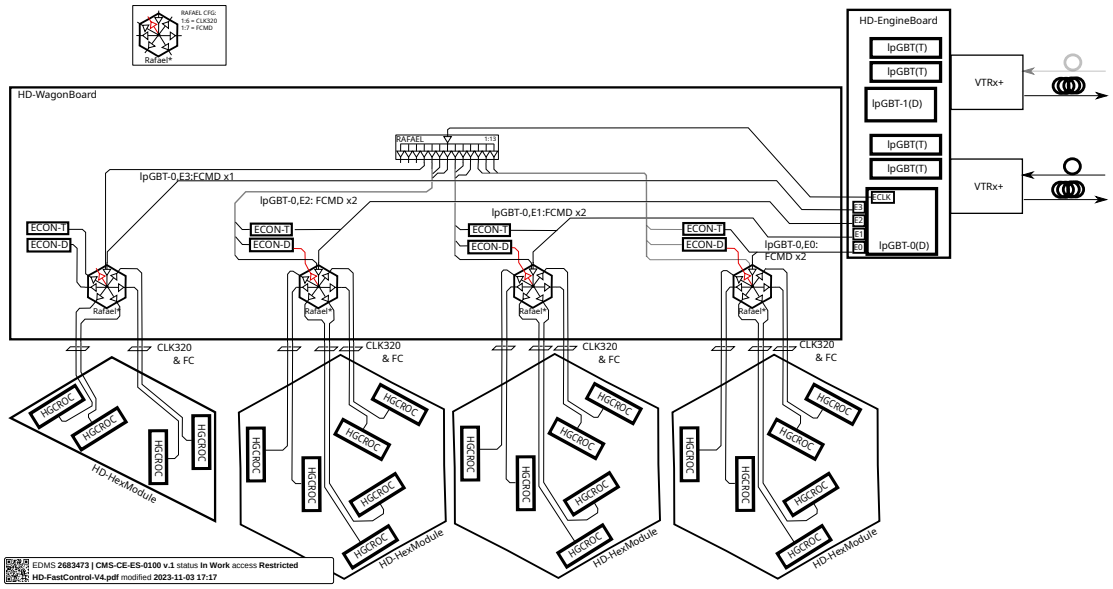


Figure 4.18: How-Density Fast Control and Clock Distribution [25].

The HGCAL employs a highly efficient and adaptive FC and CLK320 distribution network, managed by the Rafael ASIC. The network's versatile design enables efficient signal distribution across LD and HD regions, accommodating spatial limitations and varying module needs. The meticulous arrangement

guarantees that every element receives the necessary signals for optimal performance, showcasing HGCAL's advanced engineering and its dedication to precision and reliability in its operational framework.

4.6.3 The Slow control distribution scheme

The slow controls are received from the back-end by VTRx+ communicated via lpGBT (trigger), and transmitted to LD and HD Hexaboards via wagon boards. For the LD region, there is a single connection per module shared by all $3 \times HGCROC$ and $2 \times ECONs$ in a star topology. For the HD region, there are three connections per HD module, one for each sector (one third of the full Hexaboard). In the sector, the I2C links are further shared by two HGCROCs. All HGCROCs have been assigned a 4-bit I2C address

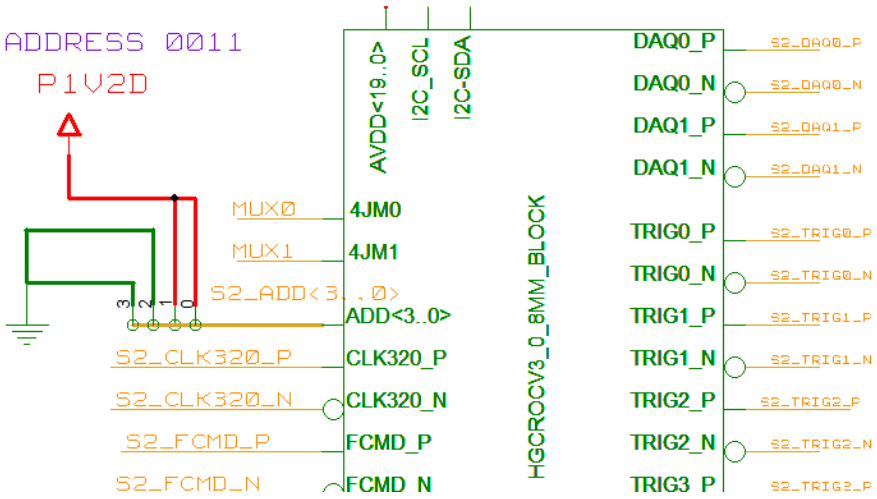


Figure 4.19: HGCROC chip I2C address setting for chip ID 0011

and configured by four hard-wired bits on the Hexaboard. The ID distribution is shown in table 4.2 and its management by HGCROC pins ADD<3..0> is shown in figure 4.19. It can be seen in this table that these addresses are unique across LD and HD full Hexaboard, but for partial, some of the code is being reused, keeping in mind that no train will read both the LD and HD full simultaneously, Similarly, no case exists when a train could have more than one type of partial; therefore, for LD partials, the I2C address of HD full, or vice versa, can be reused, and different types of partials could have the same addresses.

4.7 On-Detector versions of Hexaboard

The final versions of Hexaboards, V3-LD-Hexaboard and V3-HD-Hexaboard, are depicted in figures 4.20 and 4.21, respectively. These designs are currently in production and are deployed according to the baseline scheme of the HGCAL.

The V3-LD-Hexaboard is designed for use with the LD sensor and is equipped with three HGCROC-V3 ASICs to read out 192 sensor cells. Power management is achieved using two DCDC converters—referred to as local and deported—that step down the input voltage from 10 V to 1.5 V. This is further regulated to 1.2 V (analog and digital) using two LDOs, ensuring a stable and reliable power supply to the board's critical circuits. Additionally, the V3-LD variant incorporates a Rafael ASIC, which

	Address Bit						Allocation	Chip	Targeted Full Module	or Partial Module
Device	6	5	4	3	2					
ROC1	0	0	0	1	x		LD/HD	1	LD-Full	HD-Semi-Minus-Right- 0
ROC2	0	0	1	1	*x*		LD/HD	2	LD-Full	HD-Semi-Minus-Right-1
ROC3	0	1	0	1	x		LD/HD	3	LD-Full	
ROC4	0	1	1	1	x		NIL	NIL		
ROC5	1	0	0	1	x		HD	4	LD-Hexaboard-Semi-Half	LD Five
ROC6	1	0	1	1	x		HD	5	LD-Hexaboard-Semi-Half	LD Five
ROC7	1	1	0	1	x		HD	6		LD Five
ROC8	1	1	1	1	x					

Table 4.2: The On-Cassette I2C addresses distribution for Hexaboards variants

facilitates the distribution of the 320 MHz clock and fast commands, ensuring synchronized operation of the board's electronics.

For modular integration, the V3-LD Hexaboard includes connectors for the concentrator mezzanine, hosting the ECONS ASIC, and the LD Wagon board, which links the Hexaboard to the Engine board. The components are arranged using CAD tools to fit within the 5.1 mm vertical space constraint while maintaining service passages. Reserved no-go areas on the board prevent the placement of components where the Engine board, located just 700 μm above the Hexaboard, might interfere.

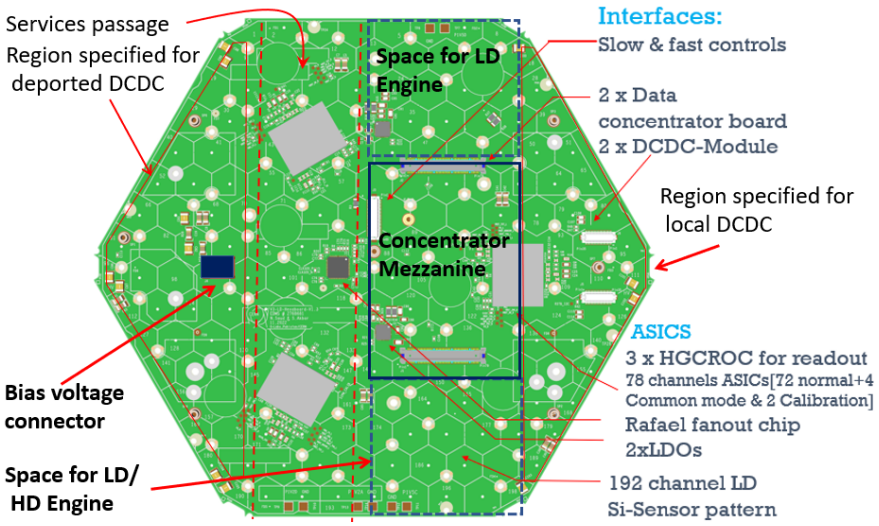


Figure 4.20: Final version of the V3-LD-Hexaboard (Full): hosts three HGCROCs to read 192 sensor cells, a Rafael ASIC for clock and fast command distribution, reserved locations for deported and local DCDC converters, and LDOs for analog and digital 1.2 V regulation. The board also includes connectors for the LD Wagon and concentrator mezzanine.

On the other hand, the V3-HD-Hexaboard, shown in figure 4.21, is designed for HD sensor and employs six HGCROC-V3 ASICs to read out 432 channels. To address the increased component density, the Rafael and ECONS ASICs have been strategically relocated to the HD Wagon board. This adjustment overcomes spatial constraints and ensures efficient fan-out of the 320 MHz clock and fast commands across the HGCAL module train.

The HD Wagon board serves as the central hub for clock and fast command distribution in the HD

configuration, demonstrating the adaptability of the Hexaboard design to meet varying density and operational requirements. Power regulation on the V3-HD-Hexaboard is managed using three LDOs, one for digital and two for analog circuits providing a stable and reliable power supply to the analog parts of the HGCROCs.

The V3-HD-Hexaboard integrates three DF12NB-60-DS connectors for interfacing with the HD Wagon board and incorporates spacers for secure integration. Its layout has been carefully optimized to balance the high channel density, mechanical constraints, and performance requirements, ensuring reliable operation under the challenging conditions of the HGCAL detector.

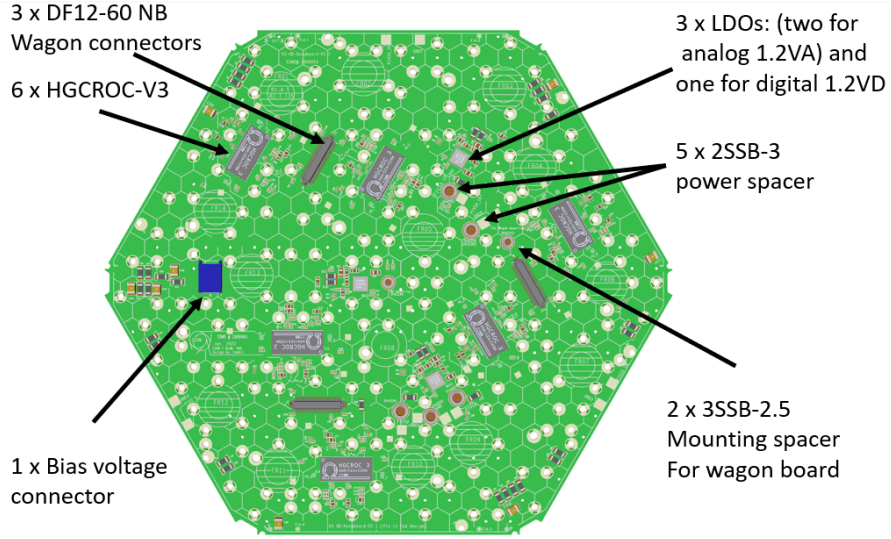


Figure 4.21: On-detector version of V3-HD-Hexaboard (Full): Includes six HGCROCs to read 432 channels, three LDOs (one for digital and two for analog power), three DF12NB-60-DS connectors for interfacing with the HD Wagon board, and mounting spacers for power entry and wagon integration.

These finalized Hexaboards underscore the HGCAL's commitment to precise engineering and modular design. The strategic placement of ASICs and integration of customized power solutions ensure the efficient operation of the detector's electronic systems, reflecting the advanced engineering underpinning the HGCAL design.

4.8 Conclusion

In this chapter, we examine the Hexaboard's role as the readout interface for HGCAL silicon modules, discuss its constraints, and outline a strategy to address these challenges. This is followed by an overview of Hexaboard variants and the power and control distribution system.

The chapter began by outlining the strategic considerations that shaped the Hexaboard's design. The interplay between sensor geometry, ASIC constraints, and mechanical integration was identified as a driving force in defining its layout and functionality. These foundational insights guided the development of a robust design strategy that ensures compatibility with the HGCAL's modular architecture.

Next, the complexities of the design, fabrication, and integration phases were discussed in detail. Challenges such as maintaining flatness, accommodating high component density, and ensuring manufacturability under precise tolerances were addressed through iterative refinement and collaborative problem-solving. These efforts underscore the precision required for such a high-performance system.

The discussion of Hexaboard variants highlighted the adaptability of the design to meet diverse sensor configurations. Variants tailored for low-density (LD) and high-density (HD) sensors, as well as partial boards for irregular geometries, showcased the versatility necessary for seamless integration across the HGCAL detector layers.

Power distribution, clock synchronization, and control signal routing schemes were meticulously analyzed, reflecting the intricate systems engineering required to ensure operational reliability. The integration of DCDC converters, LDOs, and Rafael ASICs demonstrated innovative approaches to meeting the stringent space and performance constraints.

The chapter concluded with an overview of the finalized V3-LD and V3-HD Hexaboard designs, refined through iterative validation, meeting key targets in noise reduction, signal integrity, and space utilization.

This chapter has provided a comprehensive account of the Hexaboard's development, from strategic design principles to the realization of final on-detector versions. These efforts not only highlight the collaborative ingenuity of the HGCAL project but also set a high standard for future advancements in particle detector technology.

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Chapter 5

Hexaboard Design Evolution to baseline Scheme

5.1 Introduction

This chapter focuses on the design evolution of the Low Density (LD) and High Density (HD) Hexaboards, which form an essential part of the CMS-HGCAL readout system. Their development represents a significant step forward in optimising detector performance to meet the demands of future particle physics experiments. The chapter begins by establishing the criteria for design evaluation in Section 5.2 and giving an overview of the test system used for the performance evaluation in Section 5.3.

Section 5.4 provides an overview of the LD design evolution, from the initial to the final version, with detailed discussions presented in the subsequent sections. The initial design phase, detailed in Section 5.5, introduced the LD-Hexaboard-CMS-V1, which leveraged existing knowledge but faced challenges related to noise levels and digital modulation. A detailed review, presented in Section 5.6, identified the primary root causes of these challenges, tracing them to the stack-up design taken from earlier prototype of the Hexaboard. Subsequent iterations, described in Sections 5.7 and 5.8, resulted in the LD-NSH-HB-V2 and V3-LD-Hexaboard types. These versions achieved significant improvements in noise reduction and digital modulation performance through optimized layering techniques and thorough design evaluations, as summarized in Section 5.8.2.

A critical milestone in the design process, discussed in Section 5.11, was the debugging of digital modulation issues. This challenge became particularly relevant with the integration of the HGCROC-V3 chip. Investigations into the internal ground configurations of the ASIC package provided key insights, leading to substantial improvements in the V3-LD-Hexaboard design.

The evolution of the HD-Hexaboards is explored in Sections 5.10 and 5.12, culminating in the development of the V3-HD-Hexaboard-V2.2. This advanced version incorporated the Via-in-Pad technique, significantly enhancing power and signal integrity. The V3-HD-Hexaboard-V2.2 demonstrated notable reductions in noise and digital modulation, making it ready for large-scale pre-production and production phases.

Finally, Section 5.13 addresses the development of partial Hexaboard designs for both LD and HD configurations. These designs accommodate unique geometries required to achieve complete sensor coverage within the HGCAL and are used in the peripheries of each layer.

Through a systematic process of iterative design and performance validation, the Hexaboards have been meticulously optimised to satisfy the stringent operational requirements of the HL-LHC environ-

ment, thereby reflecting the advanced engineering principles and innovation at the core of the HGCAL detector architecture.

5.2 Design evaluation criteria

The Hexaboard performance is evaluated using three primary parameters: noise, digital modulation, and coherent and incoherent noise. These metrics serve as the foundation for evaluating the board's performance in meeting the stringent operational requirements of the HGCAL.

Noise Evaluation:
In silicon-based calorimeters, the electronic noise of the front-end readout system is a critical parameter influencing both charge and time measurements. It is commonly quantified as the *Equivalent Noise Charge (ENC)*, defined as the input charge that would generate an output signal equal to the root-mean-square (RMS) value of the system noise.

For the HGCAL system, noise is evaluated by measuring the standard deviation (σ) of the ADC output distribution in the absence of a signal. Contributing factors include thermal noise from the preamplifier, shot noise from sensor leakage current, and parasitic noise from PCB layout and coupling. The measured σ, expressed in ADC units (ADCu), is converted to electrons using the calibrated charge gain of the HGCROC ASIC.

In this study, the silicon module employed a 300 μm n-on-p sensor biased at -280 V, with an estimated input capacitance of 47 pF. The HGCROC was configured in medium gain (160 fC ADC range), for which 1 ADCu corresponds to approximately 1250 electrons. The average noise across all channels of a representative chip was measured as 1.29 ADCu, with a channel-to-channel dispersion of 0.11 ADCu. This corresponds to an ENC of $\sim$1619 electrons, comfortably within the HGCAL TDR design requirement of $<$2000 e^- [6].

This noise level provides a robust signal-to-noise ratio (S/N) of over 13:1 for a MIP signal, which typically deposits a signal of $\sim$18 ADCu in a 300 μm sensor. Such performance ensures high detection efficiency and contributes to timing precision, particularly for low-charge hits. Maintaining low ENC is essential to limit timing jitter in the TOA measurement, supporting HGCAL's target timing resolution of $<$30 ps per particle shower.

Digital Modulation:
Digital modulation, also referred to as digital noise, represents the undesired coupling of the 40 MHz clock onto the HGCROC analog channels, primarily caused by disturbances on the preamplifier ground. This phenomenon degrades the analog front-end performance, affecting both the dynamic range specification (0.2 fC to 10 pC) and the Time-of-Arrival (TOA) threshold of 12 fC [27]. In HGCROC, the ADC sampling phase can be chosen in to one of the 16 steps for 25 ns of bunch crossing time. The modulation across all phases represents the digital noise superimposed on the analog channels. Ideally, the pedestal should remain constant across all phases, however, deviations are observed during the testing.

In figure 5.1 (right), the pedestal variation across the 16 ADC sampling phases for Channel 12 is shown. The difference between the maximum (96 ADCu) and minimum (83 ADCu) pedestal values defines the digital modulation, referred to as Δ-pedestal, with a measured value of approximately 13 ADCu. This parameter quantifies the level of digital noise superimposed on the analog preamplifier output. Given that 1 ADCu corresponds to roughly 1250 e^- under medium gain settings, this translates to approximately 2.4 fC.

Although the Δ-pedestal does not exhibit a strict one-to-one correlation with the ToA threshold, it plays a critical role in determining the minimum threshold that can be reliably configured. A lower

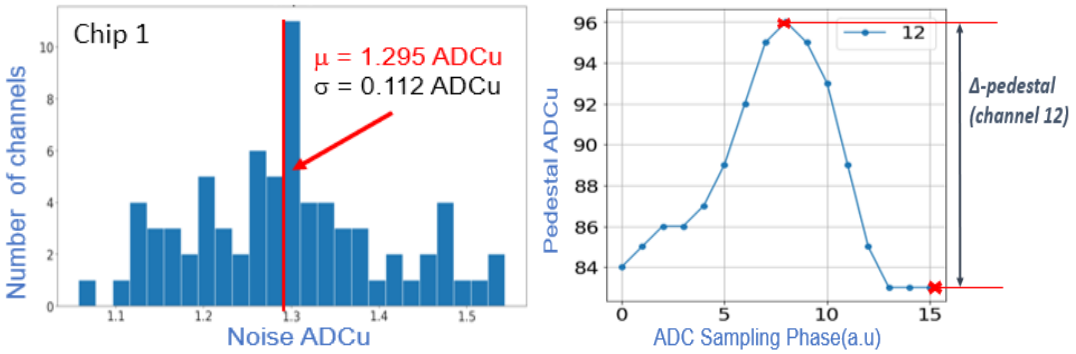


Figure 5.1: Noise histogram per chip (left) and pedestal variation with ADC sampling phases for channel 12 of HGCROC (right).

Δ-pedestal is therefore desirable, as phase-dependent oscillations at the preamplifier output are directly coupled to the input of the ToA discriminator, as illustrated in Figure 3.1. Observations from module testing indicate that silicon modules with Δ-pedestal values exceeding 20 ADCu are prone to digital instability, characterized by random triggering of multiple TDCs. This behavior undermines the stability of the ToA discriminator configuration and degrades the overall timing performance of the system.

Coherent and Incoherent Noise:
Noise analysis is a fundamental diagnostic tool in assessing the readout quality of Hexaboards and silicon Hex-Modules. Two key components are defined: *incoherent noise* (IN), which represents uncorrelated, random fluctuations specific to each channel, and *coherent noise* (CN), which corresponds to correlated variations simultaneously affecting multiple channels.

Incoherent noise primarily arises from intrinsic sources such as thermal (Johnson-Nyquist) noise, shot noise in the sensor, and local front-end electronics [73]. It manifests independently across channels and sets the baseline for per-channel noise performance. In contrast, coherent noise originates from common-mode sources like fluctuations in bias or low-voltage power supplies, clock coupling, or ground loop effects, and typically adds a systematic component to all channel responses.

To quantitatively separate these contributions, a statistical method based on Direct Sum (*DS*) and Alternate Sum (*AS*) is applied over the pedestal values of $n = 72$ channels [102]:

$$DS = \sum_{i=0}^{n-1} \text{ped}[i], \qquad AS = \sum_{i=0}^{n-1} (-1)^i \text{ped}[i]. \tag{5.1}$$

Here, $\text{ped}[i]$ denotes the pedestal value of the i^{th} channel. The *DS* aggregates all pedestal values and is sensitive to correlated fluctuations, while *AS* alternately adds and subtracts channel values to suppress correlated effects, emphasizing uncorrelated (incoherent) noise instead.

From these summations, the incoherent and coherent noise levels are computed as:

$$IN = \frac{\text{rms}(AS)}{\sqrt{n}}, \qquad CN = \sqrt{\frac{\text{var}(DS) - \text{var}(AS)}{n}}. \tag{5.2}$$

where $\text{rms}(AS)$ is the root-mean-square of the alternate sum, and $\text{var}(\cdot)$ denotes statistical variance. *IN* captures the average channel-level noise contribution, normalized by the number of channels, while *CN* isolates the excess variance in *DS* relative to *AS*, attributed to coherent effects.

An example of noise decomposition is presented in figure 5.2, where IN and CN noise components are extracted from the pedestal data of the V3-LD-Hex Module. The measured IN value of 1.91 ADC counts corresponds to approximately 2300 e^- for a 47 pF detector capacitance, which is consistent with the typical pedestal noise target range of 2000–2700 e^-, confirming acceptable per-channel noise performance.

The coherent noise is measured at 0.64 ADC counts. Although no strict specification exists for CN, its magnitude serves as a comparative metric. Lower CN values indicate effective suppression of common-mode disturbances and reflect improved analog-digital isolation, impedance control, and power integrity.

Such decomposition plots are instrumental in comparing multiple Hexaboard designs. During final validation, CN is used as a key performance indicator to identify the most optimized layout in terms of shielding strategy, stack-up design, and grounding scheme.

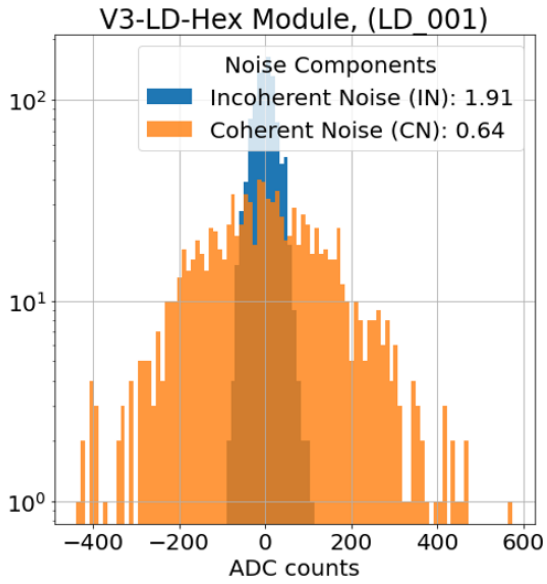


Figure 5.2: Alternate sum (AS) and direct sum (DS) distributions derived from pedestal data of the V3-LD-Hex Module. These histograms serve as the basis for extracting the incoherent (IN) and coherent (CN) noise components. The noise metrics are computed using statistical estimators, $\mathrm{rms}(AS)/\sqrt{n}$ and $\sqrt{[\mathrm{var}(DS) - \mathrm{var}(AS)]/n}$, providing a quantitative benchmark for design-level noise performance evaluation.

Noise Target Specification:

The noise target values for silicon Hex-Modules are dependent on detector capacitance. These benchmarks, extracted from measurements conducted by ASIC designers, serve as reference points for evaluating the Hexaboard's electronic noise performance. Figure 5.3 illustrates the Equivalent Noise Charge (ENC) plotted against varying capacitance values at a typical 160 fC ADC gain. These benchmarks act as critical indicators, guiding the optimization of electronic noise performance in the Hexaboard design.

Figure 5.3 presents ENC as a function of sensor capacitance for various silicon sensor thicknesses. For 300 µm Low Density (LD) sensors with a capacitance of 48 pF, the ENC target is approximately 2000 e^-. For 200 µm LD sensors with 69 pF, the target is 2700 e^-, while for 120 µm High Density (HD) sensors with 54 pF, the corresponding value is 2250 e^-.

To conclude, the design validation criteria for silicon Hex-Modules are defined by two quantitative noise specifications. First, the pedestal noise must remain below the sensor-specific ENC benchmark:

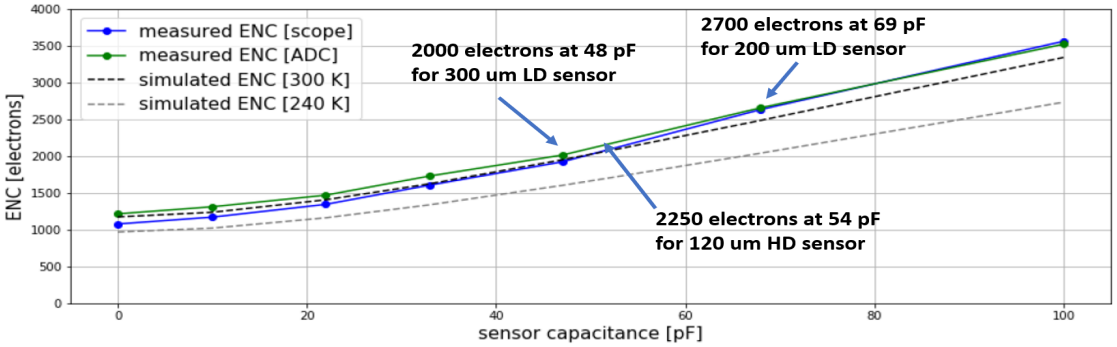


Figure 5.3: ENC (Equivalent Noise Charge) as a function of sensor capacitance at a typical 160 fC ADC gain setting. The benchmarks for the target noise performance are indicated for three silicon sensor thicknesses: approximately 2000 electrons at 48 pF for 300 µm LD sensors, 2700 electrons at 69 pF for 200 µm LD sensors, and 2250 electrons at 54 pF for 120 µm HD sensors. This plot, adapted from [26, 27] and modified from Table 6.1, serves as a benchmark for evaluating the electronic noise performance of the readout system.

2000 e^- for 300 µm LD sensors (48 pF), 2700 e^- for 200 µm LD sensors (69 pF), and 2250 e^- for 120 µm HD sensors (54 pF). Second, the Δ-pedestal—defined as the variation of pedestal with ADC sampling phase—must remain within 10–20 ADC counts, equivalent to approximately 2–4 fC, to meet the required Time-of-Arrival (ToA) threshold of 12 fC. These benchmarks are used as standardized metrics to assess noise performance and to guide iterative improvements in Hexaboard layout, grounding, and shielding strategies.

5.3 Test systems for Hexaboards

This section introduces the test systems utilized for the performance evaluation and characterization of various versions of Hexaboards and their associated silicon Hex-Modules. These test systems are designed to provide power, connectivity, and monitoring capabilities, ensuring compatibility with the Hexaboards and the DAQ system.

The Hexaboard test system primarily comprises two key components: the **Hexacontroller**, a DAQ board based on the Xilinx Trenz System-on-Module (SoM) developed by the Tubutek group; and the **Trophy Board**, an interface board between the Hexaboard and the Hexacontroller, designed and developed by the author. The Trophy Board facilitates power delivery, signal pass-through (including fast commands, clock signals, and slow control commands), and digitization of analog monitoring signals such as DC probe voltages, analog power, digital power, and current drawn by the Hexaboards.

The block diagram of the Trophy Board is shown in figure 5.4. It provides an overview of its functions, including connectivity between the Hexaboard and the Hexacontroller, monitoring of critical signals, and compatibility enhancements.

Trophy Board Variants: Over the course of development, multiple versions of the Trophy Board have been designed to accommodate different iterations of Hexaboards. These are described below:

- **Trophy-V1 and Trophy-V2**: Trophy-V1 was the initial prototype, featuring a four-layer PCB with a narrow neck geometry, implemented to allow probing access to critical test points on the Hexaboard due to layout constraints.To improve signal integrity and provide a more robust mechanical design, Trophy-V2 was designed with an extended rectangular PCB, maintaining electrical compatibility with Trophy-V1.

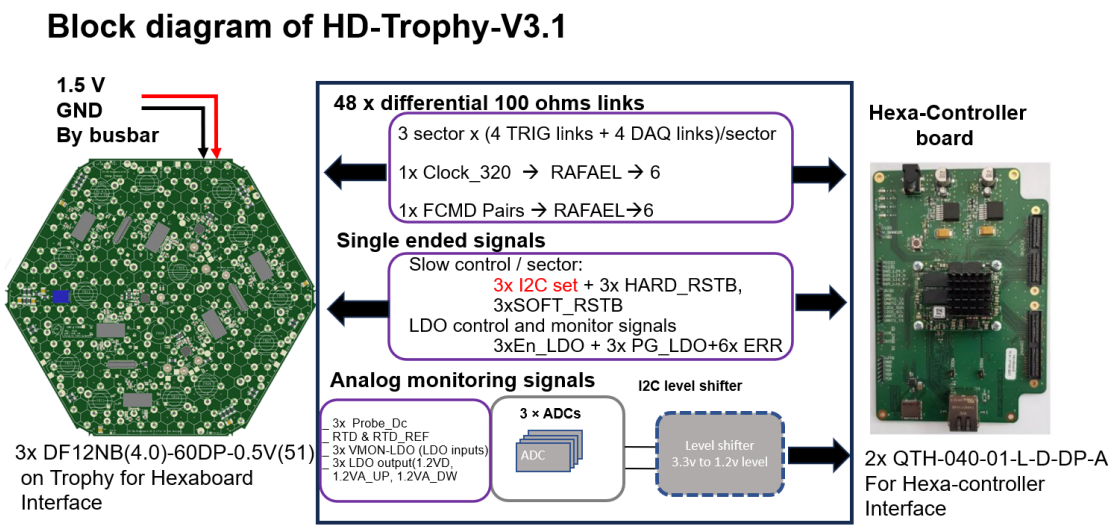
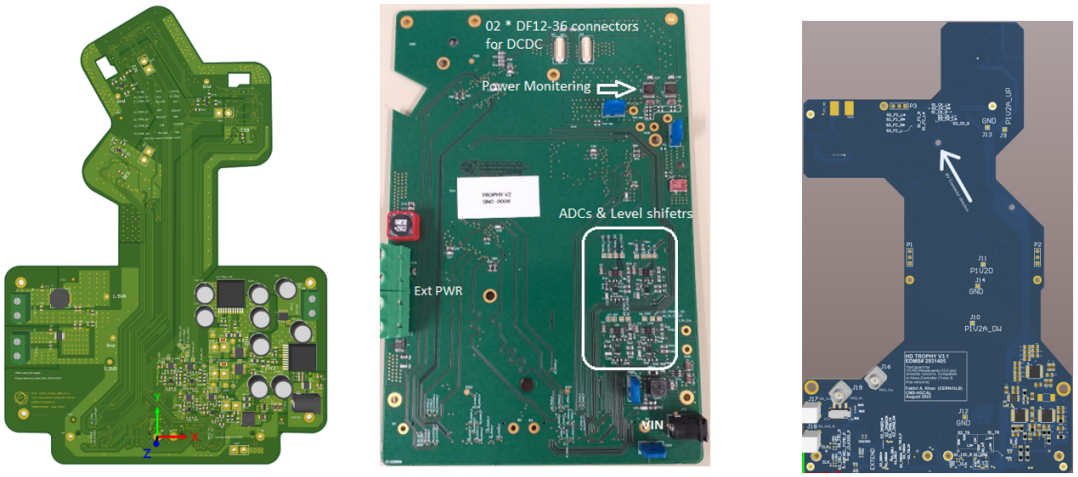


Figure 5.4: Block diagram of the Trophy Board showcasing its role in providing connectivity between the Hexaboard and the DAQ system, along with monitoring and digitization functionalities.



(a):Trophy-V1 for testing Hexaboard Version1 with 4-layers stack-up

(2):Trophy-V2 for testing Hexaboard Version1 with 6-layers stack-up

(C):V3-HD-Trophy-V3.1 for testing V3-HD Hexaboard testing with 6-layers stack-up

Figure 5.5: Evolution of Trophy Boards. (a) Trophy-V1 for Hexaboard V1 with a 4-layer stack-up. (b) Trophy-V2 for Hexaboard V1 with an optimized 6-layer stack-up. (c) HD-Trophy-V3.1 for V3-HD Hexaboard testing with a 6-layer stack-up.

- **LD-Trophy-V3**: Designed by the TUBITEK group as part of the HGCAL collaboration, this version supports the V3-LD Hexaboard.

- **HD-Trophy-V3.1**: Designed specifically for the V3-HD Hexaboard, this variant incorporates additional functionalities such as clock and fast command fanout through Rafael ASICs.

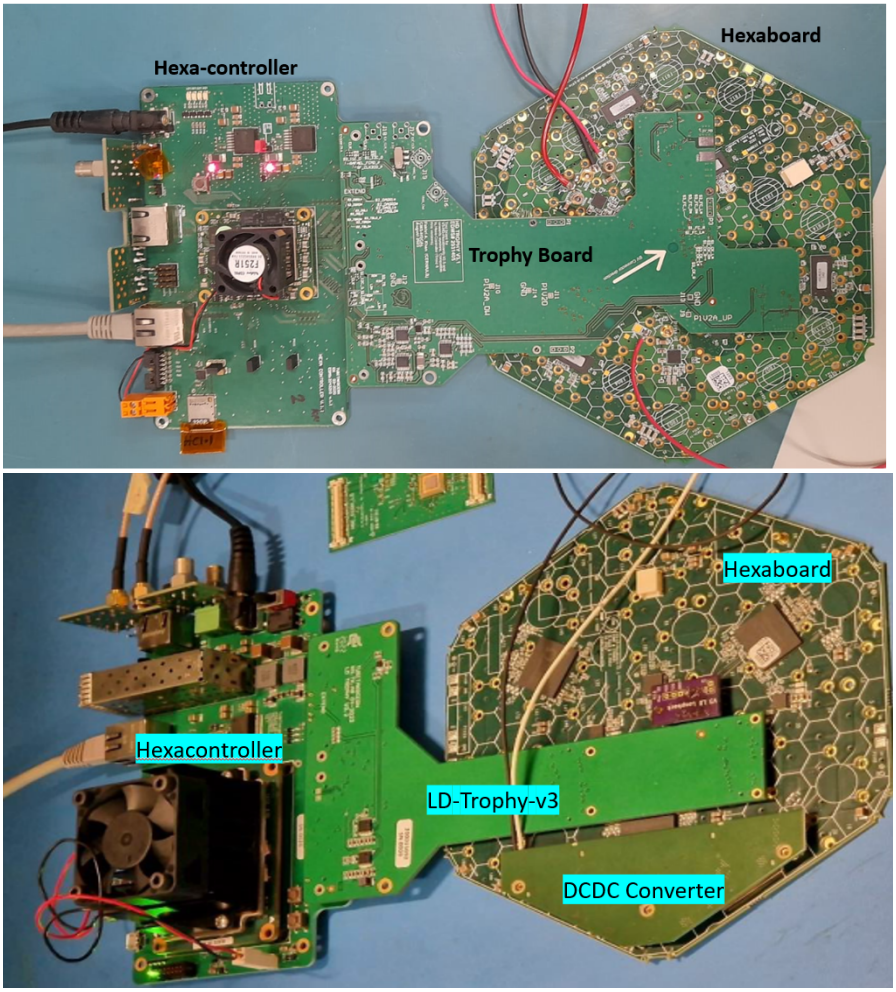


Figure 5.6: Single module test systems for Hexaboards. Top: HD test system comprising the Hexacontroller, HD-Trophy-V3.1, and V3-HD Hexaboard. Bottom: LD test system comprising the Hexacontroller, LD-Trophy-V3, and V3-LD Hexaboard.

The Trophy Boards have evolved in both mechanical and electrical designs to optimize signal integrity, compatibility, and testing efficiency. Figure 5.5 highlights these different versions of Trophy Boards designed for Hexaboard characterization.

Test System Configuration: Figure 5.6 illustrates the test system configurations for HD and LD Hexaboards, known as single module test system. The top panel shows the HD test system comprising the Hexacontroller, HD-Trophy-V3.1, and V3-HD Hexaboard. The bottom panel depicts the LD test system, which includes the Hexacontroller, LD-Trophy-V3, and V3-LD Hexaboard.

This test system framework establishes the foundation for performance evaluations discussed in subsequent sections.

5.4 Design evolution of Low Density Hexaboard to the baseline Scheme

All historical evolution, starting from the 1st prototyping version of LD-Hexaboard-CMS-V1 to the almost final third version, V3-LD-Hexaboard-V1.1 are given in figure 5.7. The initial version, was subsequently followed by an assessment of its performance. This evaluation indicated the need for a second iteration featuring a revised stack-up. The arrival of the new ASIC version, HGCROC-V3 in LD package, prompted the development of a third version. Detailed descriptions of these versions are provided in the subsequent section.

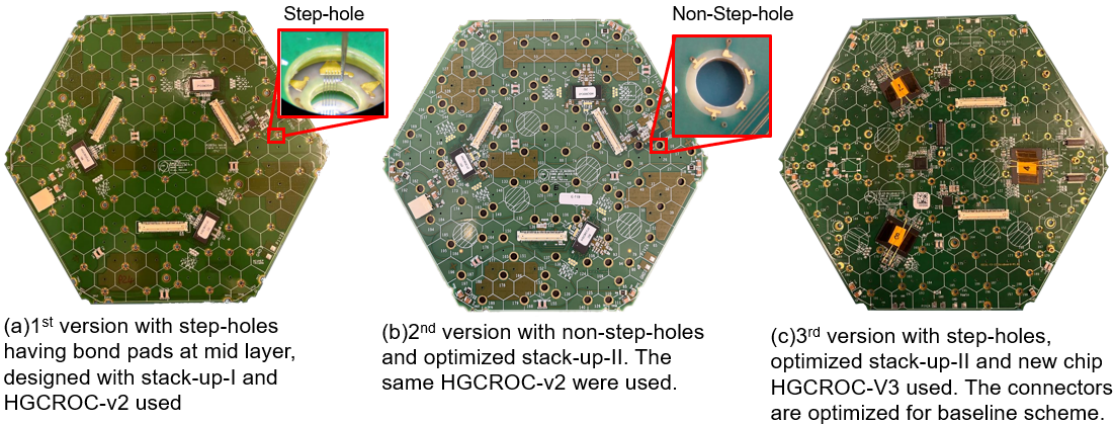


Figure 5.7: Hexaboards across different design iterations. (a) First version with step-holes and mid-layer bond pads, designed with HGROC-v2. (b) Second version featuring non-step-holes and with an optimized stack-up. (c) The final version, designed with HGCROC-V3.

5.5 1st Version of 8” LD Hexaboard

5.5.1 Stack-up inspired from 6” Hexaboard with SKIROC chip

The first version of Hexaboard known as LD-HB-CMS-V1 shown in figure 5.8 (left) used 8-layer stack-up-I shown in figure 5.8 (right). This was the first readout board with the newly designed ASCIS HGCROC-V2. The design was startup with known information from the 6 ” Hexaboard designed with an earlier version HGCROC known as SKIROC-CMS ASIC which was used for the initial proof-of-principle study during the 2016 and 2018 beam tests [102, 103].

The stack-up in figure 5.8 (righ) depicts that the 100 Ω differential signals, 2 DAQ, 4 TRIG links with 1.28 Gb/s and Clock and Fast command with speed of 320 MHz, were routed on layer1 (L1) and L2 and referenced to L3 (VDDD). The sensitive analog channels of HGCROC that bond to the diode pads through stepped-hole structures are routed on L5 and sandwiched between Ground (GND) on L6 and analog supply planes (VDDA) on L4. Analog (VDDA) and digital (VDDD) supplies on L3 and L4 were placed adjacent without any ground plane between them. This version served as an important milestone for HGCAL and the following main goals were achieved:.

- **Streamlining the manufacturing and assembly processes:**
  It was an important step for optimizing the manufacturing, assembly, and module-bonding processes. Due to the step-hole structure, the boards were like a Swiss cheese, so getting the plane board was difficult and tricky. Three manufacturers (2 from Europe and 1 from Asia) were chosen

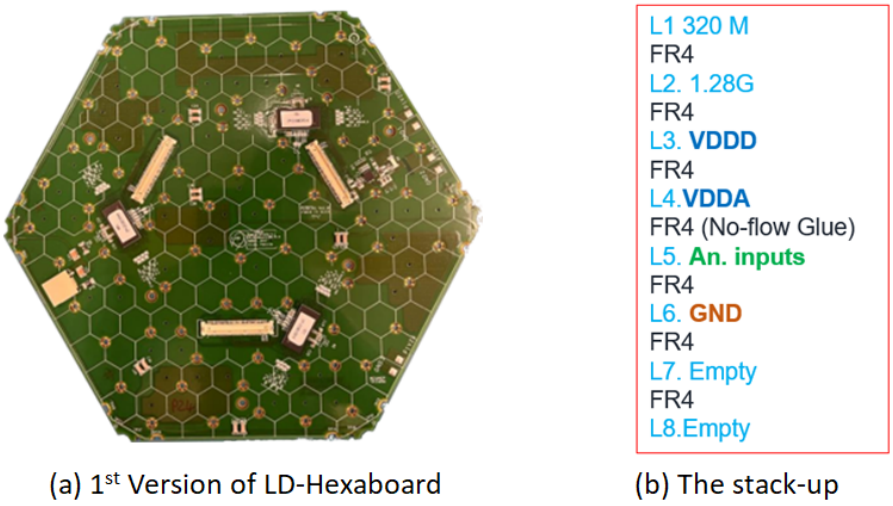


Figure 5.8: The 1^{st} version of LD Hexaboard is shown at left, while the stack incorporated is shown at right

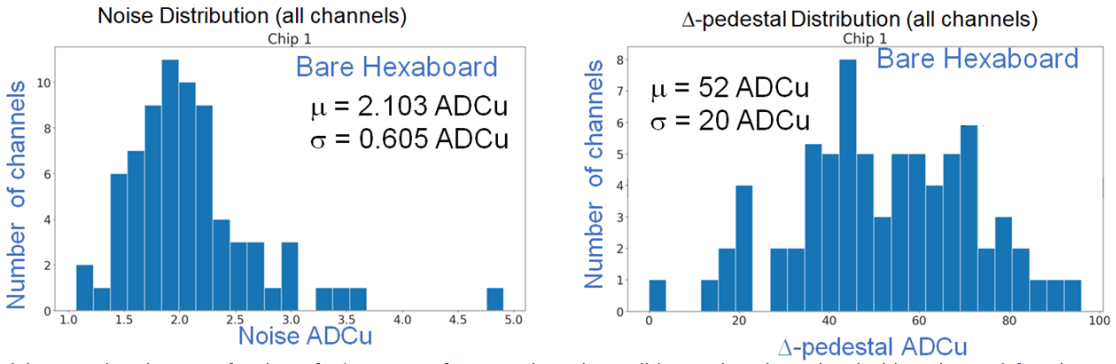
for manufacturing. Due to complex manufacturing and stringent requirements, the initial batch was produced with a very low yield and took $\sim$ 8 months for fabrication. With time, in further batches, each manufacturer was given minor freedom to play a bit with stack-up (without touching some critical layers) to optimize the yield. Much useful feedback was received from manufacturers while fabricating this batch, a few notable suggestions were like adding a teardrop to strengthen the bonding pad connectivity, improving copper balancing, adding a small notch at the end of the bonding pad for testing purposes, and pulling back the copper plane at L5 by 500 µm from step-hole boundary would reduce the glue seepage over bonding pads. All these suggestions were included in the next design. Similarly, this batch was used to find the right assembly house, and all documentation and necessary format files produced for the assembly.

- **Provided a development platform:**
  It provides a development platform for the testing software and firmware for HGCAL DAQ system, used at CERN and in many institutes in HGCAL collaboration

- **Used for silicon Hex-Module procedures and documentation at the Module Assembly Centers (MACs):**
  One of its main uses was the refinement of Module Assembly Center procedures and documentation. The USCB team assembled several silicon Hex-Modules, developed the necessary tooling, software, test procedures, and discovered many unseen constraints that have been included in future designs.

5.5.2 Performance analysis (bare Hexaboard and silicon Hex-Module)

The average noise for the chip was around 2 ADC units, which corresponds to $\sim$2500 e-, but the digital noise amplitude was very high $\sim$ 50 for the bare hexaboard and more than 100 ADC units for the silicon Hex-Module, as shown in figure 5.9 and table 5.1. Due to its high nose and $\Delta - pedestal$ values, it was not very useful for the noise performance study but had many achievements as the prototype, as discussed above.



(a) Noise distribution of a chip of 1st version of LD-Hexaboard (b) Δ-pedestal amplitude (digital noise) for Chip1

Figure 5.9: (a) shows the average noise of a chip, while (b) the $\Delta - pedestal$ is a measure of the amplitude of digital noise for a chip of the 1^{st} version of LD Hexaboard.

5.6 Hexaboard stack-up and performance optimization study

After observing a huge digital noise amplitude in the 1^{st} version, a series of detailed brainstorming sessions held at CERN and performance analysis were performed [104]. A comparative study of all existing HGCROC hosting boards, single ROC characterization board (designed by OMEGA, the ASICs designer group), Si-PM (Silicon photo-multiplier) board (Readout board with same chip for Scintillator region of the HGCAL) of DESY, and Hexaboards was performed. The review culminated in identifying limitations in the current design and proposing recommendations for the next iteration. After a detailed study, the following observations were found:

- *ASICs reference level*: It was found that the stack-up borrowed from 6" hexaboard were optimised for the SKIROC-CMS, which was designed referenced to VDDA levels, while the existing HGCROC is referenced to GND levels.
- *The floating TRIG pins*: It was observed that the TRIG1[L/R], and TRIG2[L/R] were floating. These pins are meant to be used for providing external input signals for the TOA and TOT discriminators calibration in characterization mode and should be connected to GND in the Hexaboard configuration. So this could be one of the reasons for the large noise, as its floating status could trigger TDCs randomly, which could cause digital activity in the chip and increase the noise level.
- *Differentials signals referenced to PWR plane*: All the differential signals (Fast command, clock, TRIG and DAQ) were routed with 100Ω differential impedance with reference to L3 (VDDD), and the Ground plane was very far away at L6. The power plane could be used as a reference, but it should be very close to the GND plane so that any noise coupled from the differential signal to the PWR plane could be grounded easily.
- *VDDD and VDDA adjacent planes*: The digital and analog power planes were placed adjacent to each other as L3 and L4, so any transition that occurs due to large digital activity in the HGCROC, could easily couple from the digital plane to analog plane and subsequently appear or overlap on all analog circuitry and reflect as noise in analog channels.
- *The Analog routing layer lacked shielding*: The analog channels were routed on L5, which is between VDDA (L4) and the ground plane (L6). This means that digital noise that couples from the digital plane to the analog plane could mess up the analog signals even more.

- *Not Enough Ground planes:* It is observed, in comparison with other boards, that there is only one GND plane at L6.

Many stack-up schemes were evaluated to meet the manufacturability and design constraints of the Hexaboard. Among these, Stack-up-II, shown in figure 5.10, was selected as the optimal configuration due to its enhanced design features and compatibility with performance requirements. The key aspects of Stack-up-II are detailed below:

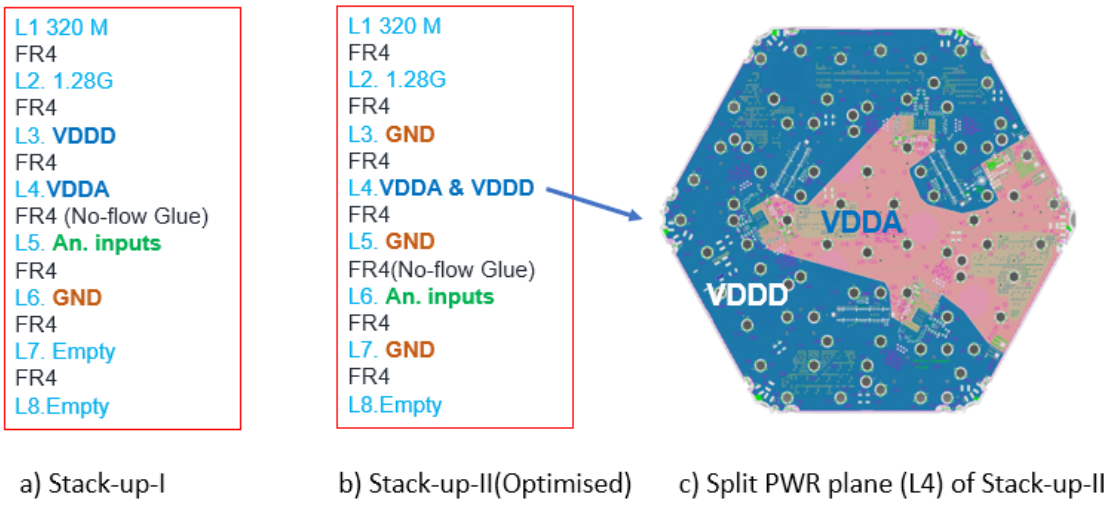


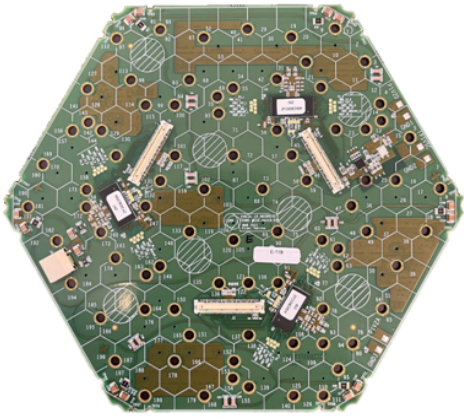
Figure 5.10: Comparison of stack-up configurations used in hexaboard designs: Stack-up-I, implemented in the first version of the hexaboard, was inspired by the earlier 6-inch hexaboard design. Differential routing was referenced to L3 (VDDD), while the bonding pads were placed on L5. Stack-up-II was optimized by including three GND planes, with L3 (GND) serving as the reference plane. Analog channels were routed on L6 with double-sided shielding provided by the adjacent GND layers. The split power plane, shown in (c), was introduced in Stack-up-II to minimize coupling between analog (VDDA) and digital (VDDD) supply planes, with shielding ensured by the surrounding GND layers.

- *Differentials signals referenced to GND plane:* High-speed differential signals, such as Fast Commands and Clock (320 MHz), were routed on L1, while TRIGs and DAQs signals operating at link speeds of 1.28 Gbps were routed on L2. These were referenced to the GND plane on L3, maintaining a 100 Ω differential impedance to ensure signal integrity and reduce crosstalk.
- *Split power plane and multiple ground planes:* L4 was designed as a split power plane, separating VDDA and VDDD to prevent mutual coupling, as illustrated in figure 5.10 (right). To take advantage of inter-plane capacitance, L4 was sandwiched between two ground planes, L3 and L5. A thinner dielectric layer (<100 µm) was chosen between these planes to maximize capacitance for high-frequency noise decoupling, improving overall signal stability.
- *Analog routing shielded between GND planes:* To isolate the analog channels from noise coupling, analog routing was moved to L6. This layer was strategically placed between GND planes on L5 and L7, ensuring effective shielding and noise mitigation.
- *Bottom empty layer:* The bottom layer (L8) was intentionally left empty of any copper connections to electrical components. This reduced parasitic capacitance between the ground planes and the silicon sensor cells, further enhancing signal performance.

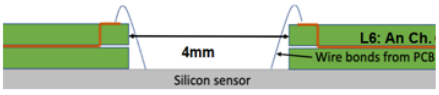
- *Inclusion of PCB design simulations in the design loop:* Given the complexity of the hexaboard and the extended time required for design-to-assembly cycles (which can span up to a year), incorporating advanced simulation tools into the design loop became essential. Sophisticated 3D field solvers and simulation tools such as ANSYS SIWAVE and Cadence Sigrity were recommended. This approach allows for the optimization and validation of the PCB design before the commencement of the manufacturing process, ensuring a more reliable and efficient development cycle.

5.7 Second version of the 8” LD Hexaboard (LD-NSH-HB-V2)

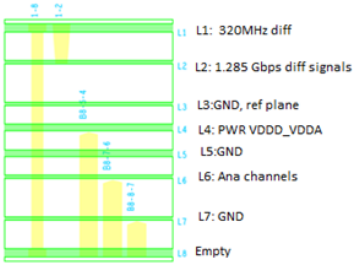
Building on the optimizations detailed in the previous section, the second version of the Hexaboard, designated as LD-NSH-HB-V2, was developed to verify manufacturability and electronics performance using the newly proposed stack-up-II. As the most complex and time-taking part of the manufacturing process is realizing the stepped-hole, these boards were produced with a non-stepped hole (NSH) structure to reduce manufacturing time and evaluate its cost implications.



(a) NSH-LD-Hexaboard-V2.



(b) Non-stepped-hole structure

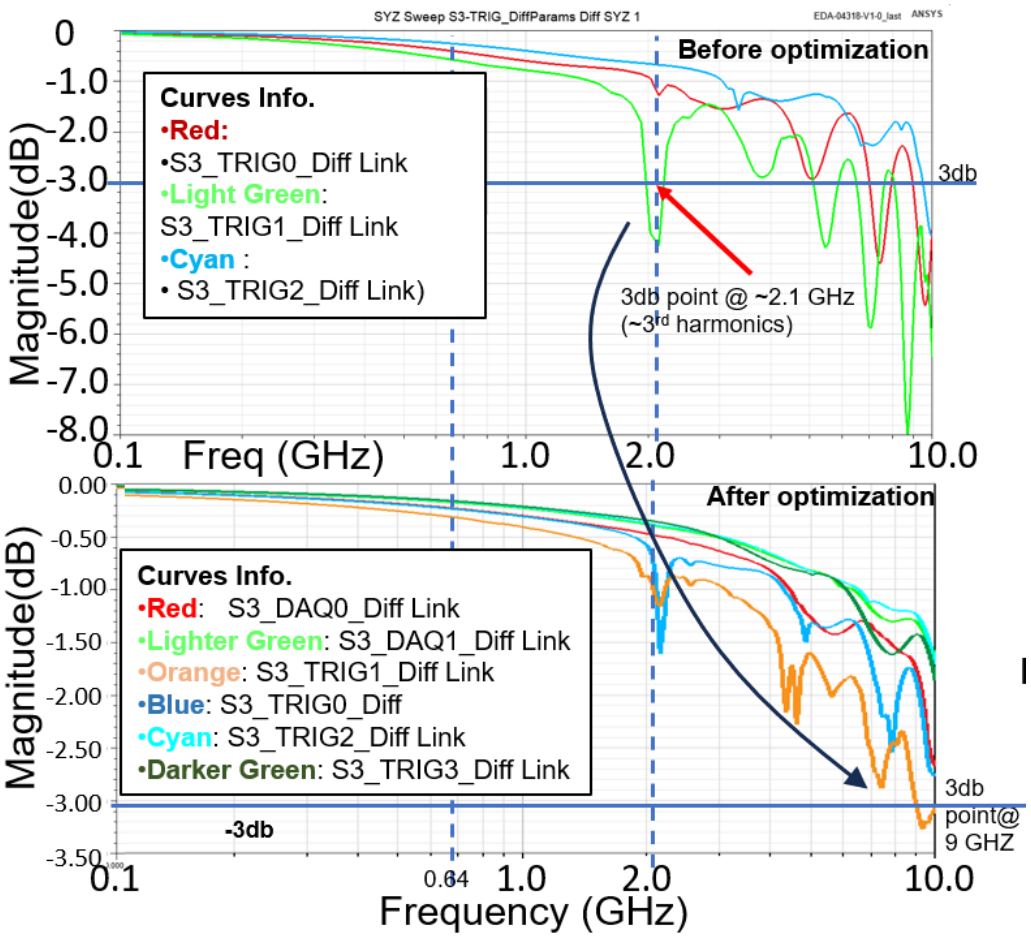


(c) Design X-sectional chart showing stack-up, via and back- drilling scheme used.

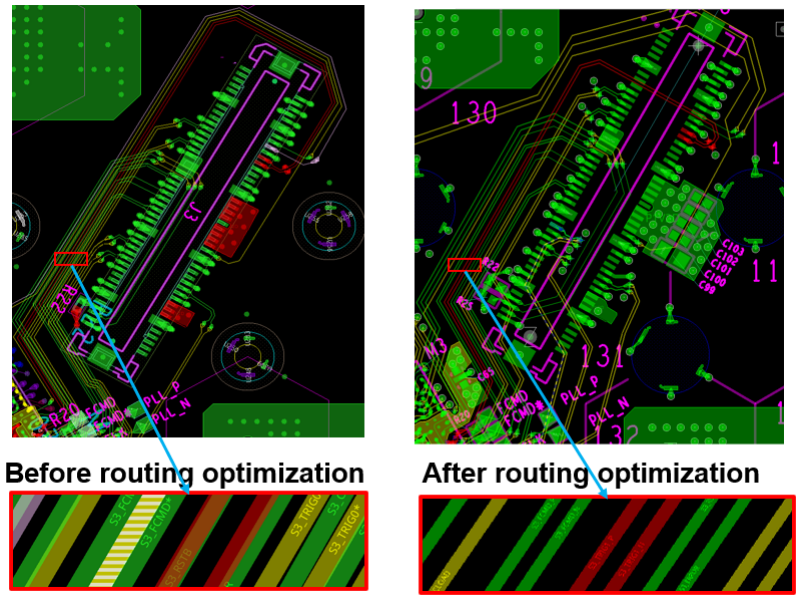
Figure 5.11: (a) NSH-LD-Hexaboard with HGCROC-V2, (b) 4 mm non-stepped hole with bonding pad at L1, and (c) cross-sectional stack-up with via (L1–L8, microvia L1–L2) and three backdrills: B8–8–7 (from L8 to L8 and must not cut L7), B8–7–6, B8–5–4. L1/L2 route 320 MHz and 1.28 Gbps signals referenced to L3. L4 carries split power (VDDD/VDDA), L6 hosts analog lines shielded by L5/L7, and L8 is left empty to reduce capacitance.

Figure 5.11(a) shows the second version of the Hexaboard, referred to as the NSH-LD-Hexaboard, assembled with HGCROC-V2. Figure 5.11(b) illustrates the 4 mm non-stepped hole design, where bonding pads are located on L1 and connected to analog routing on L6 via a plated through-hole (PTH). The 8-layer stack-up cross-section shown in Figure 5.11(c) incorporates a through-hole via (L1–L8), a microvia (L1–L2), and three backdrilling schemes: B8–8–7 (from L8 to L8, must not cut L7), B8–7–6, and B8–5–4. This layout routes high-speed differential signals on L1 and L2 (320 MHz and 1.28 Gbps), referenced to L3 Ground plane. L4 carries split power (VDDD/VDDA), while L6 is dedicated to sensitive analog signals, shielded by ground planes L5 and L7. L8 is intentionally left empty to minimize capacitive coupling to the sensor.

The LD-NSH-HB-V2 utilized the optimized stack-up-II described earlier, which had already demonstrated improved electrical and mechanical aspects. The key features of this version include:



(a) S-parameters (insertion loss) extracted before and after optimization.



(b) PCB layout and zoomed-in views illustrating routing adjustments.

Figure 5.12: (a) S-parameter (insertion loss) measurements before and after routing optimization, showing a shift of the 3 dB point from 2.1 GHz to 9 GHz, indicating improved link quality. (b) PCB layout and zoomed-in views illustrating the routing optimisation, where differential traces were staggered across L1 and L2 to minimize capacitive coupling and enhance signal integrity.

- **Retention of the stack-up-II configuration:** Ensures better grounding, utilising ground plan as refrence for all differential routing, effective shielding for analog signals and minimizes coupling between VDDA and VDDD planes.

- **Analog signal routing on L6:** Sensitive analog signals are routed on L6, benefiting from the double-shielding provided by adjacent ground planes on L5 and L7.

- **Enhanced inter-plane capacitance:** A thin 100 µm dielectric layer between L3 (GND) and L4 (power plane) increases inter-plane capacitance, aiding high-frequency noise decoupling.

This design was optimized and validated through multiple cycles of PCB simulation using Ansys SIWAVE for power integrity and signal integrity analyses.

5.7.1 Design validation through simulation

To ensure the design's robustness before fabrication, the Hexaboard design underwent rigorous validation using Ansys SIWAVE PCB simulation tools. These simulations incorporated several key scans and optimization steps (refer to chapters 12 and 13 of [105] for details), which are summarized below:

- **Power Integrity:** Power distribution network (PDN) analysis and target impedance control were employed to optimize the decoupling scheme and minimize noise on power planes.

- **IR-Drop Analysis:** IR-drop scans identified any abnormal voltage drops or current congestion across the PCB, ensuring consistent power delivery to all components.

- **Signal Integrity:** Impedance scans were performed to detect discontinuities in the 100 Ω differential routing, which could lead to signal reflections and degrade performance.

- **Insertion Loss Analysis:** S-parameters were extracted to validate the quality of differential links. The 3 dB cutoff frequency (where signal power drops to half) was verified to ensure it lies at least five harmonics beyond the operating frequency.

An example of the optimization process is shown in figure 5.12. In figure 5.12 (a), the S-parameters (insertion loss) are shown before and after optimization. Prior to optimization, the S3-TRIG0 link (green curve) exhibited a 3 dB point at approximately 2.1 GHz, close to the third harmonic of the operating frequency (640 MHz). To address this, the routing above the affected link was modified, and the insertion loss was re-evaluated. After optimization, the S3-TRIG0 link (orange curve) demonstrated a significant improvement, with the 3 dB point shifting to 9 GHz, well beyond the target range.

The PCB layout before and after the routing optimization is presented in figure 5.12 (b). In the zoomed-in view before optimization, the critical link S3-TRIG0 is highlighted in red on L2, alongside two adjacent yellow traces also routed on L2. On L1, the differential pair routing (shown in green) was positioned directly above or partially overlapping the L2 traces, resulting in increased capacitive coupling and elevated insertion losses. To mitigate these effects, the routing was optimized by staggering the differential traces across L1 and L2, thereby avoiding exact overlap. This staggered configuration improved impedance matching and significantly reduced insertion losses, consistent with the improvements observed in the S-parameters.

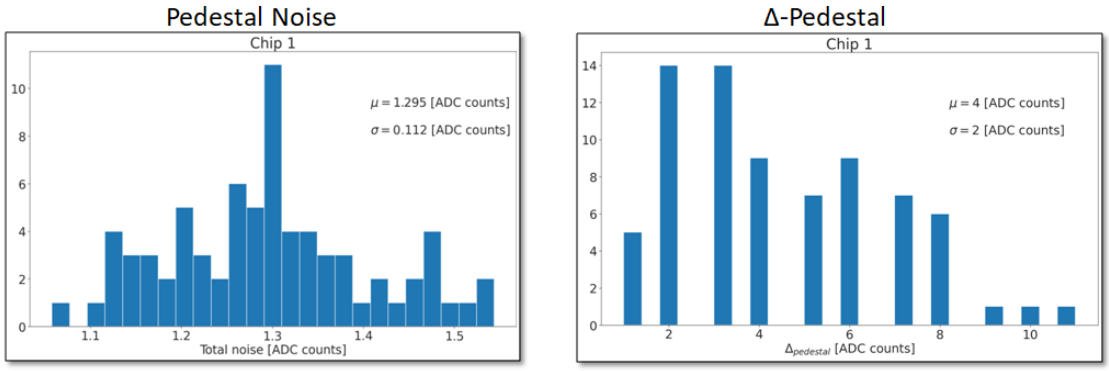
This iterative optimization approach ensures that the PCB design meets the required performance specifications while minimizing potential issues during fabrication and operation.

5.7.2 Performance analysis (bare Hexaboard and silicon Hex-Module)

The LD-NSH-Hexaboard-V2 was produced in a batch of approximately 100 boards, fabricated by three different manufacturers. These boards were assembled with HGCROC-V2 chips and subsequently tested to evaluate their performance.

Figure 5.13 summarizes the key results. The average noise per chip was measured to be approximately 1.3 ADC units, while the Δ-pedestal, a metric of digital modulation, was reduced to 4 ADC units. These values demonstrate a significant improvement over previous versions.

A detailed comparison with other Hexaboard versions is provided in figure 5.16 and Table 5.1 in section 5.8.2. The results highlight a more than 10-fold reduction in digital modulation compared to earlier iterations, underscoring the effectiveness of the design optimizations implemented in the LD-NSH-Hexaboard-V2.



(a) Pedestal Noise distribution of HGCROC Assembled on NHS-LD-Hexaboard

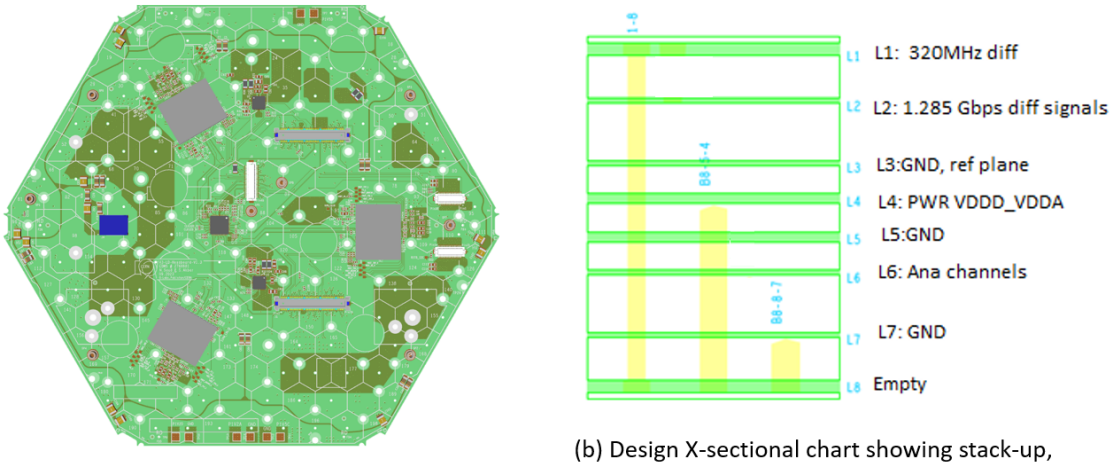
(b) Δ-Pedestal distribution of HGCROC Assembled on NHS-LD-Hexaboard

Figure 5.13: (a) Pedestal noise distribution of HGCROC assembled on the 2^{nd} version, NHS-LD-Hexaboard, showing an average noise (μ) of 1.295 ADC units with a standard deviation (σ) of 0.112 ADC units. (b) Δ-Pedestal distribution for the same board, indicating an average digital noise amplitude (μ) of 4 ADC units with a standard deviation (σ) of 2 ADC units.

5.8 3^{rd} Version of 8" LD Hexaboard (V3-LD-Hexaboard)

The third version of the LD Hexaboard, V3-LD-Hexaboard-V1.x (x = 1, 2, 3) shown in figure 5.14, was designed on the arrival of the new version of ASIC, HGCROC-V3 in the Low Density (LD) package. The main motive for HGCROC being in the LD package was to have ASIC with a bigger pitch (0.8 mm) to reduce the manufacturing complexity and production cost as well as to improve the yield for the LD-Hexaboard, which is almost $\sim$ 80% of the whole production [27]. It has used the same stack-II used in NSH-LD-Hexaboard. So far, three sub-versions for minor modifications of V3-LD-Hexaboard have been produced. The V3-LD-Hexaboard-V1.3, shown in figure 5.14 (left), is the on-cassette version. It is compliant with all on-detector constraints listed in the section 4.4. A few of these constraints include stepped holes, multiple interface connectors for the local DC-DC converter, concentrator mezzanine and wagon board, as well as mechanical mounting points for many connecting boards.

A passage for service routing through the cassettes is also managed by avoiding putting any tall components in a specific corridor, and many constraint regions left empty for the pick-up tools, engine



(a) V-LD-Hexaboard-V1.3

(b) Design X-sectional chart showing stack-up, via and back- drilling scheme used.

Figure 5.14: (Left): Final version, V3-LD-Hexaboard-V1.3. (Right): Stack-up II cross-section showing an L1–L8 thru-hole via and two backdrills: B8–5–4 (to L5, must not cut L4) and B8–8–7 (to L8, must not cut L7). L1 and L2 route 320 MHz and 1.285 Gbps differential signals referenced to L3. L3, L5, and L7 are ground planes; L6 hosts analog channels shielded by L5 and L7. L4 carries power (VDDD/VDDA), and L8 is left empty to reduce capacitance to the sensor.

boards, and DCDC shields. There are 7×no-go areas kept for pick and place tools and vacuum cups. Although the Hexaboard don't have direct connection with LD / HD engines, it takes up much of its space because we have to keep the area specified for LD/HD engines components free, as there will be only 0.7 mm gap between Hexaboard and Engine boards. In addition to the three HGCROCs, the PCB included Rafael ASICs for clock and fast command fan-out, and LDOs for on-detector point-of-load power regulation [106]. Multiple silicon Hex-Modules are assembled with this version of the board. The bare Hexaboard and Hex-module exhibit measured performance very close to the final specification (see section 5.8.2).

5.8.1 Design and stack-up

The final production stack-up is illustrated in figure 5.14, (right) which shows an 8-layer stack-up based on the optimized stack-up-II configuration shown in figure 5.10 (b). This configuration incorporates several key modifications to improve manufacturability and performance.

To accommodate the relaxed 0.8 mm pitch of the BGA package, a fan-out design with PTH vias was implemented, maintaining a drill-to-pad ratio of 200 µm / 500 µm. Originally, multiple back-drill sets were planned to remove stubs from all vias for each layer. However, initial production phases revealed that the back-drill depth in the Back-drill set B8–3–2 (Back drill from L8 to L3, must not cut L2) adversely affected the flatness and production yield. In response, the design was refined to include only two back-drill sets: Back-drill set B8–5–4 to remove stubs from all high-speed 1.28 Gbps and 320 MHz signals, and Back-drill set B8–8–7 to remove copper from remaining vias connected to analog channels and the ground net, effectively isolating L8 from all copper connections to any electrical net.

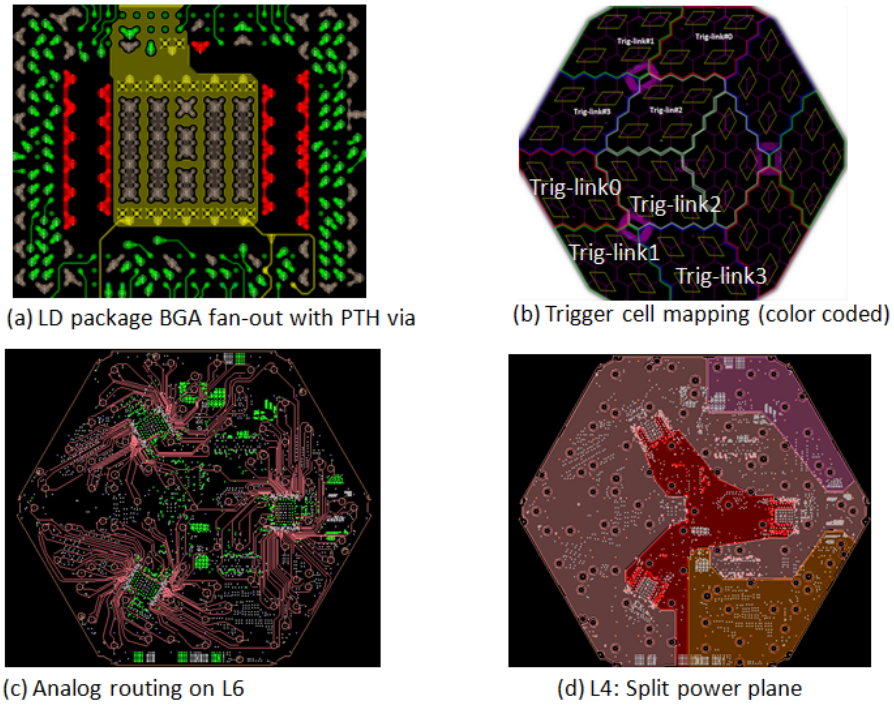
Several design features of the final version, V3-LD-Hexaboard-V1.3, are depicted in figure 5.15. These include:

- **BGA Fan-Out:** Figure 5.15 (a) illustrates the fan-out scheme for the BGA package using PTH

vias.

- **Trigger Cell Mapping:** Figure 5.15 (b) shows the grouping of silicon Hexaboard cells into trigger primitives, represented with color-coded regions.
- **Analog Routing on Layer 6:** Figure 5.15 (c) highlights the routing of sensitive analog channels on L6.
- **Split Power Planes on Layer 4:** Figure 5.15 (d) displays L4, featuring multiple split power planes differentiated by color to minimize coupling between VDDA and VDDD.

This optimized stack-up and design layout ensure improved performance, manufacturability, and signal and power integrity for the V3-LD-Hexaboard-V1.3.



(a) LD package BGA fan-out with PTH via

(b) Trigger cell mapping (color coded)

(c) Analog routing on L6

(d) L4: Split power plane

Figure 5.15: The final version, V3-LD-Hexaboard-V1.3, shows key design features: (a) BGA fan-out with PTH vias, (b) trigger cell mapping (color-coded), (c) analog routing on L6, and (d) split power planes on L4.

5.8.2 Comparitive performance analysis of bare Hexaboards and assembled silicon Hex-Modules

The performance evolution of the three iterations of LD Hexaboards and their corresponding silicon Hex-Modules is illustrated in figures 5.16 and 5.17, with a detailed numerical comparison provided in Table 5.1. The results demonstrate a systematic progression in noise reduction and Δ-pedestal minimization, culminating in the V3-LD-Hexaboard and its corresponding module, which meet the HGCAL TDR [6] noise requirements and the ENC benchmark, as shown in figure 5.3.

Figure 5.16 presents a comparative analysis of pedestal noise and Δ-pedestal values for the three iterations of LD Hexaboards. The data illustrate a consistent reduction in both parameters across successive versions, attributable to improvements in PCB stack-up, optimized grounding schemes, and enhanced component integration. The V3-LD-Hexaboard achieves the lowest noise and Δ-pedestal values, establishing its suitability for precision calorimeter readout.

Similarly, Figure 5.17 compares the performance of silicon Hex-Modules assembled with the V2-NSH-Hexaboard and V3-LD-Hexaboard. The V3-LD-Module exhibits a noise level of approximately 1.3 ADC units and a Δ-pedestal of ∼4 ADC units (biased by zero channels, with the actual value being 7 ADC units), significantly outperforming the NSH-Module, which records ∼2.3 ADC units in noise and ∼19 ADC units in Δ-pedestal. These results confirm the noise stability and reduced digital modulation in the V3-LD-Module, underscoring the impact of refined PCB design and grounding optimizations.

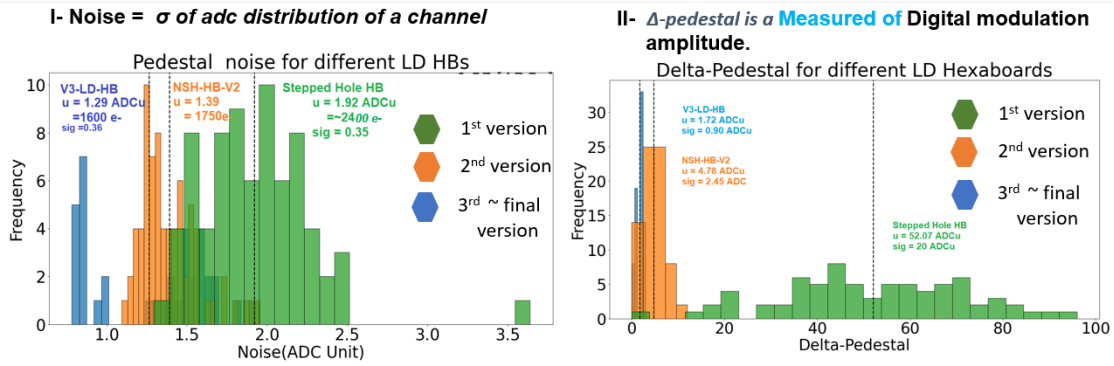
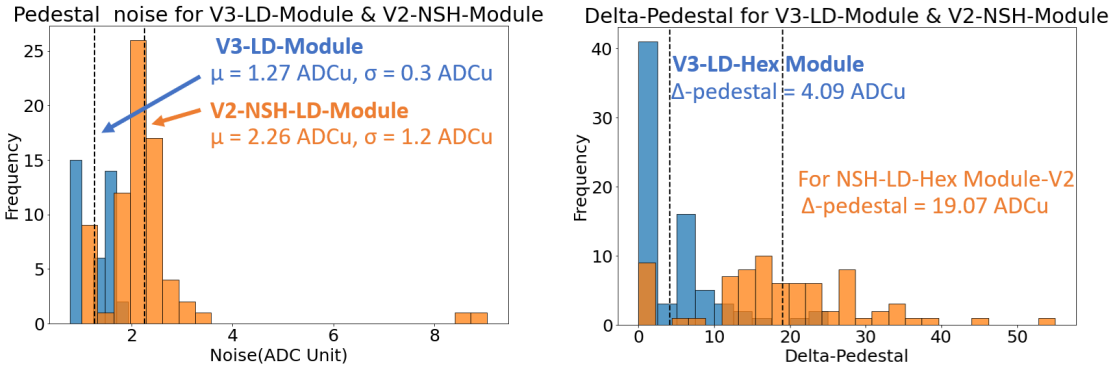


Figure 5.16: Comparison of pedestal noise (σ of ADC distribution) and digital modulation amplitude (Δ-pedestal) for all versions of LD Hexaboards. The plots demonstrate progressive performance enhancements, culminating in the reduced noise and Δ-pedestal of the final version (V3-LD-HB).



(a) Pedestal Noise comparison of chip2 for V3-LD-Module and V2-NHS-LD-Module

(b) Δ-Pedestal comparison of chip2 for V3-LD-Module and V2-NHS-LD-Module

Figure 5.17: Comparison of pedestal noise (σ of ADC distribution) and digital modulation amplitude (Δ-pedestal) for silicon Hex-Modules assembled with NSH-LD-Hexaboard and V3-LD-Hexaboard. The results highlight significant improvements in noise and modulation stability in the V3-LD-Module.

The performance metrics in Table 5.1 further substantiate the improvements achieved across iterations. The LD-HB-CMS-V1, with an average noise of 2.1 ADC units and a Δ-pedestal of 52 ADC units,

Table 5.1: Comparison of all three Hexaboard versions and their corresponding silicon Hex-Modules, adapted from [107].

Hexaboard Type	Noise (ADC units)	S/N (MIP/Noise)	Δ-pedestal (ADC units)
LD-HB-CMS-V1	2.1	-	52
LD-Hex-Module-V1	$\sim$ 50	<1	>100
LD-NSH-HB-V2	1.3	-	4
LD-Hex-Module-V2	2.4	7	17
V3-LD-HB	1.0	-	1.43
LD-Hex-Module-V3	1.5	11	$\sim$9

exhibited severe limitations when assembled into LD-Hex-Module-V1, where the noise increased to $\sim$50 ADC units, the S/N ratio dropped below 1, and the Δ-pedestal exceeded 100 ADC units. These values significantly deviated from the HGCAL TDR target of 2000 electrons for a 47 pF sensor capacitance.

The LD-NSH-HB-V2 introduced significant improvements, with noise reduced to 1.3 ADC units, while the module (LD-Hex-Module-V2) exhibited a noise level of 2.4 ADC units, an S/N ratio of 7, and a Δ-pedestal of 17-19 ADC units. Despite improved noise performance, the relatively high Δ-pedestal remained a limiting factor in achieving the required TOA threshold of 12 fC.

The final version, V3-LD-HB, achieved the lowest recorded noise of 1.0 ADC units, and when assembled into V3-LD-Hex-Module, the noise marginally increased to 1.3-1.5 ADC units (1900 electrons), while the Δ-pedestal further dropped to $\sim$7-9 ADC units (0.5 MIP). These values align well with the HGCAL TDR noise specification of 2000 electrons, reinforcing the suitability of this version for high-precision detector applications. The S/N ratio improved to 11, ensuring robust signal integrity and minimal digital modulation.

The results presented in figures 5.16 and 5.17, along with Table 5.1, depict a clear trajectory of iterative optimization. The transition from LD-HB-CMS-V1, which exhibited excessive noise and instability, to the V3-LD-Hexaboard, which meets stringent HGCAL requirements, highlights the effectiveness of progressive design refinements. The final iteration achieves an optimal balance between low noise, high signal integrity, and minimal digital modulation, ensuring reliable performance under HL-LHC operational conditions.

5.9 Design evolution of High Density Hexaboard to the baseline Scheme

This section outlines the evaluation and performance study of the high-density (HD) Hexaboards, detailing the development journey from the first version to the final V3-HD-Hexaboard. The discussion includes the pros and cons of the first version, the debugging process to address high digital modulation issue, and the resulting improvements in the final version.

5.10 1^{st} Version of 8 ” HD-Hexaboard

The first version of the HD-Hexaboard, shown in figure 5.18, was designed to integrate six HGCROC-V2 chips to read out 432 silicon diode pads. As the initial versions of both LD and HD Hexaboards were developed concurrently, they shared the same stack-up design, which was originally adapted from the 6 ” Hexaboard. Additionally, both versions employed identical BGA fan-out schemes for the HGCROC-V2 chips. Consequently, the HD-Hexaboard faced similar design challenges as the first LD-Hexaboard, as

detailed in Section 5.6.

However, the HD-Hexaboard's design posed additional complexities. With six HGCROC-V2 chips tasked with reading more than twice the number of cells compared to its LD counterpart within the same physical area, the design required a significantly higher density of step-holes to connect with the 432 cells. This increased density led to a porous power plane, which adversely affected the power distribution's integrity. Furthermore, the high density of step-holes introduced challenges in maintaining board flatness due to uneven copper distribution, resulting in additional complexity in the manufacturing process.

To address these challenges, approximately 20 prototypes of the first HD-Hexaboard were produced to refine the manufacturing techniques. Several of these prototypes were equipped with HD silicon sensors to conduct functional tests of the module assembly processes and to carry out a preliminary assessment of module performance. Similar to the first version of the LD-Hexaboard, the HD prototypes exhibited sub-optimal electrical performance, with significant noise and digital modulation issues observed during testing. Despite these limitations, the prototypes proved valuable for advancing manufacturing processes, board assembly, and module assembly techniques. They also played a crucial role in the development of software and firmware for the HGCROC.

Given the challenges encountered, further prototyping of the HD version was temporarily paused, and with focus shifted to refining the LD design. Once the optimized design was established with the LD version, the development and prototyping of the HD version resumed, incorporating these design remedies to achieve the desired performance metrics.

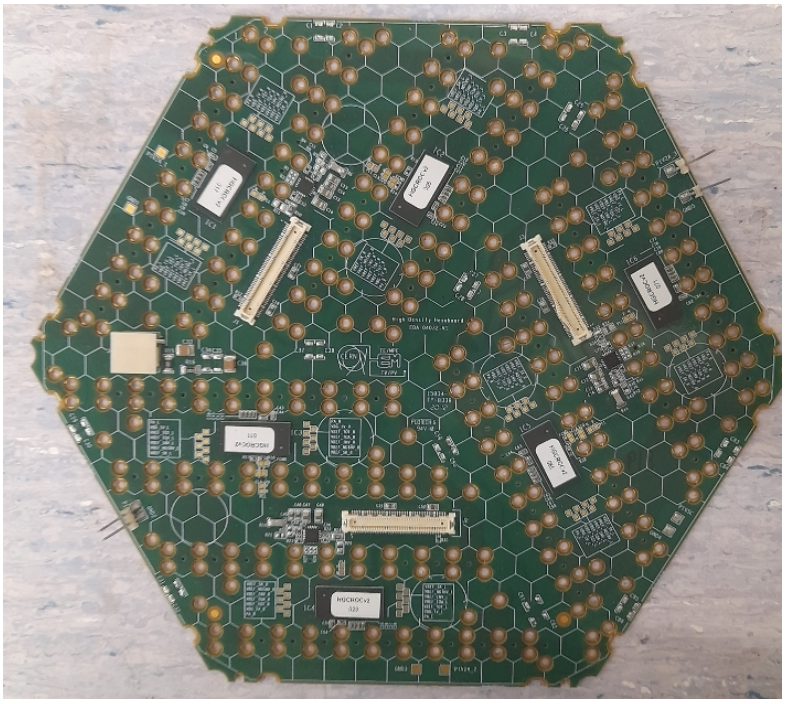


Figure 5.18: First version of the HD Hexaboard assembled with HGCROC-V2.

5.11 Debugging the large digital modulation amplitude in the designs with 0.6 mm BGA package

This part discuss the debug of large Δ-pedestal in the HD HGCROC package, which effectivly impact all the futre design of Hexaboards and packaging scheme of HGCROC.

The October 2021 SPS beam test (section 6.3) was primarily conducted with silicon Hex-Modules assembled with NSH-LD-Hexaboard-V2. During this period, a new version of the ASIC, the HGCROC-V3, became available, featuring the same pinout and package as HGCROC-V2. To study its performance, a silicon Hex-Module assembled with NSH-LD-Hexaboard-V3 was also tested under identical conditions. Surprisingly, a significant difference was observed between the two modules, despite being assembled with the same Hexaboard but incorporating different versions of the chip.

		Noise	Δ-pedestal
HGCROC-V2	NSH-Hexaboard	~ 1	4
	Hex-module-V2	$2.5 - 3$	~ 17
HGCROC-V3	NSH-Hexaboard	~ 1	16
	Hex-module-V3	> 2.5	> 170

Table 5.2: Comparison of noise and Δ-pedestal between NSH-Hexaboard and modules assembled with HGCROC-V2 and HGCROC-V3.

Table 5.2 highlights the noise and Δ-pedestal values for the NSH-Hexaboards and silicon Hex-Modules equipped with different ASIC versions. It is evident that the silicon Hex-Module read out by HGCROC-V3 exhibited a nearly ten times increase in digital modulation compared to the module assembled with HGCROC-V2.

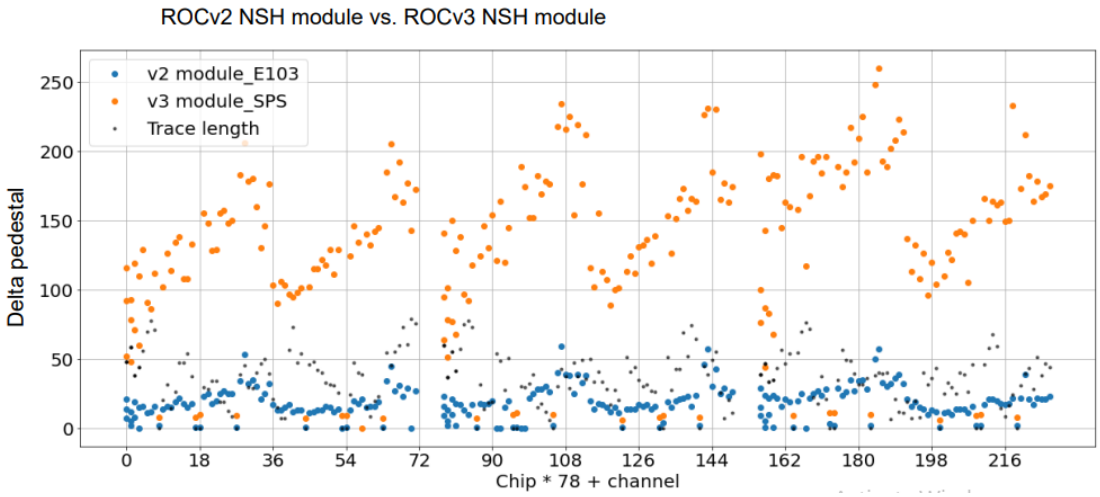


Figure 5.19: Δ-pedestal comparison between NSH-Hex Modules assembled with HGCROC-V2 (blue) and HGCROC-V3 (orange). A seesaw pattern in Δ-pedestal amplitude, repeating every 36 pins (half-chip), indicates that the effect increases from pin 1 to pin 36 in each half.

This initiated a comprehensive series of investigations to identify the root cause of the increased digital modulation. The findings revealed that the modulation was independent of both the number of active chips and the number of active channels on the Hexaboard. Instead, it exhibited a strong correlation

with the input capacitance value. Furthermore, a distinct channel-wise top-to-bottom trend was observed in the Δ-pedestal values, as illustrated in figure 5.19, where the modulation followed a seesaw pattern, increasing progressively with the channel number.

Further investigations revealed that the primary difference between HGCROC-V2 and HGCROC-V3 was the ground configuration within the package at the substrate level. Figure 5.20 illustrates this difference across three aspects: the substrate ground configuration (a), the BGA routing for the NSH-Hexaboard (b), and the block diagram for ground connectivity in Hexaboard-V2 and Hexaboard-V3 (c).

In HGCROC-V2, the ground plane within the package is split into two distinct regions: Analog Ground (AGND) and Digital Ground (DGND), as shown in figure 5.20 (a). The DGND pins are centrally located within the package and grouped in sets of four, allowing for efficient connection to the Hexaboard ground plane using PTH vias with a drill-pad ratio of 200 um/500 um. These connections ensure a robust grounding scheme for digital return currents. Conversely, the AGND pins are arranged in vertical columns and, the space limitations within the BGA region make it impractical to implement PTH vias for AGND connections. Instead, micro-vias with a smaller drill-pad ratio of 150 um/350 um are used to connect these pins to a sub-ground plane on L2. This sub-ground plane is then connected to the Hexaboard's main ground planes (L3, L5, L7) via PTH vias placed outside the congested BGA region.

To maintain a common ground across the Hexaboard, AGND and DGND are linked by a small connection on the top layer, as indicated by the arrow in figure 5.20 (b). However, this link introduces design challenges. Digital currents (I_d), primarily oscillating at the fundamental clock frequency of 40 MHz, flow through multiple PTH vias into the ground planes (L3, L5, and L7). In contrast, analog return currents (I_a), which are largely DC or low-frequency currents, pass through a combination of micro-vias and PTH vias. Due to the limited space within the BGA region, only one PTH via per half was allocated for analog return currents. This suboptimal allocation caused impedance in the analog return path, forcing a portion of I_a to mix with the digital return currents. The resulting interference introduced 40 MHz oscillations into the analog ground, which serves as a reference for the pre-amplifier. Consequently, these oscillations were amplified by the pre-amplifier and coupled into the analog input channels, leading to increased digital modulation.

The HGCROC-V3 employs a unified ground configuration at the substrate level, as shown in figure 5.20 (c) (left), the AGND and DGND regions are internally connected by GND plane within the package, providing a low impedenace parallel path to the small link on top layer, causes significant mixing of analog and digital return currents at the package level. This mixing results in a tenfold increase in digital modulation observed in the associated silicon Hex-Module as shwon in table 5.2.

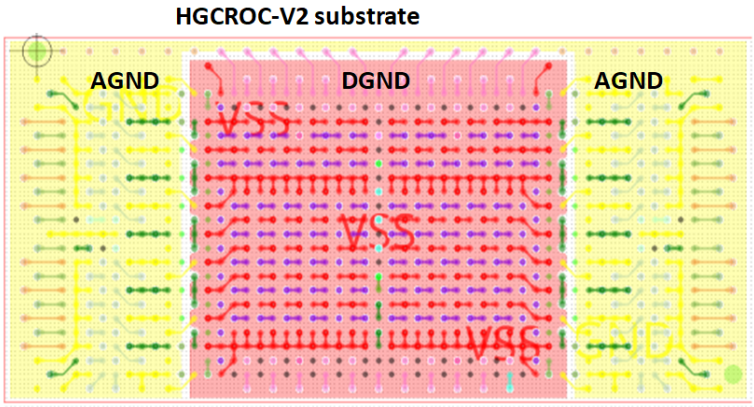
To validate the assumption that any connection between the return paths (either within the package or on the Hexaboard routing layers) prior to their convergence on the low-impedance ground planes of the Hexaboard contributes to increased digital modulation, an experiment was conducted using the NSH-Hexaboard-V2.

In this experiment, the small link on the top layer of the Hexaboard, which connected the AGND and DGND paths, was removed, and the board was assembled with HGCROC-V2. With the link removed, the only connection between the return paths occurred on L3, the primary ground plane of the Hexaboard. The Δ-pedestal values were measured before and after breaking the link. The results showed an average fourfold reduction in Δ-pedestal values, as depicted in figure 5.21.

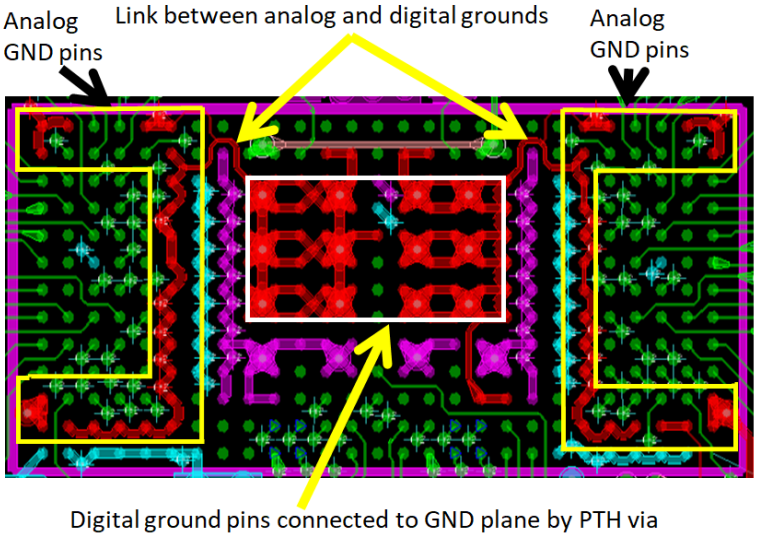
This result marked a significant breakthrough in the design of Hexaboards, particularly for the high-density (HD) version utilizing the HD package of HGCROC. It highlighted the critical impact of return path design on digital modulation and laid the foundation for a set of design guidelines aimed at optimizing performance in future Hexaboard iterations.

Design Guidelines for Future Hexaboards:
Based on the findings of this experiment, the following recommendations were established for all future designs:

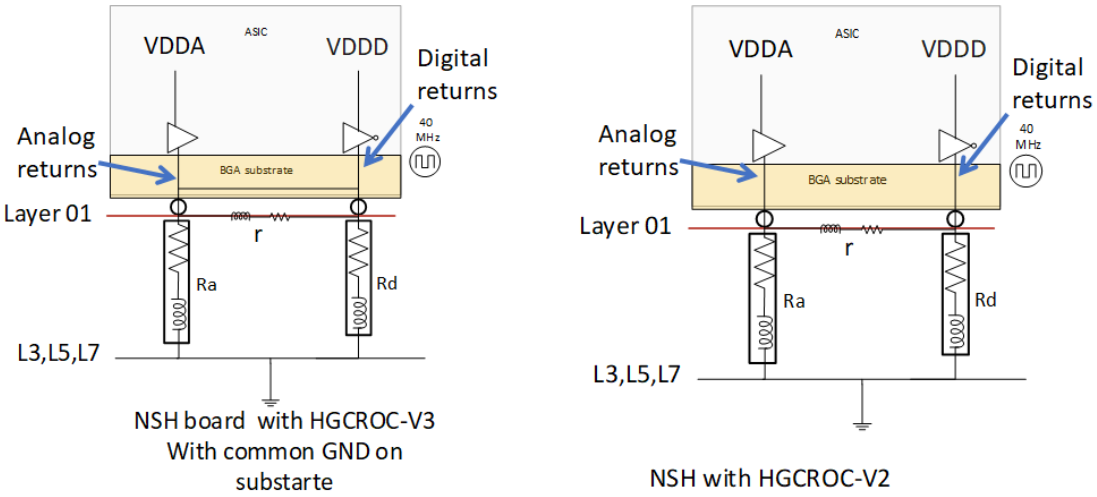
- **Avoid Mixing of Return Currents:** To minimize interference between analog and digital circuits,



(a) Ground plane configuration in HGCROC-V2. AGND and DGND are separated within the substrate.



(b) BGA routing for NSH-Hexaboard. Red areas indicate ground connections.



(c) Block diagram showing ground connectivity for NSH-Hexaboard-V2 and NSH-Hexaboard-V3.

Figure 5.20: Comparison of ground configurations and routing for NSH-Hexaboard-V2 and NSH-Hexaboard-V3. (a) Ground plane configuration in HGCROC-V2, with AGND and DGND separated on the substrate. (b) BGA routing on NSH-Hexaboard, highlighting ground connections (red areas). (c) Block diagram illustrating ground connectivity for NSH-Hexaboard-V2 (assembled with HGCROC-V2) and NSH-Hexaboard-V3 (assembled with HGCROC-V3). Differences in AGND and DGND connections result in varying Δ-pedestal values, with unified grounds in V3 contributing to increased digital modulation.

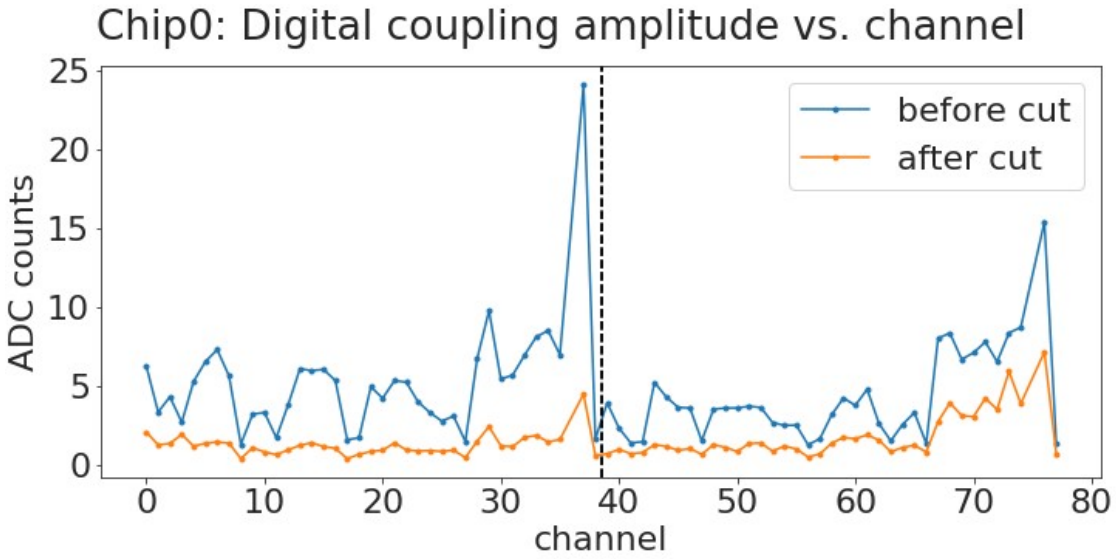


Figure 5.21: Reduction in Δ-pedestal values observed across channels by isolating the analog and digital return paths in NSH-Hexaboard-V2. The plot compares the digital coupling amplitude before and after breaking the AGND-DGND link on the top layer, highlighting a significant reduction in digital modulation.

it is imperative to separate analog and digital return currents at both the package level and on the Hexaboard's top layer. This separation should be maintained until their convergence on a low-impedance ground plane. Hexaboards are designed with three primary ground planes: L3, L5, and L7, which are interconnected through PTH vias. This ensures a robust and consistent grounding scheme across the board.

- **Ensure Optimal Connectivity for Power and Ground Pins:** The experiment highlighted a critical limitation in the current design, namely the insufficient allocation of PTH vias for analog ground pins due to space constraints. Additionally, the use of micro-vias (limited to connections between L1 and L2) proved inadequate for providing low-impedance access to the main ground plane (L3). Future designs must establish a direct connection between each power and ground pin and the corresponding ground and power planes on the Hexaboard to improve electrical performance and system reliability.
- **Adopt Via-in-Pad Technology:** Implementing Via-in-Pad technology is recommended to address the space limitations encountered in high-density designs. This approach enables more efficient connections for power and ground pins while adhering to the physical constraints of the HD-Hexaboard design. The implementation of this strategy will be discussed further in the context of the V3-HD-Hexaboard-V2 design.
- **Recommendations for ASIC Design:** ASIC packages should maintain separation between analog and digital return paths at the substrate level. Digital components exhibiting high-speed transients and analog components must have distinct return paths to ensure minimal interference. These currents should converge only at the Hexaboard's ground planes, allowing isolation of return currenst inside the package level.

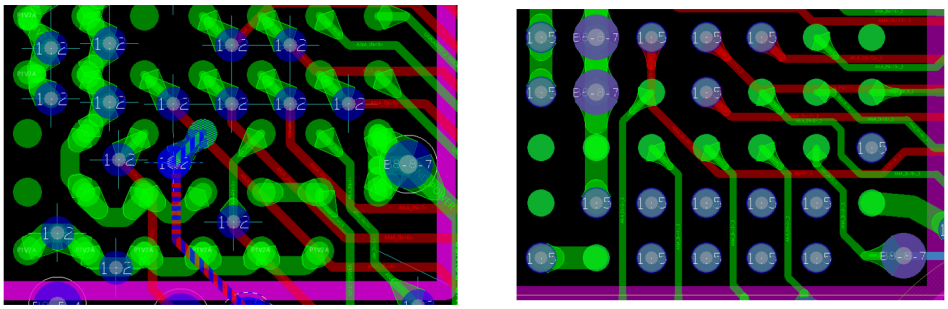
The experiment with NSH-Hexaboard-V2 and the subsequent development of these guidelines rep-

resent a pivotal step in addressing digital modulation challenges. These insights will be instrumental in shaping the design and performance optimisation of the next-generation HD Hexaboards.

5.12 2^{nd} version of 8" HD Hexaboard (V3-HD-Hexaboard)

As recommended in Section 5.11, to achieve low-inductance power and return paths, the V3-HD-Hexaboard design was implemented using the Via-in-Pad technique. As the name suggests, the "Via-in-Pad" design incorporates vias directly within the BGA pads. This approach reduces the area required for vias, providing more routing space between BGA balls to simplify signal routing. It also significantly improves heat dissipation by connecting each pin directly to the inner PCB layers, enabling efficient heat transfer. The reduced routing length between the BGA pad or decoupling capacitor and the via, minimizes parasitic inductance, thereby improving signal integrity and decoupling for high-speed transients.

However, this technique incurs additional manufacturing costs. After drilling the holes in the pads and coating them with copper, the holes either be filled with non-conductive resin and then copper-capped or fully copper-filled to prevent solder flow, ensuring robust component assembly. A final planarization process is also required to smooth the pad surfaces for assembly. Figure 5.22 compares the traditional Dog-Bone fanout technique with the Via-in-Pad approach.



(a): BGA fanout with Dog-bone pattern in NSH Hexaboard (b): BGA fanout with Via-in-Pad in V3-HD-Hexaboard

Figure 5.22: Comparison of BGA fanout techniques in NSH-Hexaboard and V3-HD-Hexaboard. (a) Dog-bone pattern used for BGA fanout in NSH-Hexaboard, highlighting the traditional approach with separate via placements. (b) Via-in-Pad technique implemented in V3-HD-Hexaboard, enabling efficient space utilization and improved electrical performance by integrating vias directly within the pads.

The final iteration of the high-density Hexaboard, designated as V3-HD-Hexaboard-V2.2, is illustrated in figure 5.23. The "V3" indicates the use of HGCROC family version 3, while "V2.2" refers to the specific iteration within the design evolution, succeeding versions 2.0, 2.1, and 2.2. This Hexaboard is equipped with six HGCROC-V3 chips (HD package) to read out an HD full silicon sensor comprising 432 diode pads, each with an area of 0.5 cm^2.

Power Distribution and Connectivity:
The power distribution scheme for the V3-HD-Hexaboard is illustrated in figure 5.24. Figure 5.24 (a) shows the split power plane on L4, segmented into three sub-power planes: 1V2D (digital), 1V2A-UP (analog upper region), and 1V2A-DW (analog lower region). Due to space constraints, the V3-HD-Hexaboard adopts a customized power delivery solution. Power is supplied to the board via a lug connector and five power spacers: two for grounding, two for analog 1.5 VA, and one for digital 1.5 VD, as shown in figure 5.24 (b). These 1.5V supplies are further regulated to provide three distinct outputs: 1V2A-UP, 1V2A-DW, and 1V2D, ensuring efficient power distribution to all functional regions of the board.

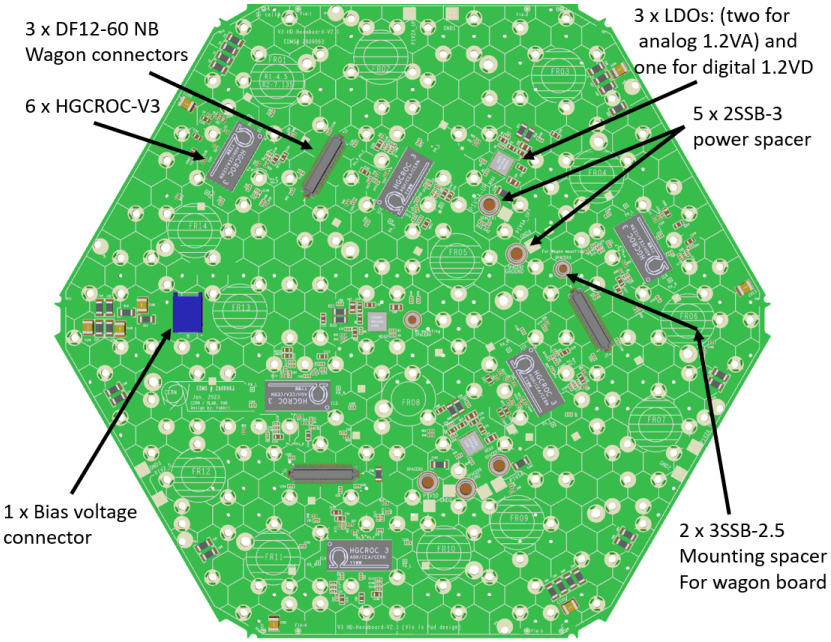


Figure 5.23: Layout of the latest HD design V3-HD-Hexaboard-2.2. The board features 6 HGCROC-V3 chips, 3 × DF12-60 NB Wagon connectors for data transmission, and 1 bias voltage connector for module operation. Additionally, it includes 3 LDOs (two for analog 1.2 VA and one for digital 1.2 VD), 5 SSSB-3 power spacers, and 2 SSSB-2.5 mounting spacers for wagon board integration.

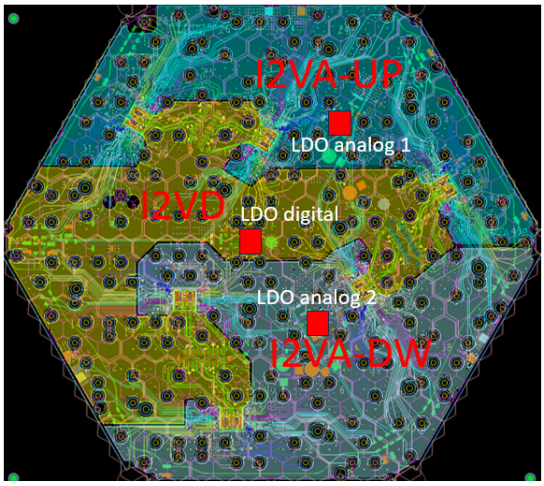
These boards also feature a dedicated connector for bias voltage delivery and six strategically positioned offset step holes to ground the silicon sensor guard ring. Figure 5.24 (c) illustrates the wagon stack-up, demonstrating how power is routed to the board using a crimp-fit lug and MAC-8 spacers, offering a robust and space-efficient solution for power connections.

Connectivity with Detector Components:
To facilitate communication with other detector components, the V3-HD-Hexaboard integrates three wagon connectors (DF12NB-60DS-0V5, 60 pins each) corresponding to the three sectors of the Hexaboard (s1, s2, s3). These connectors communicate DAQ data, trigger-data signals, clock, slow and fast controls, and various reset and status signals. Each wagon connector services two HGCROCs and one LDO within its designated sector.

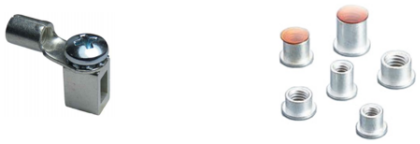
The V3-HD-Hexaboard-V2.2 incorporates 14 reserved no-go areas, deliberately kept empty to enable secure handling by vacuum cups of the pick-and-place machine during the automated module assembly process. This design enhancement ensures reliable mechanical integration and marks a substantial step forward in addressing the challenges posed by high-density PCB architectures, while fulfilling the stringent performance and integration requirements of the HGCAL detector system.

5.12.1 Stack-up and VIA Scheme

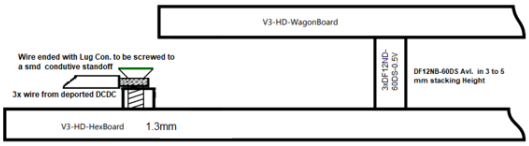
The V3-HD-Hexaboard design incorporates an 8-layer PCB stack-up and employs the Via-in-Pad fanout technique, as shown in figure 5.25. The cross-sectional view of the stack-up, depicted in figure 5.25 (b), illustrates the eight layers and the details of the two types of vias used, along with the back-drill scheme. The design utilizes two distinct via types: a PTH via spanning L1 to L8, and a specialized via that serves as a blind via but is PTH Via, extending from L1 to L5. The latter is a result of the Hexaboard's unique



(a): The power plane for V3-Hd-Hexaboard



(b): The lug connector and MAC-8 spacer



V3-HD-HB and Wagon stack up

(c): PWR will be brought via crimp fit Lug to smd 2SSB-2.5 spacer

Figure 5.24: Power scheme for the V3-HD-Hexaboard. (a) Split power plane on L4, divided into three sub-power planes: 1V2D, 1V2A-UP, and 1V2A-DW, each powered by individual LDOs. (b) The lug connector and MAC-8 spacer are used for customized power delivery in space-constrained designs. (c) Schematic of the V3-HD-Hexaboard and wagon stack-up, illustrating how power is brought to the board using a crimp-fit lug and SMD 2SSB-2.5 spacer.

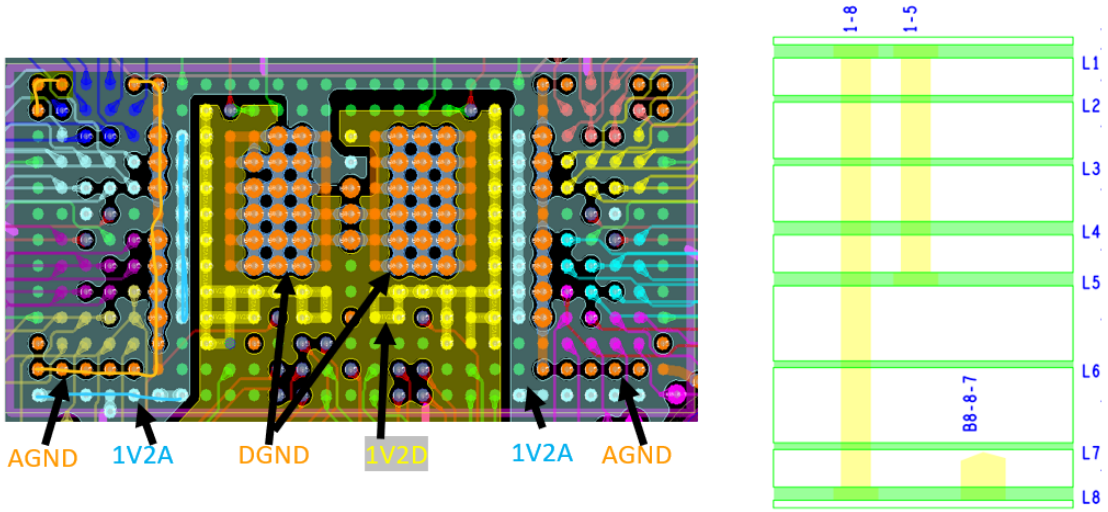
manufacturing process, where it is initially fabricated as a PTH via and subsequently modified to function as a blind via.

The PCB stack-up is largely similar to that of the V3-LD-Hexaboard, with one significant modification: the swapping of L2 and L3. Layers L1 and L3 are now dedicated to high-speed differential signal routing, with reference to the ground plane located at L2. L4 functions as a split power plane, divided into sub-power planes for digital (1V2D) and analog (1V2A) supplies. To enhance inter-plane capacitance, a ground plane with minimal dielectric separation (100 µm) is positioned adjacent to L4.

The analog routing is critical for connecting the bonding pads on L6 (intended for bonding to silicon diode pads) to the HGCROC pre-amplifier input. This routing requires careful shielding to preserve signal integrity. Ground planes at L5 and L7 are strategically placed to shield the sensitive analog signals while maintaining their integrity. To reduce capacitive coupling with the silicon pads, L8 is intentionally left unpopulated, optimizing the electrical performance of the Hexaboard.

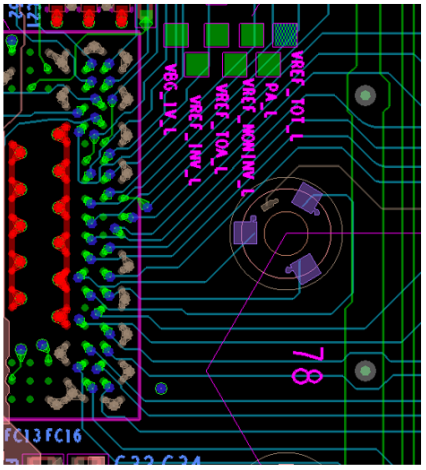
The justification for swapping L2 and L3 compared to the V3-LD design is shown in figure 5.26. In the V3-LD-Hexaboard as shown in figure 5.26 (a), the larger 0.8 mm BGA pitch allows the use of a single type of PTH via for all layers, enabling analog routing from L6 to L1 directly. This design minimizes coupling between analog and digital signals in the BGA region, allowing the ground plane to remain at L3. However, in the case of V3-HD-Hexaboard, shown in figure 5.26 (b), manufacturing constraints preclude the extension of blind vias to L6. Consequently, analog signals must first be routed to L1 or L2, which increases the likelihood of coupling between analog and digital signals. To mitigate this, the ground plane is moved to L2, sandwiched between the routing layers L1 and L3, effectively reducing cross-layer interference.

In the BGA region, the analog channel pins (excluding those in the first and last columns) are routed using a blind via breakout strategy. Pins in the first and last columns are routed on L1 and subsequently connected to L6 via PTH vias. For digital ground (DGND) pins located centrally in the BGA, a direct

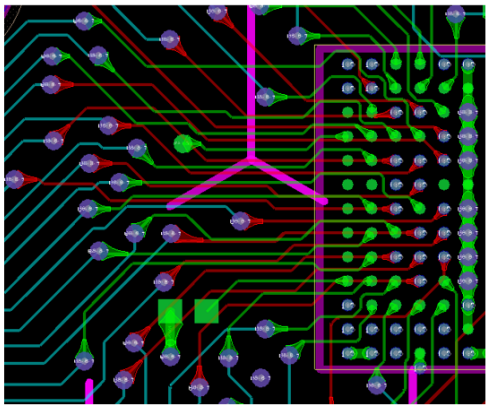


(a): HGCROC-V3 HD package BGA fanout in V3-HD-Hexaboard (b): Cross-section view

Figure 5.25: (a) The fan-out of the HD-HGCROC-V3 in V3-HD-Hexaboard-V2.2, utilizing PTH vias (L1-L8) and blind vias (L1-L5). (b) Cross-sectional view of the PCB stack-up, detailing the types of vias and the back-drill scheme employed.



(a) V3-LD-Hexaboard routing scheme: Layers colors: L6: light blue, L1: Green.



(b) V3-HD-Hexaboard routing scheme: Layers colors: L6: light blue, L1: Green L2 : red

Figure 5.26: Comparison of PCB routing in V3-LD and V3-HD designs. (a) V3-LD analog signals (light blue) are routed directly from L6 into the BGA region and connected to pins using PTH vias (L1-L8). (b) V3-HD analog signals are routed from L6 to L2 (red) or L1 (green) via PTH vias and then further routed to BGA pins.

connection to the ground plane is established using PTH vias. In contrast, analog ground (AGND) pins, situated at the periphery, use a combination of PTH and blind vias, depending on the available routing

space. Power pins are connected to their respective sub-power planes (1V2D and 1V2A) on L4 using blind vias. Some pins are intentionally left without vias and are connected to the nearest available net to facilitate power distribution within the internal layers.

The V3-HD-Hexaboard's stack-up and VIA scheme optimize signal integrity and power distribution within the constraints of a 0.6 mm BGA pitch. The design effectively mitigates signal coupling through the strategic placement of ground planes and employs advanced routing techniques to meet HGCAL's performance requirements.

5.12.2 Design validation by simulation

Hexaboard is a very complex, noise-sensitive, multilayer HDI design. It is very important to validate and sign off design before fabrication. For this purpose, the design is passed through a long PCB simulation cycle. The Ansys SIWAVE PCB signal and power integrity simulation tools are being used for these studies.
The main scans and tools used for these validation cycles are the following: (see chapters 12 and 13 of [105])

- *Power integrity simulation*: Includes PDN Target Impedance control and IR Drop Scan.
- *Signal Integrity Simulation*: includes S-Parameter Extraction for validation of high-speed links (320MHz and 1.28 Gbps) and Impedance Scan.

The details of these tests are:

- TARGET IMPEDANCE: The term "target impedance" denotes the highest permissible impedance that the PDN can exhibit towards the load, while still satisfying the voltage regulation criteria of the load components. The target impedance curve is typically established based on the transient response criteria of the load and the permissible voltage fluctuation defined for the system. PDN Target Impedance is extracted for a wide frequency range to see if there are any large impedance peaks for certain frequencies, that can cause a large ripple at that specific frequency in PDN. This target impedance scan utilysed for optimizing the decoupling scheme and controlling power path impedance below a certain threshold to reduce ripple in the system for large frequency ranges. The target impedance for a power plane is calculated by equation 5.3 shown below:

$$Z = \Delta V / I_{nst}. \tag{5.3}$$

Where ΔV is the allowed ripple in the supply voltage. Its nominal allowed value is 5% of applied voltage. For Hexaboard, the applied voltage value is 1.2 V;

$$\Delta V = 1.2 * 5/100 = 0.06 \text{ V}. \tag{5.4}$$

And I_{nst} is the Instantaneous current drawn by the load, in our case its average value is 2 A, therefore, the target impedance values is:

$$Z = 0.06 \text{ V}/2 \text{ A} = 30 \text{ mOhms}. \tag{5.5}$$

The impedance profile of the digital power plane for the V3-HD-Hexaboard-V2.2 is illustrated in figure 5.27. This figure demonstrates that, across a broad spectrum of frequencies, the digital power plane's target impedance is effectively regulated. However, the PDN exhibits minor resonant peaks

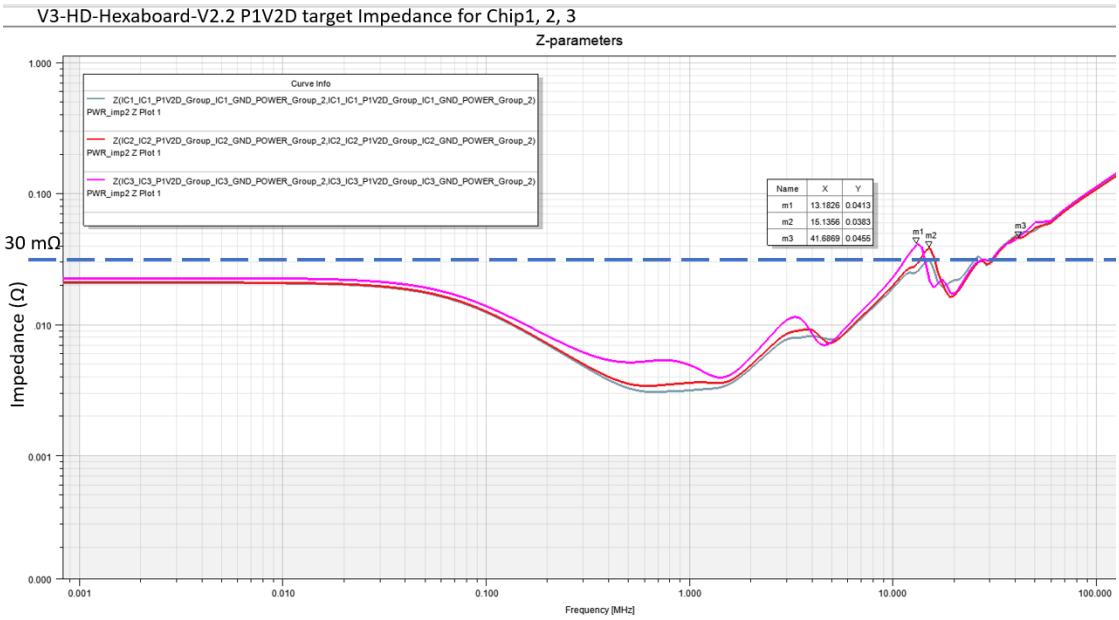


Figure 5.27: Target Impedance extraction for V3-HD-Hexaboard-V2.2 for digital power 1V2D for chip1, 2, 3.

at frequencies of 13.18 MHz and 15.13 MHz, denoted by markers M1 and M2, respectively. Resonant peaks indicative of excessive impedance can be mitigated by incorporating decoupling capacitors tuned to the corresponding resonant frequencies, thereby enhancing the overall impedance characteristics of the PDN.

- IR-DROP SCAN : For identifying abnormal plane voltage drops and current congestion; the IR scan is performed. Figure 5.28 provides a detailed IR-drop analysis, including IR-drop measurements "Δ-V" and current density of the V3-HD-Hexaboard power plane. The left plot uses a color-coded scale to clearly illustrate the voltage drop across the power plane. Notably, the LDO regulator, where the voltage is 1.197 V, is marked by red markers when it is close by. Blue markers, on the other hand, indicate areas with the lowest recorded voltage value of 1.194 V, which means there is a mere 3 mV, indicating the effectiveness of the power plane in sustaining a steady voltage level. The right figure is depicting the current density of the power plane and especially helpful in spotting possible current flow congestion, which may point to inefficient regions or the possibility of localized heating. These kinds of insights are essential for identifying the power plane's malfunctions and for directing further optimization techniques.

- IMPEDANCE SCAN: To identify impedance discontinuities for differential and critical single-ended signals. It is a very useful tool for reducing the reflections in signal transmission. Figure 5.29 analyzes PCB 100Ω differential traces impedance in detail. The picture uses color coding to show PCB trace impedance levels, helping identify if there is any impedance miss-match that could affect circuit performance. The yellow colors represent 97.5Ω impedance levels for the L3 routing while the Orange color shows 105.5Ω for L1 differential routing. both values are acceptable and are in the range of 100Ω with ±10% which is by the design specifications.

- S-PARAMETER EXTRACTION: S-parameter especially insertion-loss scan used to validate the differ-

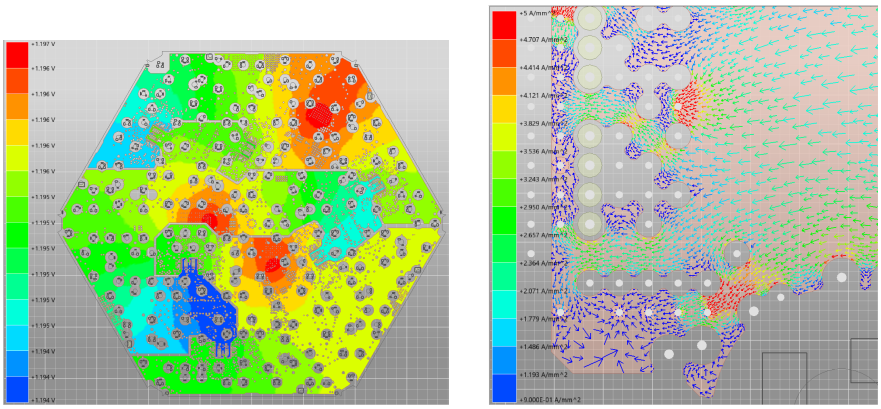


Figure 5.28: The Voltage distribution and current density analysis of V3-HD-Hexaboard power plane: The left image shows the voltage gradient across the plane, with red regions near the LDO at 1.197 V and blue regions with minimal drops (3 mV). The right image shows the current flow density, revealing PDN congestion.

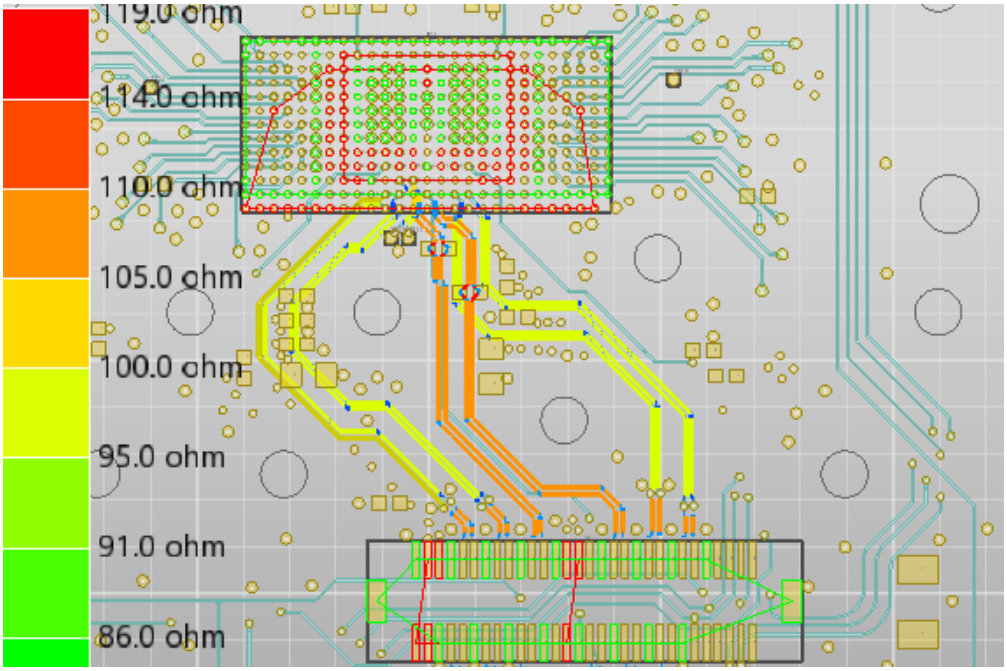


Figure 5.29: Impedance scan for differential routing on L1 and L3. The plot shows the differential impedance of the 100 Ω routing, displayed in a color-coded manner, with values maintained within ±10% of the target 100 Ω.

ential links quality, to ensure that the 3 dB loss point is at least 5 harmonics above the signal frequency. Figure 5.30 illustrates the S-parameter response analysis of a signal with a fundamental frequency of 320 MHz. This diagram is crucial for illustrating the signal's behavior throughout a wide range of frequencies. The response curve exhibits a crucial point at a frequency of 7.05 GHz,

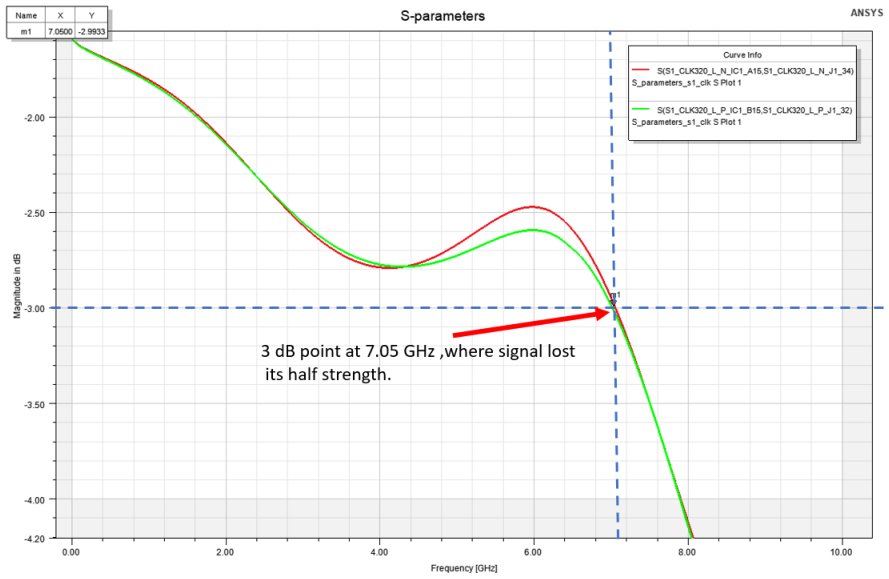


Figure 5.30: S-Parameter response analysis for a signal with a frequency of 320 MHz. The plot depicts the dB magnitude of the S-parameters over a frequency range of up to 10 GHz. It highlights the 3 dB cutoff point at 7.05 GHz, which signifies the frequency at which the signal intensity is halved.

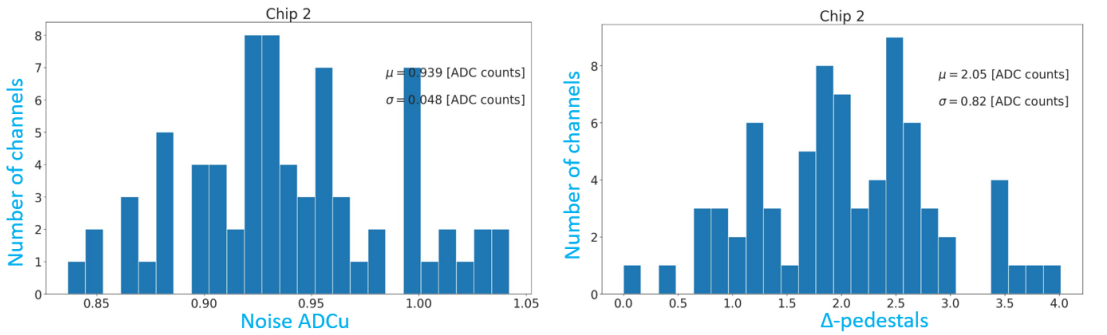
which is recognized as the cutoff frequency with a 3 dB attenuation. This point signifies a notable breakthrough in signal analysis, as it denotes the frequency at which the power of the signal is reduced to half of its maximum value. It effectively serves as a metric for the system's bandwidth. An analysis of this nature is crucial during the design and verification of high-frequency circuits since it enables the fine-tuning of the circuit's performance across the desired frequency range.

5.12.3 Performance analysis (bare Hexaboard and silicon Hex-Module)

The average noise and Δ-Pedestal values for five V3-HD-Hexaboards are presented in tables 5.3 and 5.4 respectively, with detailed plots for Chip 2 of board XHF03PN-00023 shown in figure 5.31. The results exhibit a consistent pattern of noise and Δ-Pedestal values across the tested boards, identified by serial numbers XHF03PN-00020, XHF03PN-00023, XHF03PN-00025, XHF03PN-00034, and XHF03PN-00035 (where XHF denotes the full HD-Hexaboard version, 03 represents HGCROC-V3, and the last two digits indicate the Hexaboard serial number).

Average Noise (ADC units)						
Board	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
XHF03PN-00020	0.95	0.97	0.74	0.78	0.96	0.73
XHF03PN-00023	1.059	1.017	0.93	0.94	1.04	0.91
XHFO3PN-00025	0.91	0.99	0.93	0.95	0.96	0.855
XHF03PN-00034	0.933	0.959	0.995	0.761	0.938	0.726
XHF03PN-00035	0.998	1.018	1.074	1.052	0.997	1.04
Average	0.97	0.9908	0.9338	0.8966	0.979	0.8522
All Boards Avg.	**0.93 ADC units** ($\sim 1200e^-$ at 160 ADC gain range)					

Table 5.3: Average noise values for all chips of 5 V3-HD-Hexaboards (XHF03PN-000xx).



(a): Average Noise for Chip2 of XHF03PN-00023 (b): Average Δ-pedestals for Chip2 of XHF03PN-00023

Figure 5.31: Average noise and Δ-Pedestal values for Chip 2 of XHF03PN-00023. The noise histogram (left) shows a mean of 0.93 ADC units, while the Δ-Pedestal histogram (right) records an average of 2.05 ADC units.

Δ-Pedestal (ADC units)						
Board	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
XHF03PN-00020	1.86	1.63	4.85	3.81	1.48	5.4
XHF03PN-00023	1.74	1.69	2.05	1.88	1.94	2.32
XHFO3PN-00025	1.59	1.55	2.25	1.8	1.92	1.58
XHF03PN-00034	1.68	1.72	3.49	1.8	1.72	1.25
XHF03PN-00035	1.71	1.77	1.42	1.9	1.52	1.55
Average	1.716	1.672	2.812	2.238	1.716	2.42
All Boards Avg.	**2.09 ADC units** ($\sim 2600e^-$ at 160 ADC gain range)					

Table 5.4: Δ-Pedestal values for all chips of 5 V3-HD-Hexaboards (XHF03PN-000xx).

The mean noise level across all chips remains below 1 ADC unit, with an average of ~ 0.93 ADC units for all boards, indicating a low-noise operational environment for the Hexaboards. The Δ-Pedestal average value is recorded at ~ 2 ADC units, which is slightly higher than the ~ 1.8 ADC units observed in V3-LD-Hexaboards for limited datasets. Among the chips, Chip 3 exhibits the highest average Δ-Pedestal value of 2.238 ADC units, suggesting the need for closer inspection and debugging, both at the operational and design levels.

The HD silicon Hex-Module has been assembled using a 120 µm-thick silicon sensor with the V3-HD-Hexaboard series. The histograms in figure 5.32 show the average noise and Δ-Pedestal distributions. The noise histogram (left) records an average value of ~ 1.7 ADC units, translating to ~ 2200 electrons for the 54 pF capacitance of the 120 µm silicon sensor. This value aligns closely with the anticipated noise levels for 54 pF as shown in figure 5.3. The Δ-Pedestal histogram (right) has an average of ~ 5.6 ADC units, with a few outlier channels exceeding 20 ADC units, suggesting the need for further analysis to enhance TOA threshold settings.

The latest V3-HD-Hexaboard design demonstrates significant improvements over the previous NSH-Module, which utilized the same HGCROC-V3 ASIC in an HD package. Specifically, the average noise and Δ-Pedestal values for the V3-HD module are ~ 1.7 ADC units and ~ 5.6 ADC units, compared to 2.5 ADC units and 175 ADC units, respectively, for the NSH-Module. These advancements are attributed to enhanced design robustness, better grounding, and improved routing strategies.

A comparison of coherent and intrinsic noise levels across the V3-HD, V3-LD, and NSH modules, as shown in figure 5.33, further highlights the performance improvements of the V3-HD module. The Incoherent noise, represented by the even-odd subtraction in the blue histograms, is lowest for the V3-HD

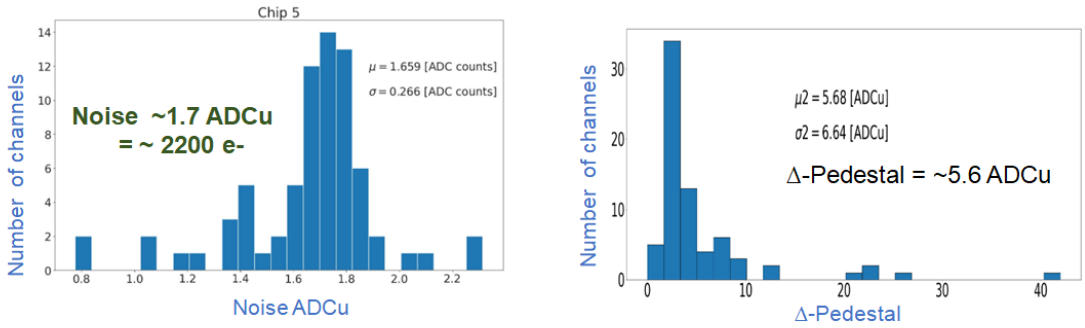


Figure 5.32: Histograms showing the average noise and Δ-Pedestal values for the V3-HD silicon Hex-Module. The noise histogram (left) records an average of $\sim$ 1.7 ADC units ($\sim$ 2200 e^-), and the Δ-Pedestal histogram (right) shows an average of $\sim$ 5.6 ADC units.

module with a standard deviation normalized by the square root of the number of channels (std/$\sqrt{n}$) at 1.46 ADC units. In contrast, the V3-LD and NSH modules exhibit higher coherent noise values of 1.91 and 1.94 ADC units, respectively. Similarly, the coherent noise (orange histograms) is also lowest for the V3-HD module, with a CN of 0.30 ADC units compared to 0.64 ADC units for the V3-LD module and a significantly higher 2.76 ADC units for the NSH module.

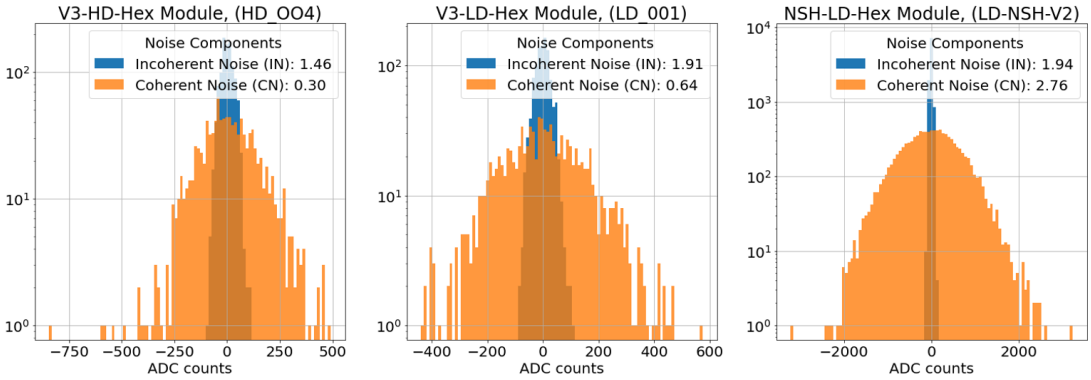


Figure 5.33: Comparison of coherent and incoherent noise for different silicon Hex-Module variants. The plot illustrates the noise performance of the V3-HD-Hex Module (120 µm sensor), V3-LD-Hex Module (300 µm sensor), and NSH-Hex Module (300 µm sensor). For each configuration, the alternate sum (even-odd channels) and direct sum (all channels) noise are analyzed. The V3-HD-Hex Module demonstrates the lowest coherent and incoherent noise levels, highlighting its optimized design and enhanced signal integrity compared to the other versions.

These results emphasize the effectiveness of the V3-HD design in minimizing both coherent and intrinsic noise, which is crucial for high-precision applications. The data presented underscores the reliability and robustness of the V3-HD module, reinforcing its suitability for pre-production. With consistent noise levels, controlled Δ-Pedestal values, and significantly reduced noise characteristics, the V3-HD module is well-positioned to set new benchmarks for performance and reliability in high-precision detec-

tor systems.

5.13 Partial Hexaboards

To maximise the coverage at the inner and outer cassette peripheries, partial Si sensors diced from full hexagonal sensors by cutting full hexagonal sensors into different non-hexagonal subparts are used. Each sensor variant requires a distinct PCB design, resulting in 11 Hexaboard variants [101]. Following hexaboard variants based on their cell size, the partials also have LD and HD variants. There are a total of 11 variant hexaboards; two of them are full (HD and LD), five LD partials, and four HD partials. The full versions are already explained in detail.

5.13.1 LD-Partial Hexaboards

Figure 5.34 presents five variants of LD-partial Hexaboards designed to meet the unique geometrical requirements of LD sensors in the HGCAL system. Subfigure (a) depicts the V3-LD-Half designs, specifically addressing the top and bottom regions of the half-sensors to ensure complete coverage. Subfigure (b) showcases the V3-LD-SEMI designs, optimised for the left and right sections of the SEMI sensors. Subfigure (c) features the V3-LD-Five design to efficiently read out the Five-partial sensors. The first four designs utilise two HGCROC chips each, while the fifth employs three chips for a full readout of silicon pads. These unique designs ensure full coverage of the silicon sensor readout for the HGCAL detector.

Each partial hexaboard has a unique design tailored to its location and function within the detector assembly. Unlike the full hexaboard, the partial hexaboards connect to a dedicated Partial Concentrator Mezzanine board (PCM), which houses the ECON-D, ECON-T, and Rafael ASIC for clock distribution and command fanout. This PCM interfaces with the wagon board through a specialised, thin Zipper board, ensuring efficient data transmission and command routing, as depicted in figure 5.35.

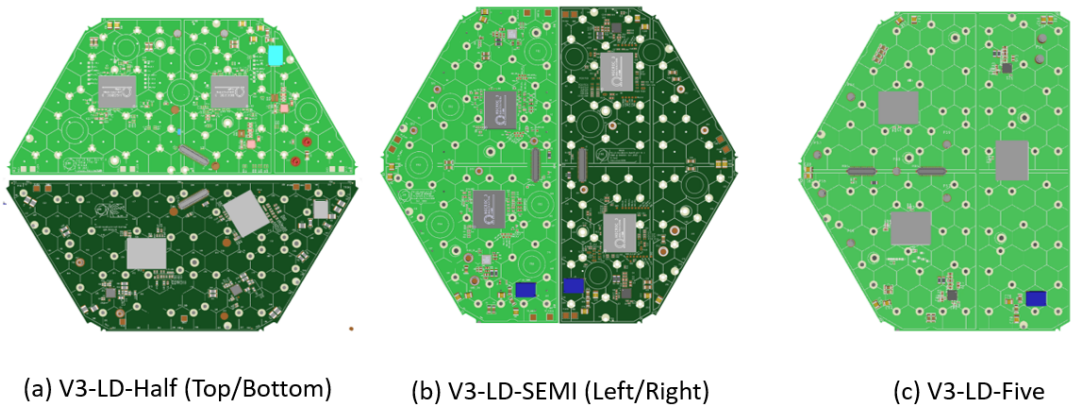


Figure 5.34: The LD-Partials design: (a) shows V3-LD-Half (Top/Bottom), (b) shows V3-LD-SEMI (Left/Right), and (c) shows V3-LD-Five.

To accommodate the detector's complex geometry, various PCB configurations were initially required for LD partials, depending on their spatial orientation and connection points to the wagon board. However, the design process was streamlined by reducing the number of board variations. The physical complexities are now addressed through the tailored shapes of the partial concentrator boards, which maintain robust connectivity to the wagon using specialized compact concentrator cards.

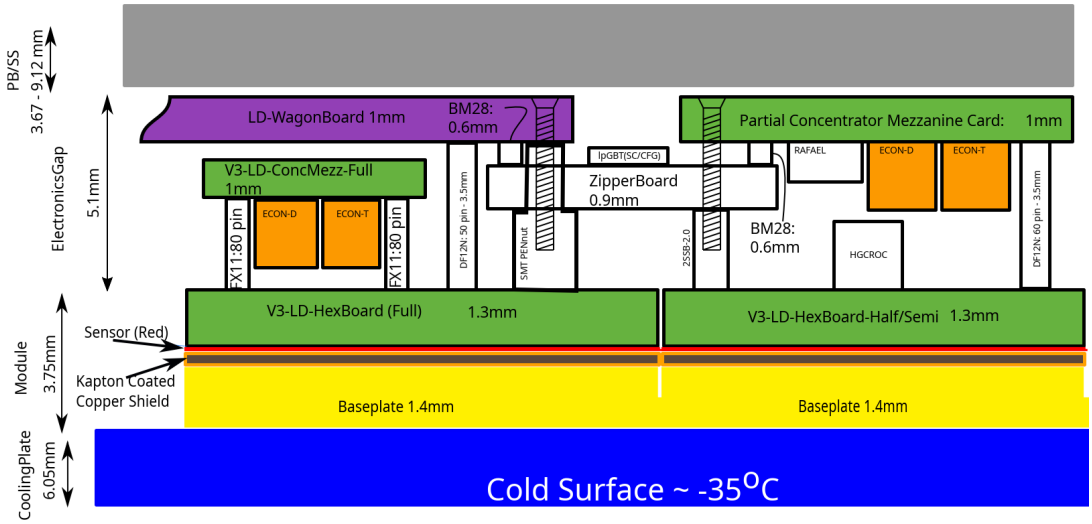
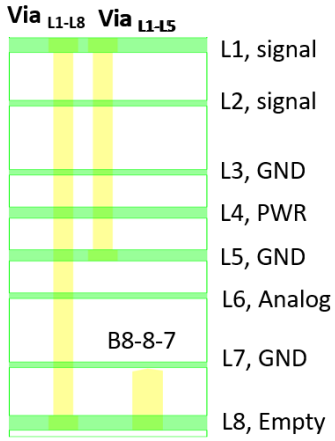
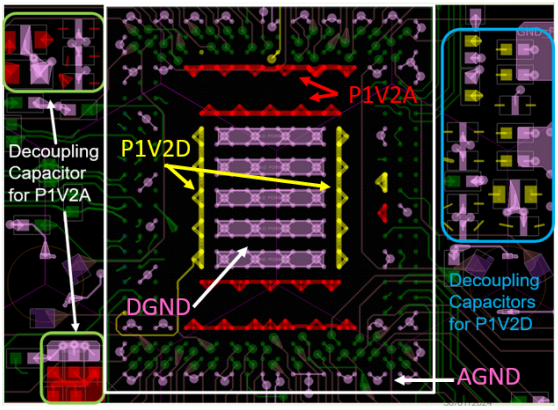


Figure 5.35: The LD Partials board connectivity scheme with Wagon through partial concentrator mezzanine and a Zipper board [28].

Each LD-partial hexaboard design ensures complete coverage of the sensor's active area, with unique channel mappings and split power plane configurations tailored for efficient power distribution. This thoughtful approach enables the seamless operation of both the digital and analog LDOs, facilitating precise signal processing within the HGCROC.



(a): Stack-up cross-section with VIA types and back-drilling set.



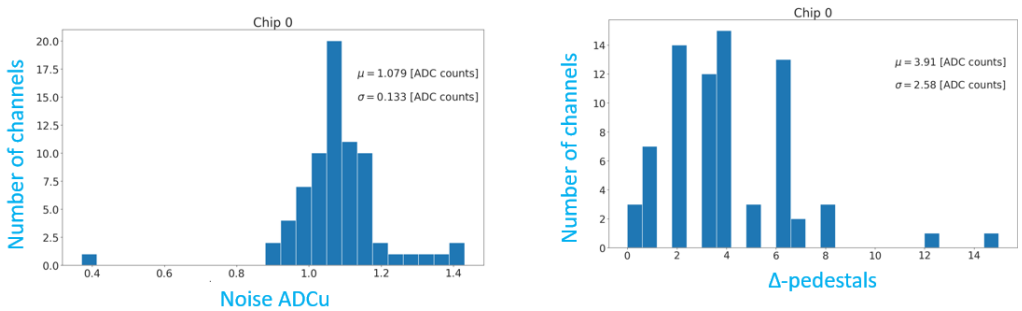
(b): HCGROC-V3 fanout in LD-Partials

Figure 5.36: (a) Stack-up cross-section with VIA types and back-drilling set. (b) HGCROC-V3 fanout in LD-Partials, illustrating power (P1V2A, P1V2D), ground (DGND, AGND), and decoupling capacitor placements.

Figure 5.36 illustrates the LD-partial stack-up and BGA fanout, highlighting key design adaptations

tailored for partial boards. Subfigure (a) presents the eight-layer stack-up, derived from the LD full version, with specific modifications inspired by the HD design. These modifications include the addition of VIA [L1-L5], strategically placed in areas above the dicing line of the silicon sensor carrying the bias voltage. This adjustment not only optimised the design but also reduced the backdrill requirement to a single layer (B8–8–7), improving manufacturing efficiency. Subfigure (b) details the BGA fanout and routing, where decoupling capacitors for analog (P1V2A) and digital (P1V2D) power are positioned on the left and right sides, respectively. Power pins are connected to their respective power planes via PTH vias, while digital ground pins link to L3, L5, and L7 through grouped PTH vias. Analog ground is isolated on Top layer and routed through PTH VIA [L1-L8] to connect with the inner ground planes. This meticulous layout ensures robust grounding, reliable power delivery, and stable performance, all critical for the operation of the LD-partial hexaboards.

The performance of a partial design of the LD-SEMI left is shown in figure 5.37. The noise distribution, depicted on the left, demonstrates an average noise value of 1.079 ADC units for Chip 0, indicating stable and uniform behaviour across the channels. On the right, the Δ-pedestal distribution shows an average value of 3.91 ADC units, reflecting the pedestal variability with phase. These metrics validate the robustness and operational stability of the design, with opportunities for further improvement in Δ-pedestal uniformity through tuning and debugging of a few channels with higher values to enhance the overall electrical performance.



(a): Average Noise for Chip0 of LD-SEMI left (L01) (b): Average Δ-pedestals for Chip0 of LD-SEMI left (L01)

Figure 5.37: The Noise and Δ-pedestal performance of LD Partial SEMI (named as L01): (Left) The histogram represents the noise distribution for the Partial LD-SEMI, with an average noise value of $\mu = 1.079$ ADC units, indicating stable noise performance across the chip's channels. (Right) The histogram shows the Δ-pedestal distribution for the Partial LD-SEMI, with a mean value of $\mu = 3.91$ ADC units, reflecting the variation in pedestal with phase across the chip's channels.

The LD-Partial hexaboard designs effectively meet the geometrical and functional requirements of the LD sensors, ensuring full coverage, stable connectivity, and optimised power distribution. The V3-LD-SEMI left achieves comparable performance to the full LD hexaboard, with an average noise of $\sim$1 ADC units and a Δ-pedestal of 4 ADC units, both within the acceptable range and compliant with full LD specifications.

5.13.2 HD-Partial Hexaboards

The four HD-partial hexaboard designs, V3-HD-Top (Half), V3-HD-CHOP-II (Bottom), V3-HD-SEMI-Left, and V3-HD-SEMI-Right, are shown in figure 5.38. These designs are specifically developed to address the geometrical and functional requirements for the inner pheripery of the HD sensors, ensuring precise signal readout and robust connectivity across all regions. Each partial has a unique design against

its own set of constraints, similar in concept to their LD counterparts. The stack-up and via scheme for these partial boards are consistent with the design principles of the full HD hexaboards, as detailed in Section 5.12.1. This consistency guarantees reliable signal integrity and optimized power distribution across all configurations.

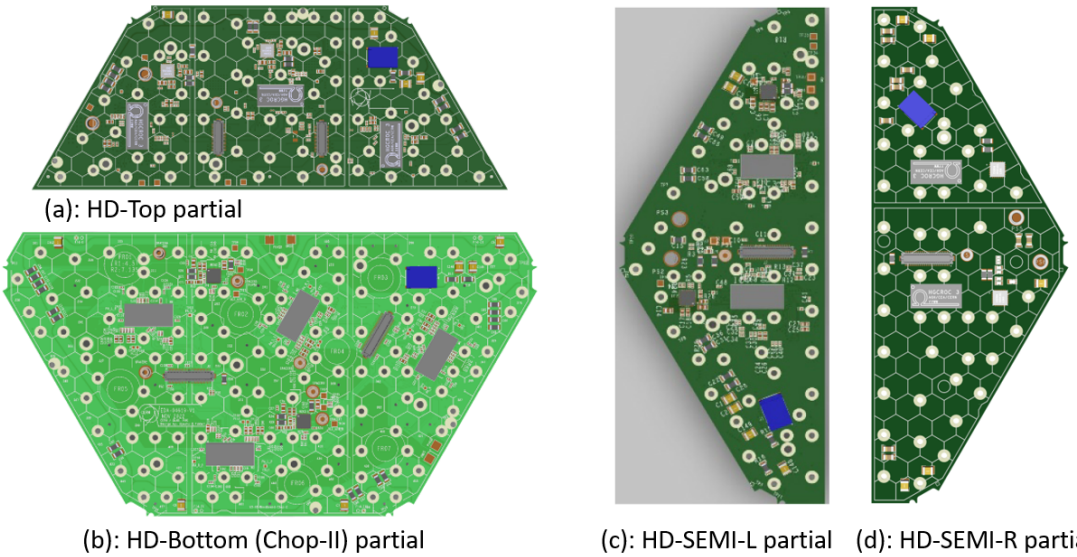


Figure 5.38: HD-Partial hexaboard designs: (a) HD-Top partial, (b) HD-Bottom (CHOP-II) partial, (c) HD-SEMI-Left partial, and (d) HD-SEMI-Right partial. These boards are tailored for the inner periphery of the HD sensor.

The connectivity for the HD partial boards mirrors that of the full HD design. Each board is read by the HD wagon, which hosts the Rafael ASIC for clock and fast command fanout, and the ECON-D and ECON-T ASICs for data and trigger concentration. All the designs have undergone extensive PCB simulations to validate their performance and reliability. However, these boards are still in the pre-production phase, and no test results are available at the time of this writing.

Overall, the HD-partial hexaboards provide a versatile and efficient solution for sensor coverage in regions where the full HD boards cannot be deployed.

5.14 Conclusion

This chapter presented the design evolution, prototyping, and optimisation of Hexaboards for the HGCAL detector, focusing on both LD and HD configurations. The development followed a structured approach, beginning with the LD Hexaboard as a reference before transitioning to the HD version.

The initial prototype, LD-HB-CMS-V1, designed with existing knowledge inspired by earlier SKIROC-based designs. While it served as a proof of concept, its high digital noise and inadequate shielding between analog and digital circuitry highlighted key areas for improvement. Despite these limitations, valuable insights were gained, leading to refinements in copper balancing, bonding pad layout, and glue-seepage mitigation. These improvements laid the groundwork for subsequent iterations.

The second prototype, LD-NSH-HB-V2, incorporated an optimised stack-up and leveraged PCB simulations to refine signal integrity. By replacing stepped holes with non-stepped holes, manufacturing complexity and production time were reduced. These changes significantly improved pedestal noise, lowering it to $\sim$1.3 ADC units for the bare board and $\sim$2.4 ADC units for assembled modules. However, assembling with HGCROC-V3 revealed an unexpected increase in Δ-pedestal, necessitating further R&D. This investigation emphasised the importance of low-impedance return path separation for analog and digital grounds, both at the package level and PCB top layer.

The final version, V3-LD-Hexaboard-V1.3, integrated all previous refinements and met the performance benchmarks set by HGCAL. Pedestal noise was reduced to $\sim$1.0 ADC units for the bare board and $\sim$1.5 ADC units for assembled modules, with a Δ-pedestal of $\sim$9 ADC units. The signal-to-noise ratio (S/N) reached 11, ensuring compliance with the HGCAL TDR specifications. Further enhancements improved manufacturability, optimizing mechanical integration and service routing for deployment in HL-LHC conditions.

Building on the LD Hexaboard experience, the HD Hexaboard design incorporated key improvements, including isolated analog and digital grounds with low-impedance paths. The Via-in-Pad technique was adopted to minimize parasitic inductance, improve signal integrity, and optimise spacing beneath the BGA. Performance evaluation demonstrated that the V3-HD-Hexaboard achieved an average noise of $\sim$0.93 ADC units and a Δ-pedestal of $\sim$2 ADC units for the bare board. When integrated into an HD silicon Hex-Module with 120 µm silicon, these values remained stable at $\sim$1.7 and $\sim$5.6 ADC units, respectively. In comparison, the NSH-Module with the same HGCROC-V3 ASICs exhibited significantly higher values of $\sim$2.5 and $\sim$175 ADC units, confirming that the V3-HD-Hexaboard fully complies with the HGCAL Technical Design Report (TDR) requirements.

The Hexaboard development followed an iterative process of prototyping, validation, and refinement. The final LD and HD versions achieved low noise, improved signal integrity, and compliance with HL-LHC requirements, ensuring reliable performance in high-precision detection.

Chapter 6

The Silicon Hex-Module Performance Evaluation

6.1 Introduction

This chapter presents a detailed evaluation of the CMS HGCAL silicon modules, focusing on beam test campaigns and laser-based timing characterization. The goal is to refine the module design and optimize performance to meet the stringent operational requirements of the HL-LHC. Key aspects covered include MIP detection with a targeted S/N as specified in the TDR, pedestal and common-mode noise corrections, stepwise design recommendations, timing resolution studies, and the comparison of experimental results with theoretical benchmarks.

The chapter begins with an overview of the beam test setup at the CERN SPS, described in Section 6.2. It then presents the beam test campaigns conducted in 2021 (BT2021), 2022 (BT2022), and 2023 (BT2023), detailed in Sections 6.3, 6.4, and 6.5, respectively. The corresponding results and key findings are discussed in Sections 6.3.1, 6.4.1, and 6.5.1. Based on these experimental insights, recommendations for Hexaboard design improvements are outlined in Sections 6.3.2, 6.4.2, and 6.5.2, guiding further optimization efforts.

The focus then shifts to silicon module characterization using a laser-based setup, described in section 6.6. This section discusses the calibration and synchronization of the laser system, which are necessary steps for accurate timing measurements. The findings offer valuable insights into the performance of individual silicon module channels and the overall timing resolution of the system.

In Section 6.6.1, factors influencing the timing resolution of silicon modules are explored in detail. The setup and methodology for conducting timing studies using the laser system are elaborated in section 6.6.3. Section 6.6.6 outlines the procedure for timing performance measurements and presents the results obtained from three representative channels of the silicon module. Furthermore, section 6.7 investigates the impact of temperature variations on timing resolution, providing insights into performance stability under different operating conditions.

A comparative analysis of experimental results with theoretical benchmarks, as outlined in the HGCAL TDR and ASIC design specifications, is presented in section 6.8. This section evaluates the alignment between experimental observations and design expectations, highlighting areas for optimization and refinement, while the causes of deviations are analyzed in section 6.8.

At the end of the chapter, in section 6.9, the extracted timing characteristics using the laser system are incorporated into full detector simulations to evaluate their impact on the reconstruction of neutral

hadrons (K_L^0) and photons (γ), as these particles rely solely on calorimetric measurements. The study simulates single-particle gun events with energies up to 120 GeV at pseudorapidity $\eta = 2$, focusing on the sensitivity of TOA resolution to shower efficiency and pileup mitigation. The chapter concludes by identifying opportunities for future improvements in silicon module performance, discussed in section 6.10. Collectively, this chapter establishes a comprehensive framework for evaluating and optimizing the silicon modules essential to the HGCAL system.

6.2 Silicon Hex-Module characterization in the Beam test

6.2.1 Motivation and goals

The HGCAL silicon Hex-Module evaluation in the beam tests serves several purposes. Primarily it provides an opportunity to characterise its response to real particle beams, facilitating validation of charge collection, timing performance, and overall detector behaviour under controlled test conditions. These studies further enable a systematic assessment of individual module components, including the silicon sensors, HGCROC front-end ASICs, readout printed circuit boards (Hexaboards), and thermally-conductive baseplates. The aim is to ensure that each components meets performance expectations for detection efficiency, data processing, and thermal management required for high-granularity calorimetric operation.

Calibrating the module using MIPs as a standard is another key goal. MIPs help standardize the module's response, essential for consistent and accurate data interpretation during actual operations. Similarly, beam tests facilitate checking the integration and overall functionality of the module within the broader HGCAL system, examining data synchronization, data acquisition systems, and power distribution in a controlled setting. The data collected during these tests are invaluable for refining detection algorithms and are a main source of feedback to the front-end electronics designer (ASICs, boards), ensuring that the module's design is accurate and effective.

The scope of this section of the chapter is to focus on the utilization of data derived from beam tests, which are critical and comprehensive assessments with widespread applications. It is important to mention at this stage, that plots relevent to beam test results have not produced by me, I was the part of beam test team, and participated in the data-taking and data-analysis and most of the plots have been made by other team members. The primary objective here is to analyze the beam test data to assess the silicon Hex-Module with a particular emphasis on the performance of the Hexaboard, the readout board of the silicon Hex-Module. This evaluation will consider the performance of these components in response to MIP and measure how closely the results align with the predefined target values of signal-to-noise ratio at various gains of HGCROC, listed in tables 6.1 and 6.2. Table 6.1 shows the expected values of charge, noise and signal-to-noise ratios for three types of silicon sensors with thicknesses of 300 µm, 200 µm and 120 µm at Start-Of-Life (SOL) and End-Of-Life (EOL) conditions, while table 6.2 lists the expected values of MIP in terms of ADC count at the three gain settings of the HGCROC. This analysis will address any discrepancies or issues by integrating feedback into the design of the Hexaboards to enhance their functionality.

Overall, these beam tests play a important role in ensuring that the HGCAL module is meticulously optimized and demonstrates the reliability required to meet the demanding requirements of HL-LHC phase.

6.2.2 Beam Test setup for HGCAL at Super Proton Synchrotron (SPS) CERN

The silicon Hex-Module performance evaluation has been conducted through three major beam test campaigns: September and October 2021, utilizing the NSH-Hex-Module (Non-Stepped-Hole silicon module); October 2022, with the V3-LD Hex-Module; and August and October 2023, employing V3-LD

Silicon thickness	300 µm	200 µm	120 µm
Area (cm^2)	1.26	1.26	0.56
Capacitance (pF)	48	69	54
Signal at start of life (SOL)	$\sim$ 22 ke	$\sim$ 15 ke	$\sim$ 9 ke
Charge at SOL (fC)	3.52	2.4	1.45
Preamp. Gain range (SOL)	160 fC	160 fC	160 fC
Noise (e-)	$\sim$ 2000	$\sim$ 2700	$\sim$ 2250
Expected S/N	$\sim$ 11	$\sim$ 5.55	$\sim$ 4.0
TDR value	11	6	4.5
Max Fluence	1E15	2E15	8E15
CCE at (EOL)	60%	70%	62%
Charge at EOL	$\sim$ 13.2ke	$\sim$ 10.5ke	$\sim$ 5.6ke
Leakage current (µA), $V_B = 600$ V (EOL)	9	12	13
Additional noise (adds in quadrature)	$\sim$ 1346e$-$	$\sim$ 1554e$-$	$\sim$ 1617e$-$
Preamp gain EOL	160 fC	160 fC	80 fC
Base noise (typical gain)	$\sim$ 2000$e-$	$\sim$ 2700e$-$	$\sim$ 2250$e-$
Total noise	$\sim$ 2410e$-$	$\sim$ 3115e$-$	$\sim$ 2770e$-$
S/N EOL	$\sim$ 5.5	$\sim$ 3.37	$\sim$ 2.02
S/N EOL TDR	4.7	2.3	2.2

Table 6.1: The table shows start-of-life (SOL) and end-of-life (EOL) electrical characteristics for the silicon Hex-Modules with different sensor thicknesses. It includes their cell sizes, capacitances, and the electrical signal produced by MIP at the SOL and EOL conditions, along with the expected noise and signal-to-noise ratio. The final performance is compared with the design specifications, mentioned in the TDR [6]. This information was presented by Dr. Philippe Bloch and A.Steen at the HGCAL Annual Review in 2023 [108] (slide 13).

HGCROC ADC gains	80 fC (High)	160 fC (Medium)	320 fC (Low)
01ADC unit = (Q-range/(ADC range-pedestal) assuming pedestal = 124	80 fC/900	160 fC/900	320 fC/900
ADC(fC)	$\sim$ 0.09 fC	$\sim$ 0.180 fC	0.350 fC
For 300 µm 1MIP = 3.52 fC	$\sim$ 39	$\sim$ 18	$\sim$ 10
For 200 µm 1MIP = 2.4 fC	$\sim$ 26	$\sim$ 13	$\sim$ 6.8
For 120 µm 1MIP = 1.45 fC	$\sim$ 16	$\sim$ 8	$\sim$ 4

Table 6.2: The table describes the estimated signal in ADC units, produced by the Muon, known as a minimum ionizing particle (MIP) at high, medium, and low gains setting of the HGCROC, with silicon thicknesses of 300 µm, 200 µm and 120 µm. The values are adjusted by mapping the available dynamic range (full range - pedestal) for an average pedestal of 124 ADC units and a full 10 bits ADC range (2^{10}) 1024 against the injected charge of 80 fC, 160 fC and 320 fC.

Hex-Modules (both full and partial) along with the V3-HD Hex-Module. All tests prior to the last campaign focused on single-module testing, utilizing data acquisition through the Trophy board (interface board between Hexaboard and Hexacontroler) and Hexa-controller systems. The August and October

2023 campaigns, however, transitioned to a multi-module setup, integrating the silicon Hex-Modules with ECONT ASICs on the concentrator mezzanine board and employing a DAQ system based on the Wagon and Engine boards concept. This thesis primarily focuses on the results obtained from the single-module beam tests.

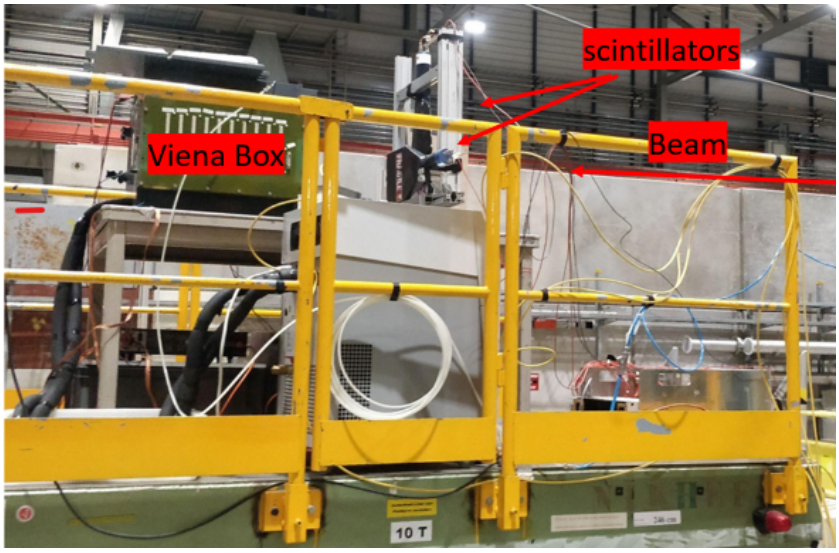


Figure 6.1: The experimental setup at the SPS CERN H2 beam line for the silicon Hex-Module beam test was conducted in September 2021. The particle beam enters from the right side of the setup, passing through the centers of a series of scintillators that are precisely aligned with the silicon Hex-Module housed within the environmental chamber, known as the Vienna box. This configuration ensures that the beam accurately targets the module for optimal data collection.

The setup used during the 2021 beam test campaign is illustrated in figure 6.1. A more detailed block diagram, depicting the connectivity of various components, is shown in figure 6.2, which is representative of all single-module beam test campaigns. The key elements of this setup are described below:

Beam Line: The HGCAL beam tests were conducted at the EHN1 Experimental Area in CERN's North Area, using the SPS as the primary accelerator. The 2021-2022 beam tests were performed on the H2 line, while the most recent campaign utilized the H4 line. Both beamlines share the same primary target, T2, and offer similar beam characteristics, as detailed in table 6.3. Both lines can supply beams of hadrons, electrons, and muons across a momentum range from about 10 to nearly 400 GeV/C, with varying purity levels to accommodate the diverse experimental needs [109, 110].

The secondary beam is produced by directing a 400 GeV proton beam from the SPS onto a 500 mm long beryllium target, generating secondary or tertiary particles, filter out through a combination of magnetic deflection and beam collimation. The selected particles then travel through dedicated beam lines, spanning approximately 540 meters for the H4 line and 590 meters for the H2 line guided by a meticulously arranged assembly of bending dipole magnets, focusing quadrupoles, and corrective elements, all of which steer the beam accurately toward the designated experimental area.

In configurations designed for electron and positron operations, particle production involves a two-stage conversion process. Photons from the decay of π^0 or η mesons, produced at the T2 target, proceed directly downstream and undergo pair production at a secondary lead target. Magnetic fields between the targets remove secondary charged particles, while a septum magnet at the start of the H4 beamline filters particles based on momentum and charge, guiding them toward the experimental setup [111].

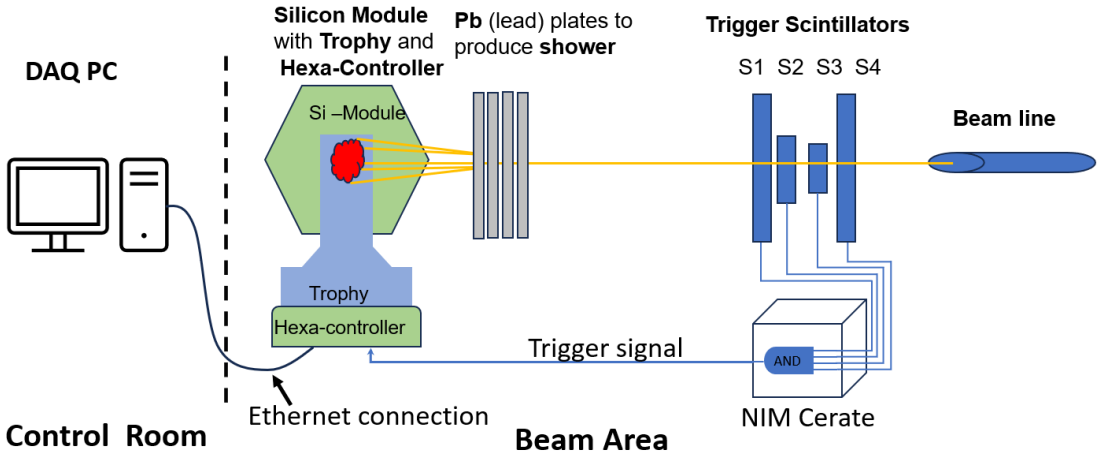


Figure 6.2: The beam test setup block diagram is true for all single-module beam setup for 2021, 2022, and 2023. The beam indicating H2 or H4 beam lines, the NIM Carte (Nuclear Instrumentation Crate), processed the four input signals from four scintillators (S1, S2, S3, and S4) and used the coincide logic to output a trigger pulse for the DAQ system, which consists of a Hexa-controller (FPGA part), and a trophy board (interface with a silicon Hex-Module). Pb (plates) are used for electromagnetic shower generation.

Parameters	Target: T2	
Beam Line	H2	H4
Maximum momentum (primary mode/secondary mode) (GeV/C)	400/360	400/330
Maximum acceptance (μSr)	1.5	1.5
Maximum Δp(p(%)	$\pm$2.0	$\pm$1.4
Max. intensity/spill (Hadrons/Electrons)	$10^7/10^5$	$10^7/10^6$
Ion beams	Y	Y
Available particle types	Primary proton / pure electron/ mixed hadrons/Muon	

Table 6.3: Beam parameters for the EHN1 beam lines[109]

Trigger Scintillators (S1 - S4): These scintillators are thin detectors arranged in sequence, producing a light flash when a charged particle passes through. The light is converted into an electrical signal by photomultiplier tubes or photodiodes. The output of these scintillators are then processed by a NIM crate to generate a valid trigger signal based on coincidence logic, which initiate a data acquisition process at DAQ- setup.

Lead (Pb) Plates: The lead plates are positioned between the silicon Hex-Module and the trigger scintillators. As a particle traverses the four scintillators, it generates a trigger signal that activates the readout circuitry. The particle then passes through the lead plates, where an electromagnetic shower is induced by the interaction of high-energy particles with the lead. This interaction produces secondary particles, which are subsequently detected by the silicon modules that form the core sensing elements of the calorimetric system.

silicon Hex-Module and Data Acquisition: The silicon Hex-Module (usllay knows as Hex-Module),

an essential component of the HGCAL, consists of a Hexaboard attached to a silicon sensor, Kapton foil, and a base-plate (detailed in Section 2.6). The data acquisition system includes the Hexacontroller, a customized board with a Trenz FPGA module, and the Trophy board, which serves as an interface between the silicon Hex-Module and the Hexacontroller. The readout chips of module captures charge and TOA information, digitizes it, and transmits it to the Hexacontroller, which then stores the data in raw format on the DAQ PC. This data is subsequently processed and analyzed to evaluate the silicon Hex-Module's performance.

This precisely engineered setup has been essential for the systematic characterization of silicon Hex-Modules under controlled test conditions.

6.3 Beam Test campaign 2021 with the NSH-LD-Hex Module

The beam test campaign conducted in 2021 employed the NSH-LD-Hex module, assembled with HGCROC-V2 and HGCROC-V3 ASICs and a 300 µm thick n-on-p silicon sensor. The module and its readout configuration includes the Trophy-V2 board and Hexa-controller, as depicted in figure 6.3. The assembly is mounted on a copper cooling plate that is suspended vertically within the Vienna cooling box, strategically positioning the silicon Hex-Module in alignment with the beam line. Over the course of the week-long campaign, substantial efforts were dedicated to optimizing the delay settings and calibrating the module.

During the test beam campaign, electron beams with energies ranging from 20 GeV to 250 GeV were used in two configurations: with and without absorber plates. The absorber setup created a wide beam spot and served two main purposes—to align the beam with the silicon module by identifying strong central signals, and to generate electromagnetic showers for future physics analyses. For MIP detection, a configuration without absorbers was selected to deliver a narrow and focused beam targeted at a specific silicon cells.

In the first part of beam test (Sep. 2021), NSH-LD-Hex-Module-V2 (assembled with HGCROC-V2) was used. At 200 GeV, the incident electron beam was detected by the silicon Hex-Module; however, no MIP signal was observed. This is likely due to limitations of the HGCROC-V2 chip, which was not capable of handling multiple Level-1 Accept (L1A) trigger signals, used by the trigger system to release stored data from specific memory locations within the HGCROC. Possible malfunctions in the data acquisition software may have also contributed to this absence of MIP signal.

In the second part of the campaign (Oct. 2021), another NSH-LD-Hex-Module-V3 (assembled with HGCROC-V3 ASIC) was used. The pedestal noise and Δ-pedestal values were 6 and $\sim$ 180 ADC units, respectively, as shown in figures 6.4 and 6.5. Although the noise and Δ-pedestal values were worse compared to NSH-LD-Hex-Module-V2, with noise and Δ-pedestal values of approximately 4 and $\sim$17 ADC units respectively (see figure 5.17), the acquisition software successfully detected MIP signals in 100 GeV electron beams without absorbers. Data were acquired at two different gain settings of the HGCROC-V3: a low-gain configuration with an ADC range corresponding to 320 fC, and a medium or typical gain setting where the full ADC range maps to 160 fC.

6.3.1 Achievements and results

Key achievements from the 2021 beam test include the development of effective methodologies for pedestal and common mode noise correction.

Pedestals and Common Mode noise Correction

Pedestals correction: Pedestals, represents the mean of baseline voltage levels of the HGCROC channels in the absence of a signals, are fundamental feature for accurate data analysis. Ideally, these baseline

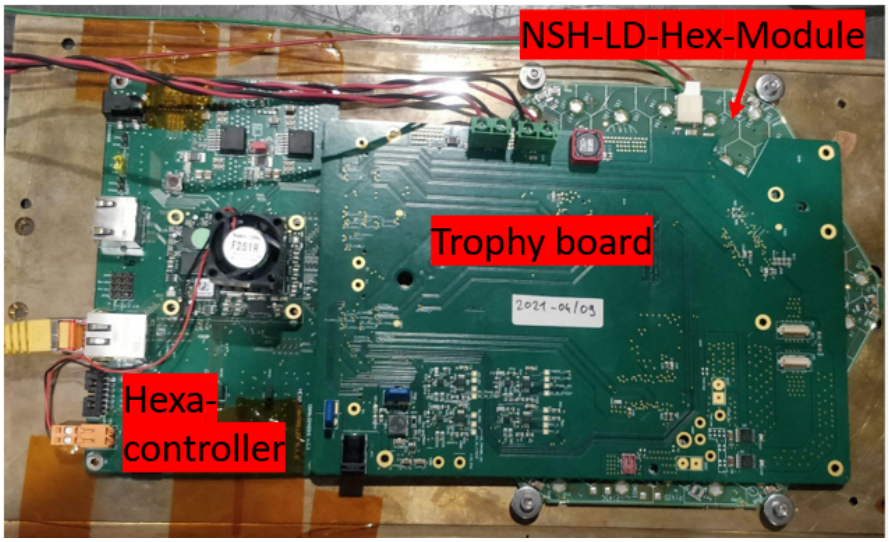


Figure 6.3: NSH-LD-Hex Module prepared for the beam test. The silicon Hex-Module, assembled on a copper cooling plate, is readout by a single module setup including the Trophy-V2 and Hexa-controller, connected to the DAQ PC via Ethernet.

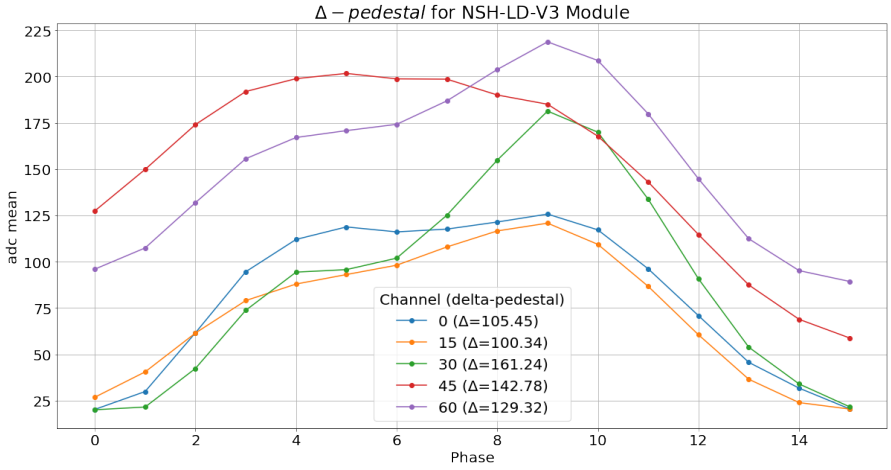


Figure 6.4: Pedestal variation (Δ-pedestal) as a function of phase for the NSH-LD-Hex-Module-V3. This figure presents the mean ADC values across multiple channels, emphasizing the shifts in pedestal levels with varying phases. The Δ-pedestal values represent the difference between the maximum and minimum points for each channel, serving as an indicator of digital noise superimposed on the analog signal.

values exhibit a Gaussian distribution, with their standard deviation reflecting the electronic noise of the system. Each new beam test configuration, whether due to changes in beam settings or HGCROC parameters, requires a dedicated pedestal run. The data from these runs serve as a reference for correcting subsequent signal data.

However, it was observed that pedestal levels vary between beam-on and beam-off conditions, and

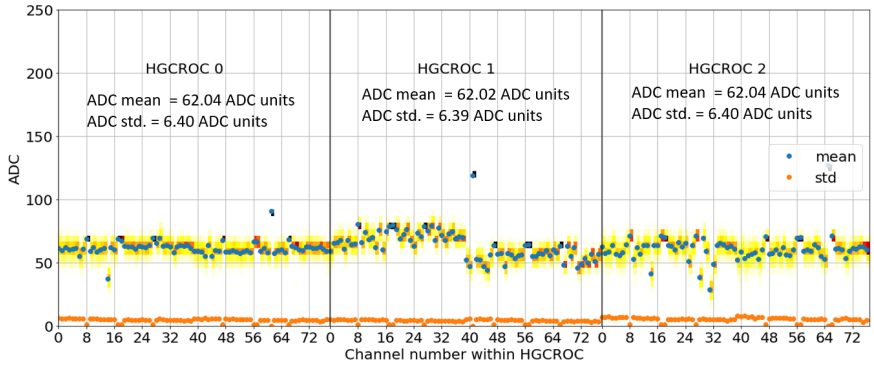


Figure 6.5: Noise profile of the NSH-LD-Hex-Module-V3 across three HGCROC chips. The figure shows the mean ADC (pedestals) values and standard deviations (noise) for each channel, highlighting consistent performance and stable noise levels critical for reliable data acquisition.

even between sub-runs within the same beam configuration. To address these inconsistencies, two correction procedures were developed:

1. **Pedestal Run Subtraction:** This method relies on data from a dedicated pedestal run:

- A pedestal run was taken for each beam configuration to measure the baseline of every channel. The pedestal value, computed as the median of the ADC values over all events, provided a stable reference.
- During beam test data analysis, the corresponding pedestal value was subtracted from each channel's ADC data to remove baseline offsets and accurately reconstruct the true signal.

2. **Beam Run Pedestal Subtraction:** This method uses data directly from the beam run:

- For each channel, the pedestal is determined by computing the median ADC value from the preceding time window (referred to as Bx–1, or the previous bunch crossing), denoted as `adcm`, corresponding to a 25 ns interval prior to the event. Although no actual bunch crossings occur in this setup, the data format adheres to the LHC convention, where each BX represents a 25 ns sampling window. The ADC values from the current BX are then corrected by subtracting the corresponding pedestal values.

In both methods, the pedestal correction for common mode (CM) channels is applied using the median ADC value from the current 25 ns time window (Bx). This is required because CM channels do not contain ADC information from the preceding time window (Bx–1), commonly referred to as adcm, within the data frame (see DAQ frame in figure 3.14).

These correction methodologies ensure that signal readings are accurately adjusted according to reliable baseline measurements, enhancing the precision of data analysis across varying experimental conditions.

Common Mode corrections: Accurate data analysis and signal reconstruction in the HGCAL system require effective subtraction of common mode noise. The readout chip of the silicon module, HGCROC chip encompasses 72 normal channels, four common mode (CM) channels, and two calibration channels (see section 3.3).

In the LD silicon Hex-Modules, 8 channels for ech HGCROC, are not connected to sensor pads nor routed on the Hexaboard, and designated as not-connected (NC), while the remaining 64 channels are

	Beam	HV	LV
Conn	✓	✓	✓
CM	×	✓	✓
NC	×	×	✓

Table 6.4: Sources of common mode noise and their correlation with HGCROC channels. 'Connected' (Conn) channels are affected by the Low Voltage (LV) supply, Bias Voltage (BV) for the sensor, and by the incident beam. 'Common Mode' (CM) channels are influenced by both the chip's power LV and the BV, while, the 'Non-Connected' (NC) channels only experience the effects of the LV.

connected (Conn) to the silicon sensor . The Common Mode (CM) channels are AC-coupled to the Bias Voltage (BV) supply. These different input types, Connected, Not Connected and Common Mode are influenced by distinct common mode noise sources, primarily the Low Voltage (LV) and Bias Voltage (BV) supplies. A summary of these coupling sources are summarised in Table 6.4 and briefly discussed below:

- **Low Voltage (LV) Supply:** Powers the HGCROC ASIC and affects all channel types, including Connected, Not-connected, and Common Mode channels.
- **Bias Voltage (BV):** Biases the silicon sensor and may introduce cross-talk between connected channels over extended distances.
- **Beam:** Directly impacts the silicon cells struck by the beam, as well as adjacent cells through short-range coupling.

To ensure precise signal reconstruction and analysis, the following algorithm was developed for processing the HGCAL beam test data:

1. Median ADC values from not-connected NC channels are used to correct the Conn and CM channels, effectively removing the contribution from the Low Voltage supply.
2. The NC-corrected Common Mode channels are then subtracted from the NC-corrected Connected channels to eliminate the common mode noise introduced by the Bias Voltage.

This method ensures that the signals are accurately reconstructed and clean from common mode noise to allow reliable data analysis under various experimental conditions.

This algorithm ensures precise correction by systematically eliminating noise through each step, allowing for clearer identification and analysis of the true signal. The application of above mentioned procedures is shown in figure 6.6. The figure comprises scatter plots and a histogram that illustrate the validation of pedestal and common mode noise corrections.

- **Scatter Plots (Left and Center):** The left scatter plot highlights a strong correlation ($corr = 0.847$) between pedestal-subtracted common mode (CM_pedsub) and pedestal-subtracted connected (conn_pedsub) channels, reflecting the significant influence of these noises before correction. The center plot, following the common mode correction (subtracting CM_pedsub from conn_pedsub), shows a noticeable reduction in correlation, indicating the effectiveness of the correction methods in minimizing both pedestal and common mode noise.
- **Histogram:** The histogram illustrates the distribution of ADC values and their standard deviations (σ) across different correction modes:
  - **conn_pedsub (Blue):** Data corrected using only pedestal subtraction.

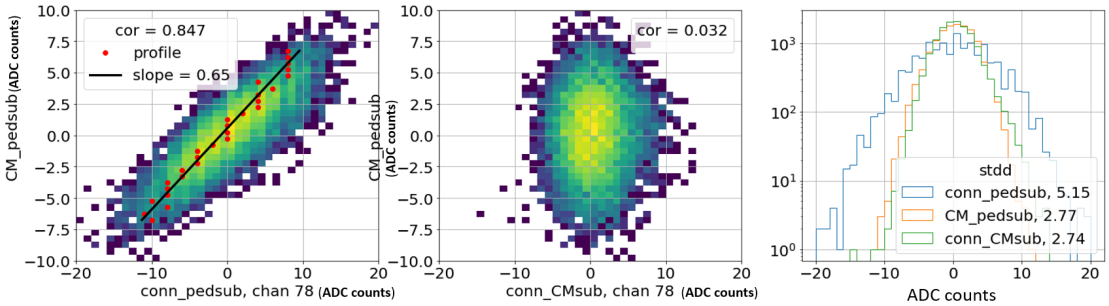


Figure 6.6: Validation of pedestal subtraction and common mode corrections procedures are shown for channel with chan_id = 78. The scatter plots at left and middle depicts the correlation between pedestal subtracted common mode (CM_pedsub) and pedestal subtracted connected channels (conn_pedsub) before and after CM corrections. A zero (0.032) correlation after correction confirms the effectiveness of the correction procedures. The histogram on the right shows the distribution of ADC values with respective standard deviation, stdd (σ) values for various correction methods, highlighting their impact on signal clarity.

- **CM_pedsub (Orange):** Data corrected using only common mode subtraction.
- **conn_CMsub (Green):** Data corrected using both pedestal and common mode subtraction.

The green curve, representing `conn_CMsub`, demonstrates the most effective noise reduction, resulting in a significantly clearer signal.

Figure 6.7 demonstrates the application of various pedestal and common mode noise correction techniques on data collected with a 100 GeV beam, under a configuration without an absorber. These techniques significantly reduce noise levels, enhancing the visibility of the MIP signal. The dashed vertical line indicates the proposed ADC threshold for each distribution, positioned at the local minimum within the 0–20 ADC unit range, to enable efficient separation between signal and background contributions. The illustration underscores that merely subtracting the pedestal or the contribution from non-connected (NC) channels is not enough for clear signal identification. However, as indicated by the red (adc_CMsub) and green (adc_NCCMsub) traces, applying common mode (CM) subtraction effectively cleans the signal, distinctly separating it from the noise. The figure also reveals that both CM correction methods yield satisfactory results. Therefore, in the context of High-Density silicon Hex-Modules, where HGCROC lacks non-connected pins, CM correction alone proves to be sufficient for accurate signal identification.

MIP (Minimum Ionising Particle) signal detection

To evaluate the detector response to minimum ionizing particles (MIPs), data from a 100 GeV electron beam without absorber were analyzed. Prior to signal extraction, pedestal and common mode corrections were applied to suppress baseline and noise contributions. The optimal acquisition window was determined through the `trigphase` parameter, which corresponds to an internal timer operating at a clock frequency of 1.28 GHz, wherein each tick represents 0.781 ns. This timer is initiated by the rising edge of the scintillator trigger signal. The Fast Command firmware block, responsible for issuing control commands to the HGCROC, subsequently generates the Level-1 Accept (L1A) signal synchronously with this timing reference.

Figure 6.8 shows the corrected ADC distributions for two gain settings: 320 fC (low gain, left) and 160 fC (default gain, right). The MIP peaks are observed at approximately 9 and 18 ADC units, respectively, consistent with the expected values for a 300 µm thick silicon sensor as listed in Table 6.2.

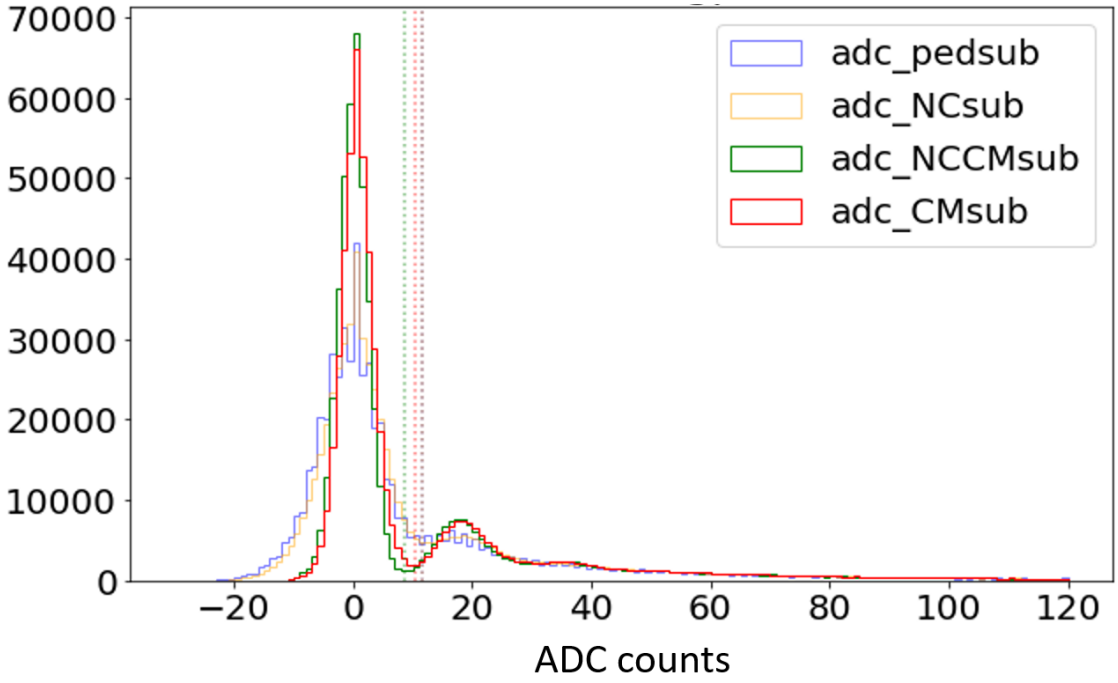


Figure 6.7: Comparison of different Common Mode and Pedestal correction algorithms applied to Beam Test 2021 data. The figure illustrates the impact of various correction methods pedestal subtraction (adc_pedsub), non-connected channel subtraction (adc_NCsub), combined non-connected and common mode subtraction (adc_NCCMsub), and common mode subtraction (adc_CMsub) on the ADC distribution. The results demonstrate the effectiveness of each approach in reducing noise and refining the signal, with common mode correction methods providing the most significant improvement in signal clarity. Dashed lines mark suggested ADC cuts, chosen at the local minimum between 0 and 20 units to separate noise from signal.

The calculated signal-to-noise ratios are approximately 9.9 for the default gain and 7.9 for the low gain configuration. While the S/N of 9.9 approaches the expected performance, it remains slightly below the target value of 11, as specified in the CMS HGCAL Technical Design Report [6] and summarized in Table 6.1. The observed deviation underscores the necessity of optimizing the Hexaboard design, with a particular focus on minimizing electronic noise to improve the signal-to-noise (S/N) performance of the system.

6.3.2 Recommendation for Hexaboard design

The NSH-hexaboard-based silicon Hex-Modules assembled with HGCROC V2 and V3 were used for the first time in beam tests. During these tests, it was observed that digital modulation, measured as Δ-pedestal, was significantly greater in NSH-LD-Hex-Module-V3 than in NSH-LD-Hex-Module-V2. This modulation triggered random activations of the TDCs, introducing substantial noise into the system, which rendered the TOA TDCs unusable in the Beam test of 2021. These findings prompted further investigation, ultimately leading to design recommendations for both the hexaboard and ASIC packaging (see Section 5.11 for more details). Key recommendations included isolating the return paths for digital and analog currents in the ASIC package and on the top layer of the Hexaboard, alongside a transition to 'Via in Pad' designs for Hexaboards utilizing HGCROC in the HD package

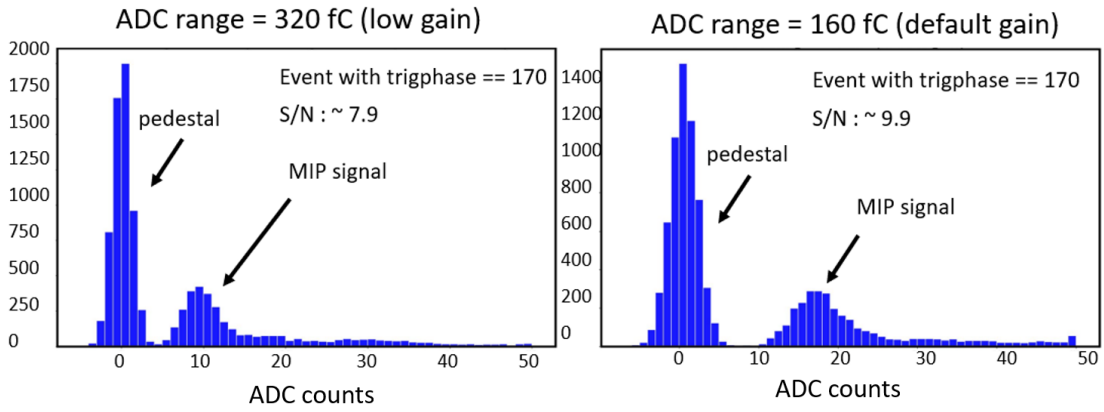


Figure 6.8: MIP signals after pedestal and common mode corrections for 160 fC (default gain) and 320 fC (low gain) settings. The histograms show the pedestal and MIP signal peaks with corresponding signal-to-noise ratios (S/N) of 9.9 and 7.9, respectively.

6.4 Beam Test campaign 2022

The Beam test 2022 was conducted with the V3-LD-Hex-Module shown in figure 6.9, assembled with the optimally designed V3-LD-Hexaboard (see sec 5.8) and utilized the LD-packaged HGCROC-V3. The noise comparison with NSH-LD-Hex-Module-V2 is shown in figure 6.10, which reveals that average noise for V3-LD-Hex Module is less than NSH-LD-Hex-Module-V2 and has an average value of 2000 electrons, which is within the specification mentioned in TDR [6] and table 6.1. All the beam test setup details are listed in table 6.5

silicon Hex-Module	V3-LD-Hex-Module with HGCROC-3A and 300 um thick sensor
HGCROC Gain setting	80 fC (high gain), 160 fC (typical gain), 320 fC (low gain)
Beam types used	Electron beam: 20 GeV to 250 GeV Muon beam: 150 GeV Pion beam: 150 GeV
Absorber plate configuration	Pb plates Infront of module (upstream) Pb plates after of module (downstream) No plate
Module powering scheme	Operated with DCDC module The Bias voltage for silicon was -270 V Leakage current: 5 uA

Table 6.5: Summary of Beam test 2022 setup and operational parameters for the V3-LD-Hex-Module with HGCROC-3A, including gain settings, beam types, absorber configurations, and module powering details.

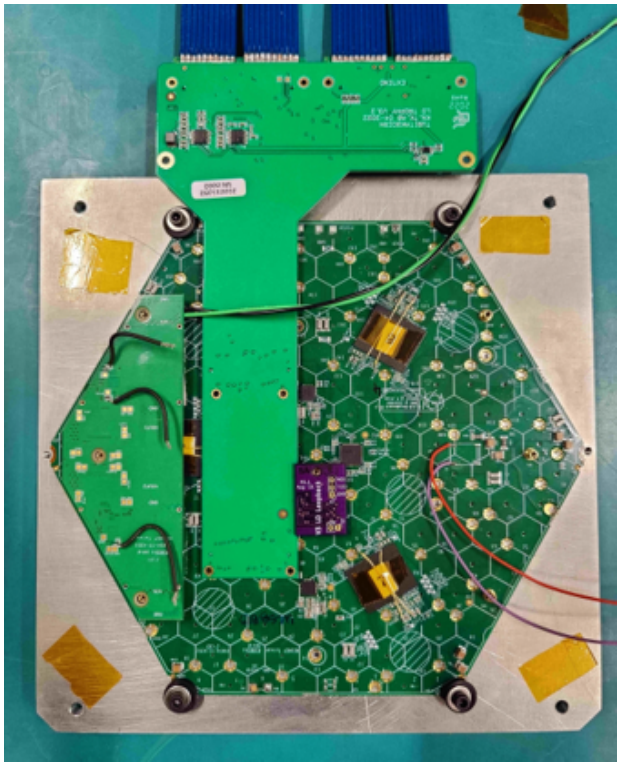


Figure 6.9: V3-LD-Hex-Module equipped with a 300 µm sensor, as utilized in the Beam Test 2022.

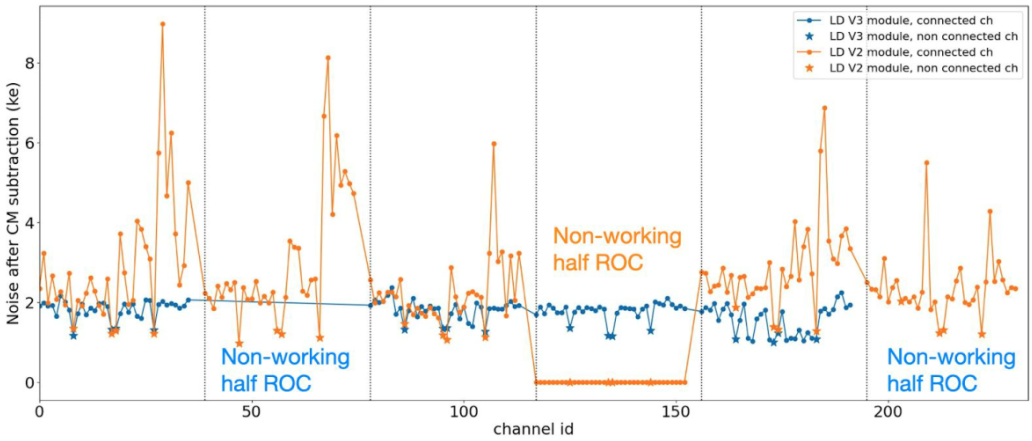
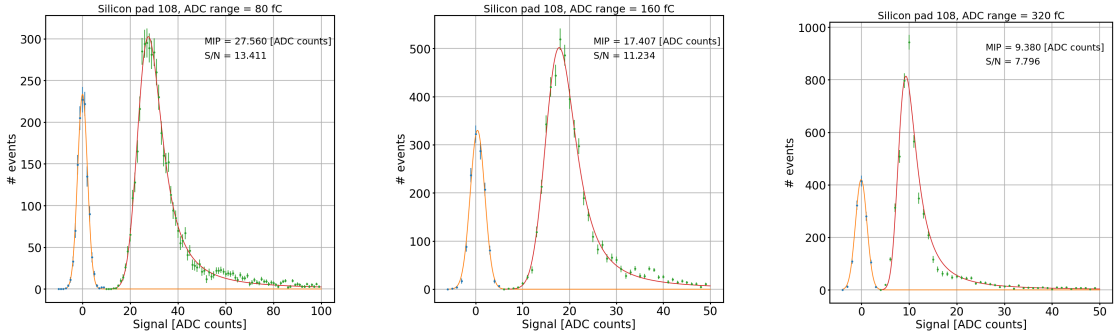


Figure 6.10: Noise comparison between the V3-LD-Hex module and the NSH-Hex-Module-V2 after common mode subtraction. The figure highlights the differences in noise levels across connected and non-connected channels, with notable sections of non-working half ROC in both modules. These regions were initially damaged by an unknown cause, which was later confirmed to be due to electrostatic discharge (ESD).

6.4.1 Achievement and results

The 150 GeV pion beam data, collected without an absorber, was selected for analysis due to the beam's narrow profile, with a diameter of less than 1 cm. This narrow beam allowed for precise scanning of individual cells within the silicon Hex-Module. The movable table at the H2 beam line further facilitated the irradiation of multiple cells, enabling a comprehensive evaluation of the module's response.

Figure 6.11 depicts the pedestal and MIP signal distribution for silicon Hex-Module cell_Number = 108 for three different HGCROC gains, with MIP values of ~ 27, ~ 17, ~ 9 ADC units, while Signal-to-noise ratio ~ 13, ~ 11, ~ 8 for high , medium and low HGCROC gains respectively. Detail statistics for ~ 29 cells shone with beam for all three gains are shown in figure 6.12 and table 6.6. The results depict that the average value for MIP (ADC unit) and S/N for three gains (starting from High) are ~ 30, 14.5 and ~ 18, 13 and ~ 9, 8.6 respectively. Its also observed that there is $\sim 4\%$ dispersion in the MIP value among the three chips. This could be because of dispersion of individual channels gain and the incident angle of beam varies due to some mechanical mis-alignment between module and beam.

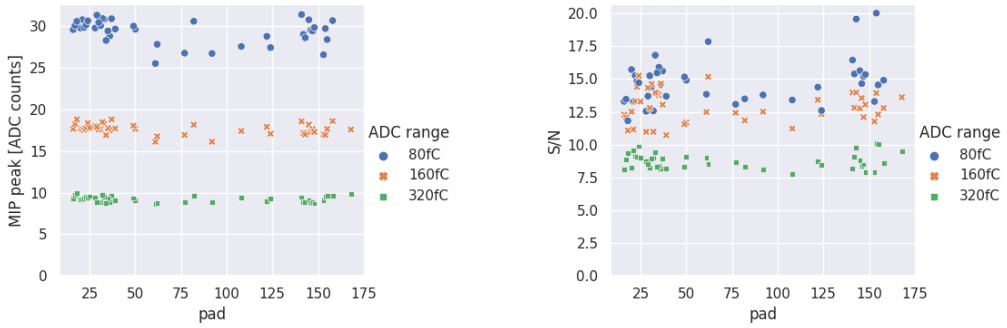


(a) Pad 108 at Hi gain (b) Pad 108 at Medium gain (c) Pad 108 at Low gain

Figure 6.11: Signal-to-Noise ratio (S/N) for Pad 108 under a 150 GeV pion beam at three HGCROC gain settings: (a) High gain (80 fC): MIP peak at 27.560 ADC counts with S/N = 13.141. (b) Medium gain (160 fC): MIP peak at 17.407 ADC counts with S/N = 11.234. (c) Low gain (320 fC): MIP peak at 8.390 ADC counts with S/N = 7.795.

gain	chip	MIP(mean)	MIP(std)	S/N(mean)	S/N(std)	nPad
80	0	30.01	0.76	14.61	1.18	15
80	1	28.47	1.59	14.12	1.07	8
80	2	30.05	0.63	15.15	0.38	5
160	0	17.8	0.4	13.18	1.29	16
160	1	17.49	0.81	12.28	0.75	8
160	2	17.8	0.58	12.86	0.53	5
320	0	9.31	0.32	8.8	0.54	16
320	1	9.17	0.28	8.51	0.43	8
320	2	9.0	0.39	8.43	0.34	5
80	all	29.58	1.23	14.57	1.08	28
160	all	17.71	0.56	12.88	1.11	29
320	all	9.22	0.33	8.66	0.5	29

Table 6.6: The noise and MIP values of different cells of V3-LD-Hex-Module for 150 GeV pion beam



(a) MIP signals for different cells at different gains

(b) S/N for different cells at different gains

Figure 6.12: Detailed analysis of the V3-LD-Hex-Module's response to a 150 GeV pion beam, highlighting the MIP signal mean values (a) and Signal to Noise Ratio (S/N) (b) across various cells at different ADC gain settings. This investigation serves to characterize the module's electronic performance under varied operational conditions, illustrating both the resilience and sensitivity of the sensor technology.

6.4.2 Recommendation for the Hexaboard designs

The results were encouraging as they meets both specification, the noise is less than 2000 electrons and S/N for MIP reaches 13 against the target value of 11. The results validate the version of the hexaboard and was a go-ahead signal for pre-series production of V3-LD-Hexaboards.

6.5 Beam Test campaign 2023

This Beam test campaign was held in Aug and Sep 2023. Four silicon Hex-Modules, 1 x V3-LD-Hex Module (Full) with 200 µm sensor, 1 x V3-HD-Hex Module (full) with 120 µm and two V3-LD SEMI partials (left and right) modules assembled with 300 µm sensor were used for the validation. These assembled modules, along with their Trophy and Hexacontroller-based single-module readout setup, are shown in figure 6.13. The modules and beam parameters, are described in Table 6.7. Various types of beams with different energies were used in different configurations, such as with and without absorbers, and different gain settings of the HGCROC. The bias voltages were set at -250 V, -200 V, and -150 V for V3-LD partial, V3-LD full, and HD-full Hex-Modules respectively.

Single modules Beam test Aug and Sep-2023 at H4 beam line, SPS CERN	
Four silicon Hex-Module types Were used:	(I)- V3-LD-Hex-Module with HGCROC-3A (LD package) with 200 µm thick sensor. (II)- V3-HD-Hex-Module with 120 µm thick sensor, HD-package. (III)-V3-LD-SEMI-partial-Left with 300 µm thick sensor (IV)-V3-LD-SEMI-partial-Right with 300 µm thick sensor
HGCROC Gain setting	80 fC (high gain), 160 fC (typical gain), 320 fC (low gain)
Beam types used	Electron beam: 20 GeV to 200 GeV Muon beam: 150 GeV (long over-night run)
Absorber plate configuration	10 mm × 5 mm thick Pb plates In front of module No plate, with 100 GeV electron beam to scan individual cells
Module powering scheme	Operated with baseline schemes The Bias voltage V3-LD partials with 300 um sensor : -250V V3-LD full of 200 um sensor : -200V V3-HD full of 120 um sensor : -150V

Table 6.7: Setup and operational parameters of the 2023 beam test campaign.

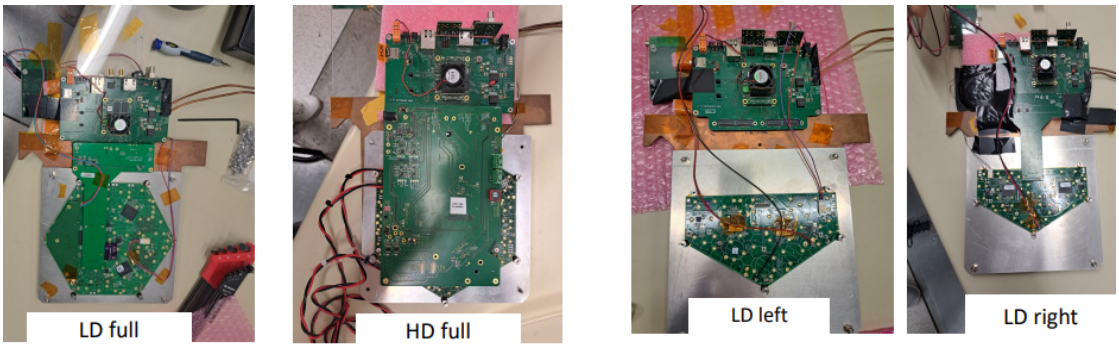


Figure 6.13: The silicon Hex-Modules, LD-Full, HD-Full, LD-SEMI-Left and LD-SEMI-Right partial used in single module beam test in Sep-2023.

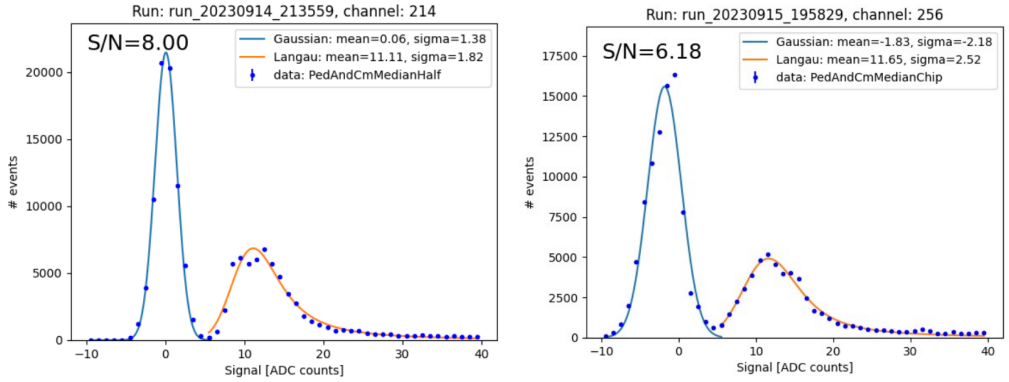
6.5.1 Achievement and results

Electron beams with energies of 40 GeV, 100 GeV, and 200 GeV were directed into the central region of each silicon module to ensure the resulting electromagnetic showers were align and centered within the sensitive area of the sensor. For spatial response characterisation, additional scans were performed using 200 GeV beams targeted at multiple positions across the surface of the modules. In all these configurations, lead (Pb) plates were introduced into the beamline to initiate electromagnetic shower development.

To evaluate the front-end electronics performance, in particular the noise behaviour and MIP signal detection capability, a 100 GeV electron beam was employed without absorber plates. This configuration enabled precise localisation of the beam within individual silicon sensor cells, allowing accurate measurement of the MIP response. The signal distributions, expressed in ADC counts, were acquired from each module. The electronic pedestal was fitted using a Gaussian function, while the MIP peak was extracted from the corresponding Landau distribution. These fits were subsequently used to compute the Signal-to-Noise (S/N) ratio, as illustrated in figure 6.14.

Figure 6.14(a) and (b) show the signal distributions in ADC counts for the LD-Full module with a 200 µm silicon sensor and the HD-Full module with a 120 µm sensor, yielding Signal-to-Noise (S/N) ratios of 8.0 and 6.18, respectively. These results exceed the corresponding design targets of 5.5 and 4.0. Likewise, figure 6.15(a) and (b) present the ADC signal distributions for the LD-SEMI Left and Right partial modules, both assembled with 300 µm thick sensors. The measured S/N values of 10.6 and 11.0 are in excellent agreement with the specified target of 11.0.

All measurements were conducted under start-of-life conditions with typical gain settings applied to the front-end electronics. A summary of measured versus expected noise and S/N performance is provided in Table 6.8, confirming that all tested module configurations meet or exceed the targeted specifications. These results validate the design and integration quality of the Hexaboard modules in a controlled beam test environment.



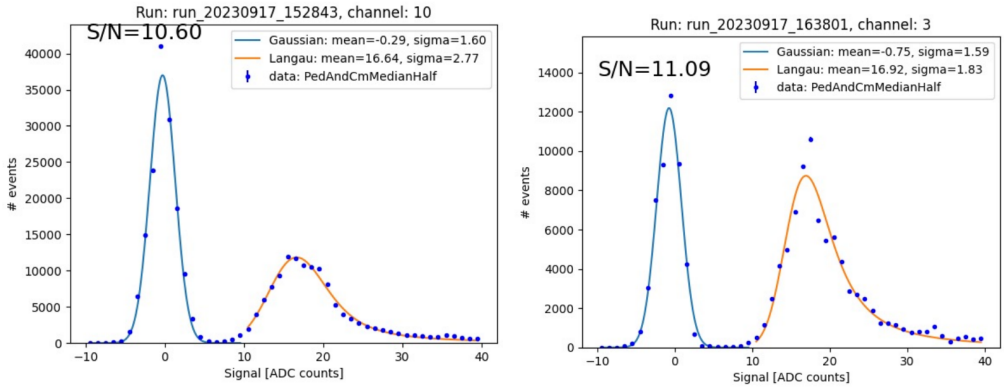
(a) MIP at in LD-Full with 200 µm sensor against 100 GeV electron

(b) MIP in HD-Full with 120 µm against 100 GeV electron

Figure 6.14: Signal (in ADC counts) distribution for Full LD module with 200 µm silicon sensor (left) and for Full HD module with 120 µm silicon sensor (right), both irradiated with a 100 GeV electron beam (without absorbers).

6.5.2 Recommendation

All Hexaboard designs have undergone a rigorous validation process, combining detailed simulation-based design verification with extensive laboratory characterisation. However, beam test campaigns pro-



(a) MIP signals in LD-SEMI-Left against 100 GeV electron

(b) MIP signals in LD-SEMI-Right against 100 GeV electron

Figure 6.15: Signal (in ADC counts) distribution for LD-SEMI-Left module (left) and LD-SEMI-Right module (right), both assembled with 300 µm silicon sensors and irradiated with a 100 GeV electron beam (without absorbers).

Module type	HGCROC	Noise	Noise expected	S/N measured	S/N expected
HD full (120μm)	HD V 3	2000	2250	4.8	4.5
LD full (200μm)	LD V3	1900	2700	8.4	6
LD semi right (300μm)	LD V3	2000	2000	12	11
LD semi left (300μm)	LD V3	1950	2000	12.2	11

Table 6.8: Noise and Signal-to-Noise (S/N) ratios for different silicon Hex-Modules across various HGCROC configurations, with comparisons between measured and expected values. The results in table confirms that these modules meet design specifications, and hence validating the Hexaboards designs.

vide a more realistic and comprehensive evaluation of module performance under operational conditions. Out of the eleven distinct Hexaboard designs, four have been successfully validated in beam tests. Notably, the full-size designs—both Low Density (LD) and High Density (HD)—which together constitute approximately 95% of the total production volume, have been thoroughly assessed. The HD variant, featuring a 120 µm thick silicon sensor and designed for deployment in high-radiation inner regions, as well as the LD variants with 200 µm and 300 µm sensors targeted for the middle and outer layers of the HGCAL, have all demonstrated stable performance. These modules were tested under multiple configurations, including with and without absorbers, and exposed to various beam types and energies. The satisfactory results obtained across all test conditions have qualified these designs for advancement to the production or pre-production stages.

Thus far, only 2 of the 9 partial designs have been tested with beam exposure, and the remaining designs are likely to be the focus of upcoming beam tests.

My focus was concentrated on noise and MIP detection with good S/N, particularly lies in the ADC region, to assess the lower detection limits. TOT measurements and calibrations were conducted as part of the Beam Tests 2022 and 2023 campaigns and will be essential for future shower physics analyses.

One key aspect of the design verification, is the timing validation, involves TOA data. This data was not utilized during BT21 due to limitations in the TOA TDC. While TOA was used in BT22 and BT23, the calibration procedures were not fully developed. Consequently, the analysis of timing data is ongoing and will be a primary focus in the next section of this chapter, which involves the utilisation of the laser

system for timing performance of the silicon Hex-Module.

6.6 Silicon Hex-Module characterization with Laser setup

The HGCAL aims to operate during HL-LHC with unprecedented precision in particle detection and measurement. Studies show that with 140-200 pileup, there will be a spread of interaction vertices over ± 50 mm along the beam axis, and over ± 150 ps in time. Detector simulation studies indicate that the physics potential can be improved by mitigating event pileup through time-tagging with a precision of ~ 30 ps (RMS) [112, 113]. Incorporating the precision timing of the recorded events will significantly enhances the reconstruction process by effectively rejecting pileup and precisely identifying the primary vertex. The HGCAL has chosen the scheme to incorporate the time tagging of incoming particle which make it 5D calorimeter capable of measuring Energy, position(x,y,z) and time.

When an incident particle passing through the silicon depleted volume, it generate electron-hole pairs which are swept to the electrodes by the applied Electric filed. As detailed in Chapter 3, the front-end readout ASIC, HGCROC, is responsible for measuring both the charge deposited in the silicon sensor by an incident particle and the time-of-arrival (TOA) of that signal. This is achieved using a 10-bit Analog-to-Digital Converter (ADC) (sections 3.4.3) and two 10-bit Time-to-Digital Converters (TDCs) (section 3.4.5.) embedded within each channel. Figure 6.16 illustrates an example of such a measurement for a single channel, showing the reconstructed charge and timing information.

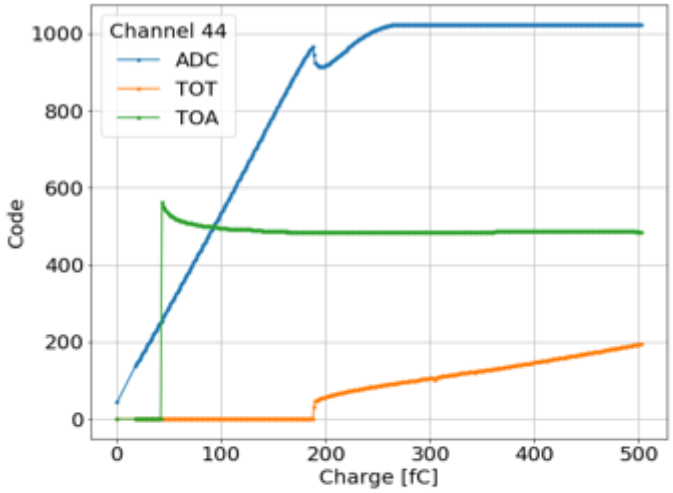


Figure 6.16: HGCROC Front-end charge and timing measurements: An ADC (blue) read charge till $\sim$ 160 fC and then the TOT TDC activates(orange). The TOA TDC (green) measures the time of arrival (TOA) when a certain threshold crossed.

The charge is initially digitised by the on-chip ADC operating within the linear range of the preamplifier, up to approximately 160 fC under medium gain settings. Once the preamplifier saturates, the Time-Over-Threshold (TOT) TDC assumes control of the charge measurement by evaluating the duration for which the signal remains above a defined threshold. The TOA measurement is initiated when the input pulse exceeds the TOA discriminator threshold (V_{ref}-TOA) at which point a discriminator pulse is generated to trigger the time digitisation circuitry. This timing chain consists of a 2-bit Gray code counter running at 160 MHz, a 5-bit coarse TDC with a resolution of 195 ps, and a 3-bit fine TDC for residual phase correction. Together, these components form a 10-bit TDC architecture, covering a 25 ns bunch crossing interval with 1024 ticks, yielding a bin size of 24.5 ps. An optional 11^{th} bit can be enabled to further enhance the resolution to 12.25 ps. This timing precision is critical for accurate event time-

tagging, effective pileup suppression, and overall high-performance operation of the HGCAL system under HL-LHC conditions.

For the timing study discussed in this second half of the chapter, laser light will be injected into the silicon Hex-Module. The injected charge will be reconstructed using ADC and TOT data, while the TOA will be measured. This process will allow us to determine the dependencies of the TOA on the injected charge, enabling the extraction of charge-dependent corrections and time resolution for the specific channel in the silicon Hex-Module.

6.6.1 Time Resolution

Time resolution of a detector refers to the precision with which the arrival time of a particle can be measured. High time resolution is crucial for accurately distinguishing between events that occur in rapid succession, especially in the high pileup situations of the HL-LHC. The overall time resolution of a timing detector "σ_t" is influenced by several factors, each contributing to the total timing uncertainty. These contributing factors include electronic noise (jitter), Time-Walk, Landau noise, signal distortion, and TDC binning. The total time resolution can be expressed as the quadrature sum of these individual components are shown in equation 6.1, taken from [113]:

$$\sigma_t = \sqrt{\sigma^2_{\text{jitter}} + \sigma^2_{\text{TimeWalk}} + \sigma^2_{\text{Landau}} + \sigma^2_{TDC}}, \tag{6.1}$$

Where the different contributions are explained below:

Noise Jitter σ_{jitter} is the signal timing variation due late or early triggering of the discriminator due to electronics noise as shown in figure 6.17 (left) where the variation in electronics signal amplitude crossing threshold V_T is transformed into variation in time at which the threshold is being crossed.

The timing jitter σ_j, defined as the uncertainty in the signal crossing a fixed threshold due to voltage noise N, is given by:

$$\sigma_j = \frac{N}{\frac{dV}{dt}} \approx \frac{N}{V_{\text{signal}}/t_r} = \frac{t_r \cdot N}{V_{\text{signal}}} = \frac{t_r}{S/N}, \tag{6.2}$$

where t_r is the signal rise time, V_{signal} is the signal amplitude, and S/N is the signal-to-noise ratio. This expression shows that the time jitter improves with faster rise times and higher signal-to-noise ratios.
Time-Walk and Its jitter: Time-walk phenomena can be defined as the dependence of measured time intervals of incoming signals or events on the amplitudes or shapes of the signals. Figure 6.17 (right) explains Time-Walk using three input signals of different amplitudes, originating from the same time T_0. The signal with the largest amplitude has a faster slew rate, and thus crosses the threshold earlier than the signals with lower amplitudes. Therefore, all three signals with different amplitudes register different discriminator times of arrival T_1, T_2 and T_3 [114]. The Time-Walk jitter is given by equation 6.3

$$\sigma_{TimeWalk} = [T]_{\text{RMS}} = \left[\frac{t_r V_{\text{th}}}{S}\right]_{\text{RMS}}. \tag{6.3}$$

The equation 6.3, shows that lower the discriminator threshold V_{th} or faster signal (shorter t_r) or increasing the input signal amplitude reduces the Time-Walk jitter.

Landau Noise σ_{Landau}: The Landau noise is the fluctuations in charge deposition by ionizing particles, causing variations in signal amplitude and shape, for laser system, as the injecting photon has very lower energy than MIP, this part is negligible.

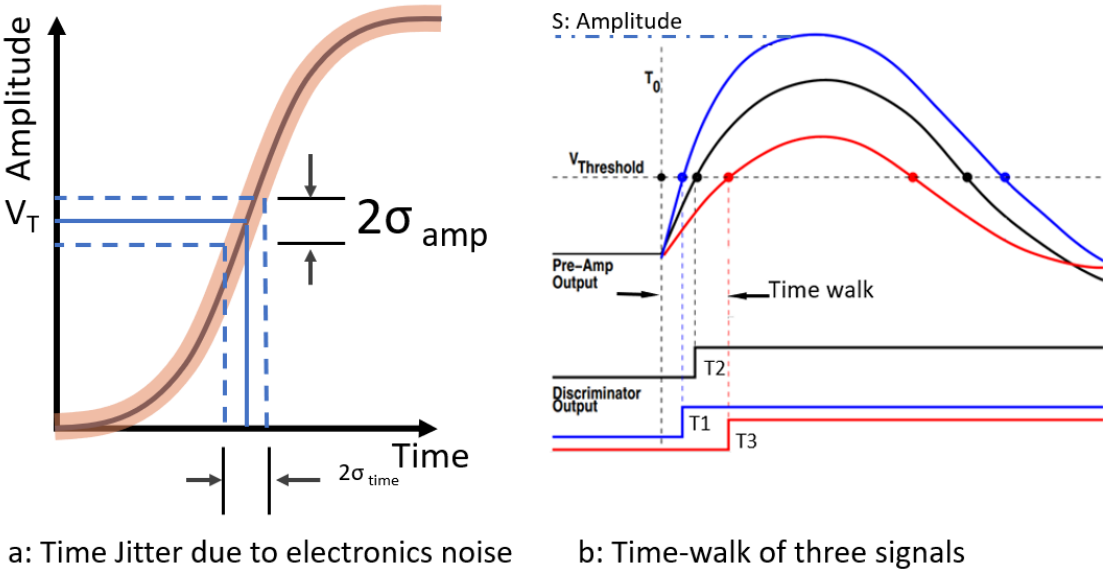


Figure 6.17: Jitter sources: (a): Electronics noise in signal amplitude, crossing a discriminator threshold, transform into time jitter, (b): Time-Walk effect: Effect of signal amplitude on discriminator output.The signals with different amplitude crossing the discriminator threshold at different times. The difference between the earliest and the latest discriminator output is known as Time-Walk.

TDC Binning σ_{TDC}: This represents the quantization error from Time-to-Digital Converters (TDC) and is given by $TDC - LSB/\sqrt{12}$, so could be ignore for TDC with LSB of 25 ps.

6.6.2 Expected timing performance of silicon Hex-Modules

The first timing performance specification is provided in the HGCAL TDR, Section 10.4 [6]. It is based on a simulation study performed using unconverted photons and non-interacting K_L^0 to assess the intrinsic timing capability of the detector. The time resolution is expressed in a parametric form as:

$$\sigma_t = \frac{A}{S/N} \oplus \sigma_{\text{floor}}, \tag{6.4}$$

where S/N is the signal-to-noise ratio, σ_{floor} is a fixed resolution floor, and $\oplus$ denotes the quadratic sum. The coefficient A captures the contribution from electronic noise, sensor response time, and clock distribution jitter. Based on the TDR specifications, $A \approx 5$ ns, while σ_{floor} (also know as Constant term) $\approx$ 20 ps at high signal amplitudes.

Further measurements from dedicated ASIC characterisation studies, presented in [29], demonstrate the practical timing performance of the HGCROC front-end ASIC. As illustrated in figure 6.18, the TOA jitter reaches a minimum of 13 ps for charge injections exceeding 100 fC, with a maximum observed jitter of 125 ps at 15 fC with Noise term $A = 1.15$ ns/fC and σ_{floor} (Constant term) $\approx$ 13 ps. The time-walk effect across the dynamic range is measured to be approximately 2.5 ns.

It is important to note that these measurements were performed using test boards with a 47 pF capacitive load simulating the sensor. They exclude realistic contributions from the full detector assembly,

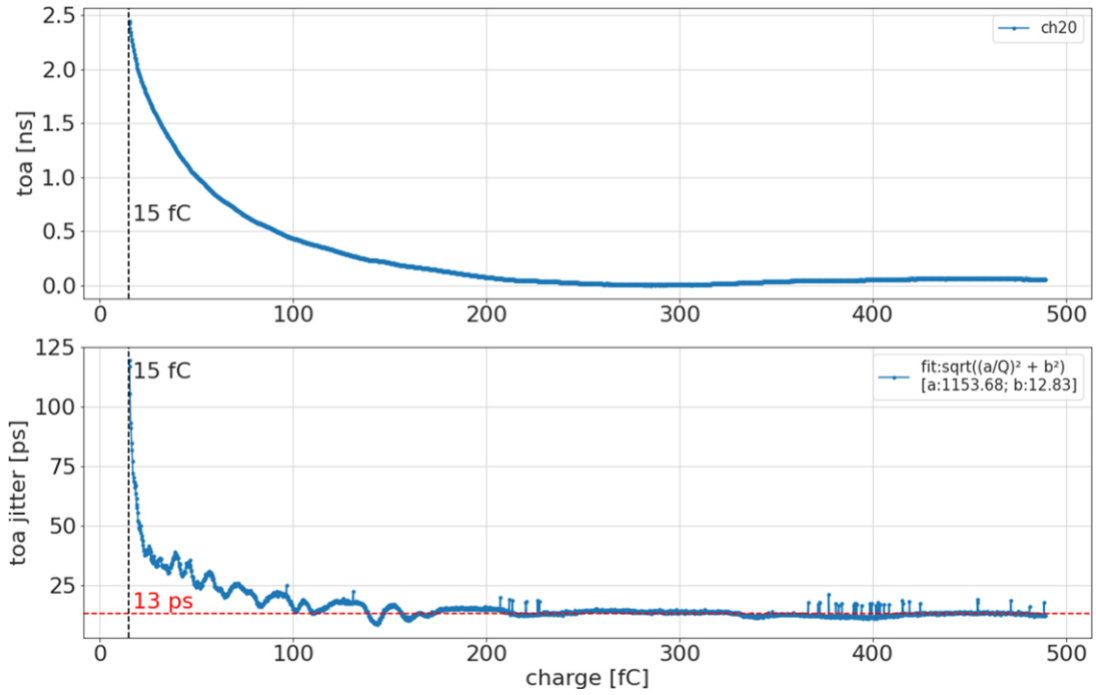


Figure 6.18: Timing performance of the HGCROC-3 ASIC measured on a test board [29]. Top: Time-walk observed up to 2.5 ns for injected charges up to 500 fC. Bottom: TOA jitter as a function of injected charge, reaching a floor of ∼13 ps.

including PCB parasitics, silicon sensor capacitance, and distribution clock jitter. Therefore, empirical validation using full module prototypes is essential.

To enable timing performance studies under realistic laboratory conditions, a dedicated laser system has been developed [115], as detailed in the subsequent subsections. The system delivers sub-100 ps FWHM infrared pulses, phase-locked to a master reference clock, and injects light through access points in the module assembly to target individual sensor pads. This configuration allows precise measurement of TOA jitter and time-walk, facilitating accurate calibration of the HGCROC response and validation of the 30 ps RMS timing resolution requirement for HL-LHC operations.

6.6.3 Laser setup for silicon Hex-Module characterization

The silicon Hex-Module is subject to very stringent performance requirements of having a timing resolution of less than 100 ps, a dynamic range spanning from 0.2 fC to 10 pC, and an electronic noise level below 2500 electrons for a sensor capacitance of 65 fF [6].

To characterise the silicon Hex-Module against these specifications, I have designed a testing setup based on a laser system operating with low jitter (the order of ps). featuring an XYZ stage with a positional accuracy of 0.5 µm and with laser intensity control via optical attenuator. The test system developed for the silicon Hex-Module characterisation uses a 1064 nm pulsed laser-diode having a very narrow 100 ps FWHM (Full Width Half Maximum) pulse, offering 7 µm beam size using a microfocal lens. The laser driver exhibits ∼ 3 ps RMS intrinsic jitter, triggered externally by an arbitrary wave form generator AWG3252, resulting in a combined system jitter of around 15 ps. The test setup block diagram

is shown in figure 6.19, while the actual view of system with its different parts is shown in figure 6.6.3.

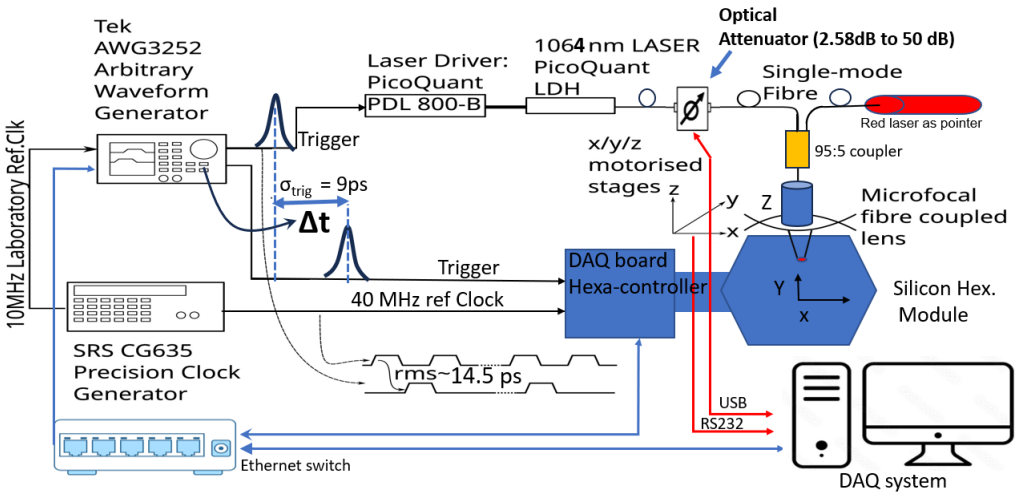


Figure 6.19: Laser setup block diagram: The clock source (SRS CG635) produces 10 MHz and 40 MHz for AWG3252 and DAQ boards. AWG3252 triggers Laser driver and Hexacontroller. Other Components include a Laser diode, optical coupler (95:5), optical attenuator, and scanning stages for the silicon Hex-Module.

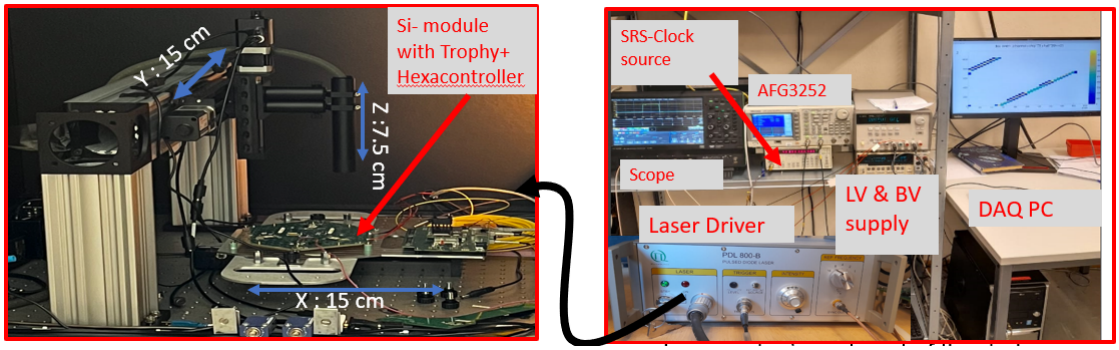


Figure 6.20: Laser setup for silicon module characterisation. Left: Si-module mounted on the XYZ scanning stage (highlighted) and interfaced with the Hexacontroller via the Trophy board. Right: Control setup including SRS CG635 clock source, AWG3252 waveform generator, laser driver, oscilloscope, low-/high-voltage supplies, and DAQ PC. The AWG3252 provides synchronous triggers to the laser driver and Hexacontroller.

The main blocks are a precise clock source SRS “CG635”, an arbitrary waveform generator “AWG3252”, a Laser driver “PicoQuant’s PDL-800B”, a Laser diode “PicoQuant LDH”, an optical attenuator, 3 x Zaber stages for x, y, z movements, and the silicon Hex-Module with Hexacontroller (DAQ board). The SRS CG635 works as a master clock source to keep all parts of the system in the same phase; it, generates two clocks: one 10 MHz laboratory reference clock going to the waveform generator AWG3252 and a 40 MHz for the Hexacontoller. The AWG3252 generates two trigger pulses with a programmable relative delay and repetition frequency of 10 kHz, phase-locked to the reference clock. One is used to trigger the Laser driver, producing an optical pulse transmitted through the single mode optical fiber passing through

the optical coupler [95:5], optical attenuator and is focused into the center of the silicon sensor cell via the microfocal lens. The second trigger is sent to the Hexacontroller to open the acquisition window. The Δt between the two triggers is tuned to a value such that the Hexacontroller acquisition window opens at the time when the laser impinges on the silicon sensor. The timing sequence of the system is shown in figure 6.21.

The intrinsic jitter between the two channels of AWG3252 is $\sigma_{\text{trig}} = \sim 9$ ps, while the jitter between the laser Trigger and the 40 MHz reference clock is ~ 14.5 ps. This is the main source of the system jitter which has an overall value of ~ 15 ps. Several attempts were made to take reliable timing measurements under this condition, but the 15 ps jitter was too large to meet the HGCAL requirement of 20 ps resolution. To improve the setup, the CG635 was replaced with a more precise clock source, the Si-5344, which reduced the laser timing jitter to about 5 ps. In addition to improving the laser system, this enhancement also led to better phase stability of the internal PLL clock of the HGCROC, reducing its jitter from 27 ps (with CG635) to 17 ps (with Si-5344).

All data shown in this chapter were recorded using this improved 5 ps setup, except for channel 138 in Table 6.11, which was measured using the older 15 ps setup. Unless specifically mentioned, the timing resolution for all results should be considered as 5 ps.

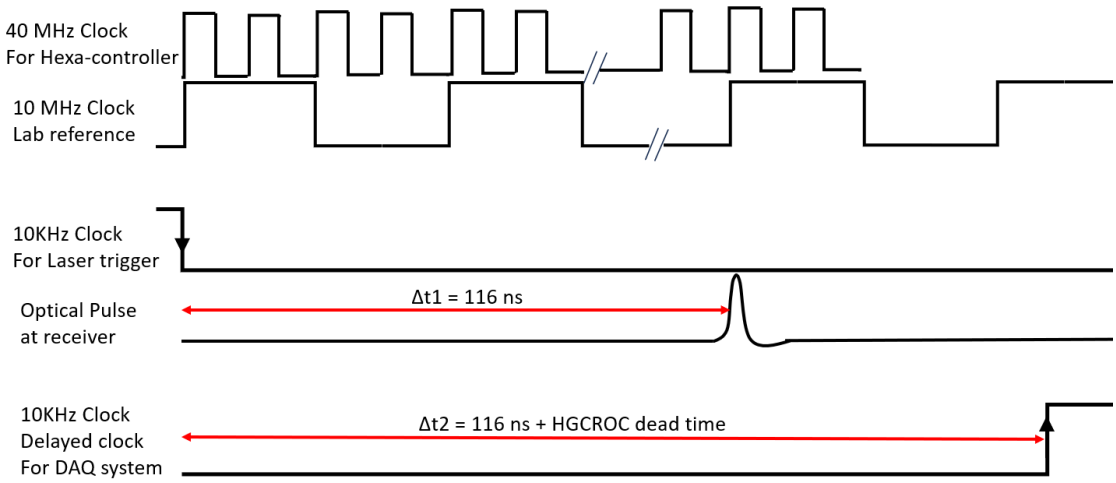


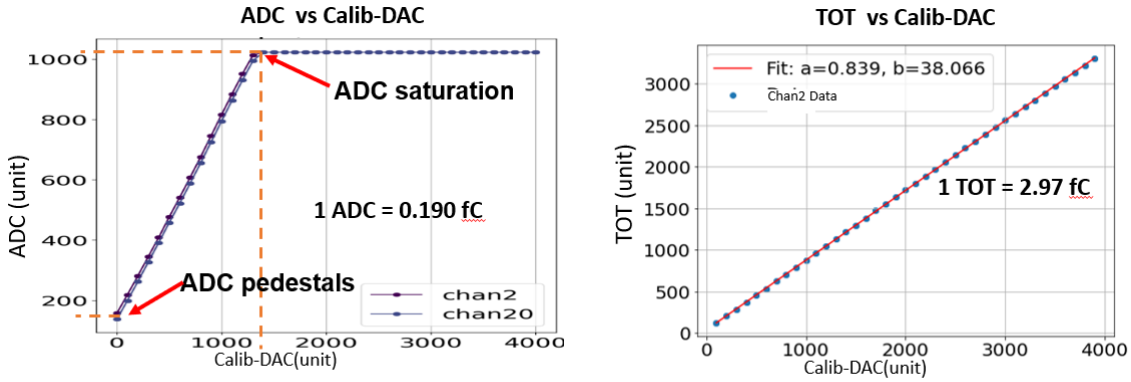
Figure 6.21: Timing diagram illustrating the synchronization between the 10 MHz lab reference clock, the 40 MHz clock for the Hexa-controller, and the 10 kHz clocks used for triggering the laser and DAQ system. Upon the falling edge of the 10 kHz clock, the laser diode emits an optical pulse with a delay of $\Delta t_1 = 116$ ns. Additionally, there is an approximate 200 ns delay within the HGCROC due to data conversion process (equivalent to 8 bunch crossings). The delayed 10 kHz clock for the DAQ system accounts for both the HGCROC internal delay and the laser delay, resulting in a total delay of $\Delta t_2 = 316$ ns.

A computer-controlled optical attenuator has been integrated to fine-tune the laser signal's amplitude, with an adjustable range from 2.58 dB to 50 dB, with a step of 0.1 dB. Additionally, the incorporation of precision xyz-motion stages facilitates the automated scanning of the silicon cells across the entirety of the silicon Hex-Module. The system utilizes two power supply modules: one low voltage (LV) supply and one Bias voltage (BV) supply. The LV supply used for low-voltage supply, provides two separate 1.5 V sources for both the analog and digital components of the silicon Hex-Module, which are further regulated through the use of customized radiation-hardened LDOs for point of load regulation of the analog and digital 1.2 V required by the HGCROCs. The bias voltage supply biases the silicon sensor.

The setup has been fully automated using Python scripts running on the DAQ PC, which connects the waveform generator to the Hexacontroller via Ethernet while communicating with the optical attenuator, and x, y, z stages through USB and RS232 protocols, respectively. This automation includes all testing procedures which involve processes like aligning the laser with the center of the silicon cell, adjusting the delay on the waveform generator, triggering the laser, changing attenuation settings, and data acquisition through the Hexacontroller. The silicon Hex-Module used for this study was biased with -270 V and all data were recorded at room temperature and in a dark environment.

6.6.4 Laser setup calibration

The steps for configuring the experimental setup for operation included the charge calibration of the HGCROC to reconstruct the charge injected by the laser pulse, along with measurements of the laser pulse jitter. Charge calibration was facilitated using the per channel internal calibration circuitry of the HGCROC. This circuitry is equipped with two selectable injection capacitors 0.5 pF and 10 pF and a 12-bit Calib-DAC, which facilitates programmable charge injection at the pre-amplifier input, ranging from 0.122 fC to 10 pC. From this injection mechanism, the ADC and TOT conversion factors were measured to be 0.190 fC / ADC-LSB, and 2.97 fC / TOT-LSB respectively. These curves are shown in figure 6.22 (a, b). Using these conversion factors, the charge injected by the laser system as a function of the attenuator setting was determined.



(a) ADC vs Calib-DAC (b) TOT vs Calib-DAC

Figure 6.22: Plots (a) and (b) display ADC and TOT calibration via internal charge injection.

A charge profile, representing the Laser injected (reconstructed) charge (Q_{inj}) as a function of the attenuation value, is produced by an automated Python script. Initially, the laser is accurately aligned with the hole in the center of the Hexaboard cell using x, y, and z stages as shown in figure 6.23 (right). Subsequently, the script varies the attenuation values from 30 dB to 3 dB and acquires both the ADC and the TOT values for all attenuation settings. These ADC and TDC codes are then transformed into charges using the factors extracted in the internal calibration process. The charge profile, presented in figure 6.23 (left), reveals that the ADC begins to detect charge at $\sim$ 29 dB and gets saturated around $\sim$ 13 dB. Beyond this point, charge measurements are carried out by the TOT, covering a range of up to 2400 fC, which corresponds to $\sim$700 MIPS.

For the Laser pulse timing measurements, the jitter was measured between the input trigger to the laser driver and the laser output optical pulse read by Agilent lightwave multi-meter “8163B”, as optical receiver and Tektronix MSO6, 6 GHz, 25,GHz/s Osciliscope. The RMS value of jitter is 15 ps, if AWG3252 used as Laser Trigger source. For more precise operation, we operated laser with silicon lab

precise clock source “Si-5344” and observed laser jitter of 5 ps (RMS).

It is notable that the profile exhibits a broad range of injected charges, going up to 700 MIPs, and offers a minimum step size of 0.1 dB. Furthermore, the system demonstrates a time jitter of ∼15 ps (rms) (could be improved to ∼5 ps (rms)), ensuring a clean and controlled environment for the characterization of the silicon Hex-Module.

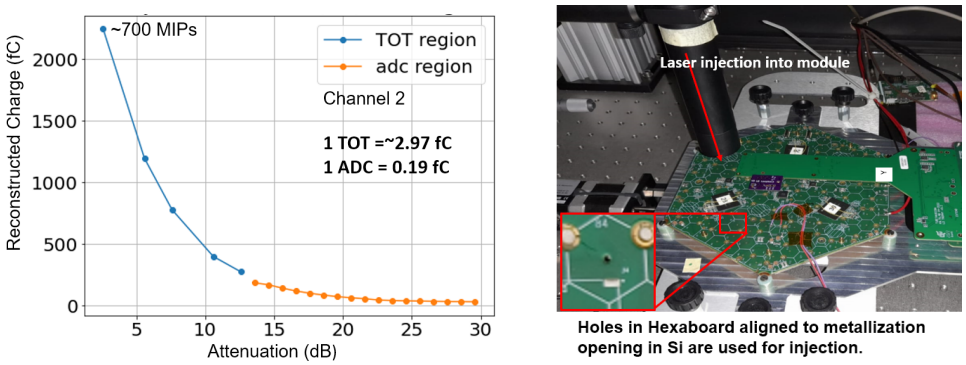


Figure 6.23: Left: Charge profile showing reconstructed charge Q_{inj} (fC) as a function of optical attenuation (dB) for channel 2 of the silicon Hex-Module, indicating the ADC and TOT measurement regions. Right: Photograph of the Hex-Module mounted on the XYZ scanning stage for laser injection.

6.6.5 Time synchronisation

The laser was shined in the silicon Hex-Module cell with a fixed attenuation of 13.58 dB and a trigger time phase-locked to the reference clock. This made sure that the pre-amplifier response was in the ADC range. The HGCROC has a per-channel DLL (Delay Locked Loop) allowing the ADC sampling phase to be swept in 16 steps through the 40 MHz reference clock. By sweeping this setting in combination with the bunch crossing, in which the trigger signal was generated, the full pre-amplifier response was sampled across four bunch crossings. From plot in figure 6.24, the optimal ADC sampling phase and right bunch crossing for the trigger were selected.

6.6.6 Timing measurements for silicon Hex-Module Channels

The laser test setup with above mentioned characteristics, offers numerous applications essential to assess the operational integrity of the HGCAL silicon Hex-Module. It facilitates the comprehensive evaluation of uniformity and responsiveness of silicon pads across all silicon Hex-Modules. It could serve in the cross-validation of calibration processes for the ADC and TDCs (TOA and TOT). The principal application of this setup in this thesis is the timing characterization aimed at extracting properties such as Time-Walk and time resolution of silicon Hex-Module channels, which constitute the central focus of this section.

This section presents a detailed timing analysis performed on silicon modules using the laser system. The study focuses on three specific channels: chan_id 35 (chip0, channel 35), 138 (chip1, channel 57), and 158 (chip2, channel 2) of the LD-Silicon module. These channels were selected based on two primary considerations. First, due to mechanical constraints of the readout setup, many laser access holes were obstructed by the Trophy board, limiting the number of usable injection points. Second, the selection ensures coverage across all three chips, allowing channel-level timing characterization to be evaluated across the entire front-end chain. The resulting measurements are used to extract key timing parameters, which are critical for the optimal performance of the HGCAL.

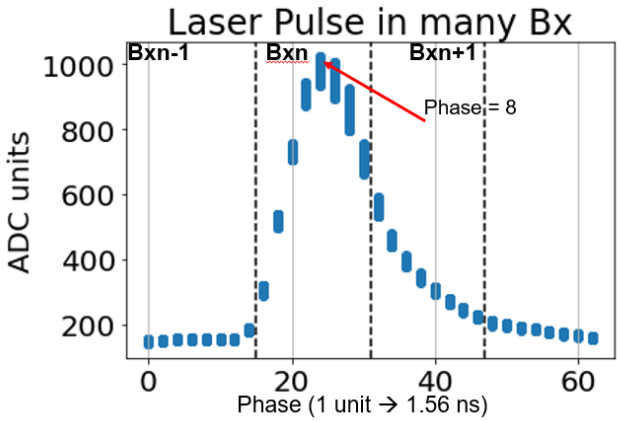


Figure 6.24: Finding the right Bx: demonstrates ADC variation across four bunch crossings, where an externally laser injected pulse is reconstructed to find best phase and right bunch crossing.

Experimental setup and methodology: This study used a V3-LD-Hexaboard equipped with a 300 um thick n-on-p LD silicon sensor, which has 192 cells read by 3 HGCROC-3A (SU04 BGA package) chips. The 3 in name corresponds to 3rd version, and A is further shows first of the sub versioning (at the time of this writing HGCROC-3C is near to submission). The SU04 shows the grounding scheme inside the BGA package, which corresponds the Analog and digital returns are kept separate at the BGA package level and mix together at Hexaboard level. A global variable Chan_id range from 0 to 233 is used to present the channels of 3 HGCROCs, where each chip has 78 channels, that further splits into two halves each of 39 channels. The module was biased at -270 V to operate the n-on-p LD-Sensor in fully depleted region. The laser was precisely aligned into the center of the hexagonal cells of the module, shone laser light and read the output. Table 6.9 summarizes the laser setup and silicon Hex-Module parameters.

Three channels with chan_id 35, 138 and 158 were subjected to timing study. Their details characteristics are listed in table 6.10.

A programmable laser attenuation scan was executed using a Python-controlled routine, covering a range from 3 dB (representing high optical intensity) to 30 dB (low intensity). At each attenuation point, 10,000 events were recorded to collect the necessary observables for timing characterization, including the ADC, TOT, and TOA measurements. The injected charge Q_{inj} was reconstructed from the ADC and TOT values, following the methodology described previously.

For the evaluation of timing performance, TOA distributions were analyzed as a function of the reconstructed charge Q_{inj}. The mean TOA values across the charge range were used to quantify the **Time-Walk** effect, defined as the charge-dependent shift in signal arrival time. In parallel, the standard deviation (σ_t) of the TOA distribution at each charge point was extracted to determine the **timing resolution**, which reflects the intrinsic time jitter of the readout system.

To generalize these results across different readout channels, the Time-Walk and timing resolution were also expressed as functions of the signal-to-noise ratio (S/N), where S/N is defined as the ratio of Q_{inj} to the electronic noise level of the respective channel. This normalization facilitates channel-independent performance comparisons and provides a clearer representation of the timing behavior relative to electronic noise.

It is important to note that the observed TOA jitter (σ_t) is primarily governed by the first two terms of Eq. 6.1: the electronic noise-induced jitter (equation 6.2) and the Time-Walk contribution (equation 6.3). However, a direct correlation between the measured timing resolution and these underlying physical

Table 6.9: Laser setup and the Silicon Hexmodule operational parameters.

Parameter	**Value**
Laser System	Laser Jitter = ∼15 ps when triggered with AWG AF3252 Laser Jitter = ∼5 ps when triggered with Si-5344 clock source Attenuation Scan: 3 dB to 30 dB
Silicon Module	**V3-LD-Hex-Module**: equipped with 300 um thick, 8 inches 192 Cells LD sensor using 3× HGCROC-3A (SU04-package) **Channel numbering**: Each HGCROC has 78 channels, further split into two halves of 39 channels. chan_id is global numbering scheme across LD Module. where $chan\_id = channel + chip * 78 + half * 39$ **Bias Voltage**:-270 V to deplete the n-on-p sensor **HGCROC PLL measured at 160** MHz **clcok that run the TDCs**: PLL jitter = ∼ 27 ps when CG635 clock source use as master clock PLL jitter = ∼ 17 ps when Si-5344 clock source used as master clock

Table 6.10: HGCROC parameters used for the timing study with laser injection. The pedestals, noise, ADC and TOT conversion factors to fC, as well as TOA and TOT thresholds are listed for channels 35, 138, and 158.

Parameter	**Channel 35**	**Channel 138**	**Channel 158**
Pedestal (ADC)	156	155	153
Noise (ADC)	1.8	2.3	2.1
Conversion (ADC/fC)	0.197	0.193	0.213
TOT Conversion (slope, intercept)	0.850, 29.16	0.850, 24.22	0.850, 25.28
TOA threshold (Calib_DAC, fC)	106 (12.9 fC)	126 (15.3 fC)	126 (15.3 fC)
TOT threshold (Calib_DAC)	470	478	482

parameters—such as the pulse rise time (t_r) or the signal amplitude at the discriminator—could not be established, as these quantities were neither accessible nor measurable within the current experimental setup.

To overcome this limitation, a parametric fitting approach was adopted to describe the measured timing behavior empirically. The following functional forms were used to model the timing resolution and Time-Walk as functions of the injected charge and signal-to-noise ratio:

$$\sigma_t = \sqrt{\left(\frac{A}{Q_{\text{inj}}}\right)^2 + C^2}. \tag{6.5}$$

$$\sigma_t = \sqrt{\left(\frac{A}{S/N}\right)^2 + C^2}. \tag{6.6}$$

$$TW = \left(\frac{A}{S/N}\right) + C. \tag{6.7}$$

This fitting procedure yields two key parameters: A, representing the noise term that dominates at low Q_{inj}; and C, the constant term, which manifests as a plateau at high charge values and is independent of the injected charge. These parameters provide insight into the main factors limiting the timing resolution of the silicon Hex-Module. Moreover, they allow for a qualitative comparison with performance expectations documented in the HGCAL TDR [6], as well as with values extracted by ASIC designers, as illustrated in figure 6.18.

Figures 6.25, 6.26 and 6.27 depict the TOA jitter and the Time-Walk effect in response to the injected charge (Q_{inj}) or $\frac{S}{N}$ for channel 35, with TOA-threshold = 115 Calib-DAC ($\sim$ 14 fC) respectively. Table 6.11 summarizes the fit results obtained for Channel 35 under two different TOA reference voltage settings (V_{ref}), as well as for Channels 138 and 158. Notably, the constant term C extracted for Channel 138 includes the contribution from laser jitter, which was estimated to be approximately 15 ps. In contrast, the fits for Channels 35 and 158 were performed under improved timing conditions, where the laser jitter was limited to about 5 ps. Indeed, for channels 35 and 158, a more precise clock source, the Sci-5344, was used.

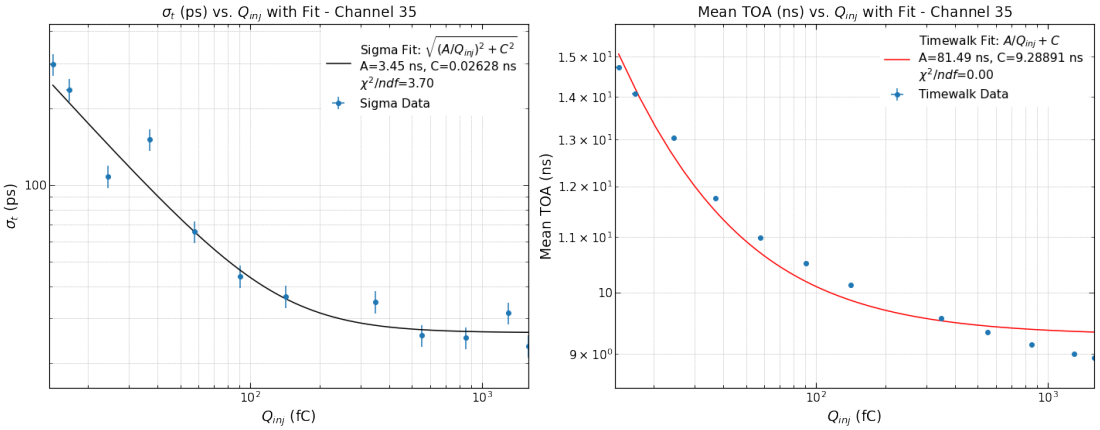


Figure 6.25: Timing analysis of Channel 35 with a TOA-V_{ref} of 14 fC. The left plot illustrates the TOA jitter (σ_t) as a function of the injected charge Q_{inj}, overlaid with the corresponding parametric fit. The right plot shows the Time-Walk behavior, depicting the mean TOA as a function of Q_{inj}, fitted using the analytical model. Each data point corresponds to the statistical analysis of 10,000 events.

6.6.7 Results and discussion

The timing analysis for three channels, presented in figures 6.25, 6.26 and 6.27 and table 6.11, provides important insights into the behavior of TOA jitter (σ_t) and Time-Walk across different channels and conditions.

The left plots of figures 6.25 and 6.27 illustrate the TOA jitter (σ_t) dependence on the injected charge (Q_{inj}) and signal-to-noise ratio (S/N), respectively. Figure 6.26 shows the zoomed view of figure 6.25 in linear scale and shows that the TOA triggered around $\sim$ 14 fC with very large error bar in time ($\pm$25 ps) for first few samples, and then data sets get stabilized. At lower charge, near the threshold ($\sim$ 14 fC), the signal is very weak and is just above the electronic noise level, and crosses the TOA threshold with very

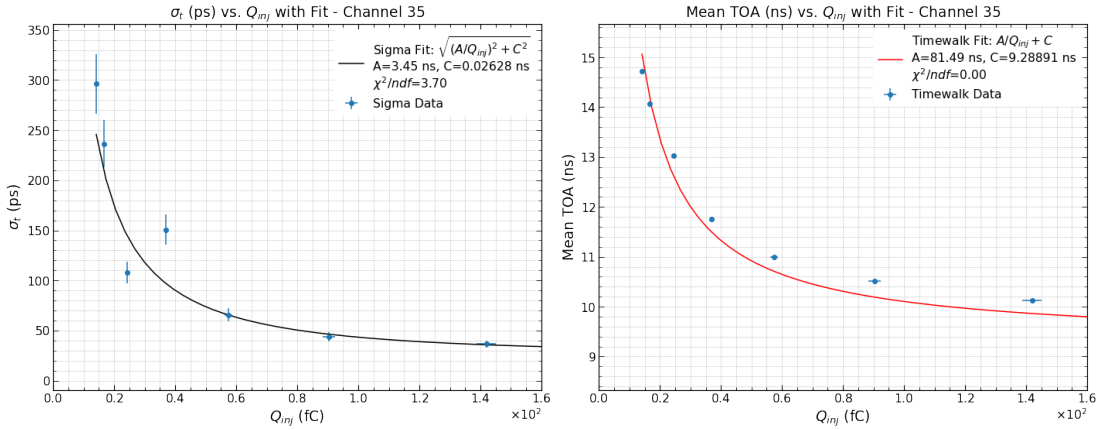


Figure 6.26: zoomed view of figure 6.25 with linear scale, for $Q_{inj} < 160\,\text{fC}$ for chan_id 35.

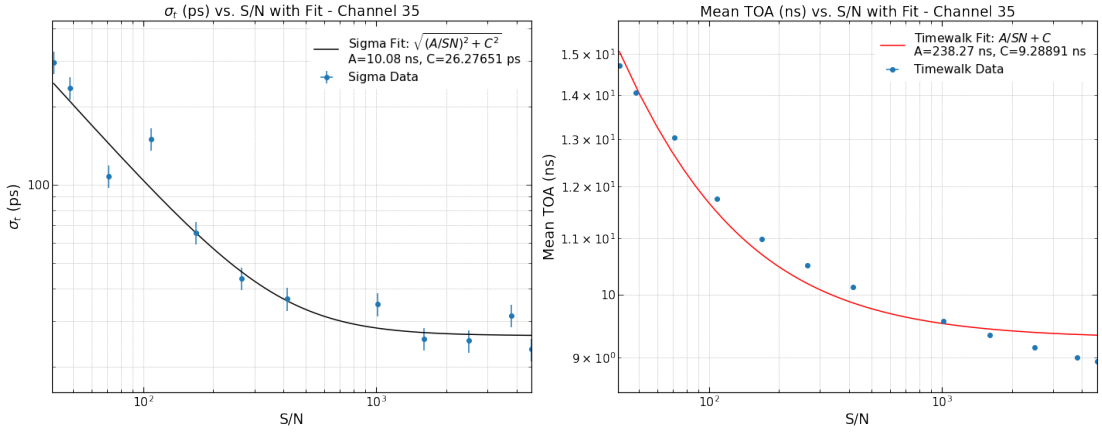


Figure 6.27: Timing analysis of chan_id 35: (left) TOA jitter (σ_t) vs Q_{inj}, (right) Time-Walk: TOA mean vs S/N.

large slew rate and rise time t_r, therefore produce large amount of time jitter σ_t which has contributions from both electronics noise source (σ_j) and Time-Walk (σ_{TW}). With higher amplitude charges injected, the slew rate and rise t_r decrease (signal crosses threshold faster) and the time jitter reduces. This jitter decrease with an increasing signal amplitude is consistent with Eq. 6.2.A higher S/N ratio improves the timing resolution, which is reflected in the observed reduction in jitter as Q_{inj} increases.

The Time-Walk behavior is illustrated in the right-hand plots of Figures 6.25 and 6.27, which display the variation of the mean TOA as a function of the injected charge Q_{inj} and the signal-to-noise ratio S/N, respectively. A total Time-Walk span of approximately 6 ns is observed, corresponding to the difference between the maximum and minimum mean TOA values. The majority of this effect originates from samples with $Q_{\text{inj}} < 25\,\text{fC}$, where the signal amplitude is low and the slew rate at the discriminator threshold is reduced. This trend is consistent with the analytical expression given in Eq. 6.3, which relates Time-Walk jitter to the inverse of the signal slope and amplitude at threshold. It emphasizes that Time-Walk can be reduced by lowering the discriminator threshold (V_{th}) or by increasing the signal rise time (t_r), both of which enable earlier and more uniform threshold crossings.

Chan_id	Data_run	TOA Vref (Calib Dac)	σ_t (ps) A($\frac{ns}{fC}$, $\frac{ns}{S/N}$), C(ps)		Time-Walk (fC) TW(ns), A($\frac{ns}{fC}$), C(ns)		
35	**48**	**115**	3.45, 10.08	26.27	6	81.4	9.28
35	49	95	3.31, 9.29	34.33	6	66.42	8.99
138	21	126	5.35, 11.89	35.09, 31.4 (cor)	6	208.6	10.75
158	31	126	4.42, 10.36	33.55	6	141.3	14.85

Table 6.11: Timing performance summary for 3 channels (Chan_ids 35, 138, and 158), including ToA Vref (threshold), timing resolution σ_t, and Time-Walk characteristics. The table presents key parameters Noise term **A** and constant term **C** for σ_t, and Time-Walk. The constant term **C** of Chan_id=138 is corrected for the Laser Jitter of ∼15 ps. For remaining channels, the laser jitter was ∼5 ps, so no correction was needed due to the negligible effect.

- **Channel 35:** Timing results for two thresholds levels TOA Vref 115 Calib-DAC (14 fC) and 95 Calib-DAC (∼ 11 fC) presented. The first row with bold text corresponding to above mentioned σ_t and Time-Walk figures, have the A is 3.45 $\frac{ns}{fC}$ or 10.08 $\frac{ns}{S/N}$, while the C is ∼ 26.27ps, which represent the Time-resolution for the channel for charge $Q_{inj} > 350$ fC. For the lower threshold setting, the extracted noise term A was found to be 3.31 ns fC^{-1} or equivalently 9.29 ns per unit S/N, while the constant term C was approximately 34 ps. These values suggest that the TOA-$V_{\text{ref}} = 115$ setting represents the optimal threshold, as it was determined by an automated minimum TOA-finding script. Further reduction of the threshold would likely make the system more susceptible to noise-induced triggers, thereby degrading performance—particularly by increasing the constant term C.

  The overall trend is consistent with expectations: a clear reduction in timing jitter σ_t with increasing Q_{inj}, indicating improved time resolution as the signal-to-noise ratio increases. In both threshold settings, the observed Time-Walk spanned approximately 6 ns. According to Eq. 6.3, a lower TOA threshold (V_{th}) should lead to reduced jitter. However, in the case of TOA-$V_{\text{ref}} = 95$, this improvement could not be realized, as the threshold level likely fell within the noise band, leading to increased timing fluctuations.

- **Channel 138:** This channel has threshold of 126 Calib DAC (∼15.3 fC) and includes a correction for the constant term C for the laser jitter of 15 ps. The Noise trem A = 5.35 $\frac{ns}{fC}$ and the C = 31.4 ps. The Time-Walk is same as channel 35.

- **Channel 158:** Its has same threshold to Channel 138, with A = 4.42 $\frac{ns}{fC}$ and the C = 33.5 ps.

The results align with expectations, showing increased TOA jitter near the threshold, which stabilizes with improved timing resolution at higher injected charges. Variations in TOA thresholds, gain settings, and minimum timing resolution were observed across channels. The ADC-to-TOA transition is not smooth, observd significant error bars, and need improved tunning of parameters responsilble for shifting from ADC to TOT. Fine-tuning these parameters is critical to achieving lower jitter and precise Time-Walk correction, ensuring optimal timing performance tailored for the HGCAL detector.

6.7 Temperature dependance of the timing resolution

This section examines the influence of temperature on the timing resolution of the silicon Hex-Module. The study explores how changes in operating temperature affect the module's timing performance, focusing on measurements taken under well-controlled conditions.

6.7.1 Experimental setup and data taking

To investigate the temperature dependency of the timing resolution for the V3-LD-Hex Module, the laser setup, as described in Section 6.6.3, was relocated to a facility at CERN dedicated to silicon sensor characterisation. The upgraded setup, shown in Figure 6.28, is largely similar to the original configuration presented in figure 6.19, with two key enhancements: the integration of a Si-5344 evaluation board providing a low-jitter clock source, and the enclosure of the silicon module within a probe station to ensure a controlled temperature environment.

The probe station, shown in figure 6.29, featured a temperature-controlled chuck with x-z positioning capabilities and vacuum holes for securely holding the silicon Hex-Module during testing. The chuck's temperature and position were managed using a Python-based graphical user interface (GUI), ensuring precise alignment and optimal thermal contact for consistent testing conditions. Inside the chamber, the silicon module was positioned on the chuck and secured via vacuum pressure. The Hexacontroller (DAQ board) was also placed within the chamber and connected to the module using TWINAX cables to enable efficient data acquisition. The laser beam was delivered into the chamber through an optical fiber and aligned precisely with the silicon cell using the chuck's positioning system. Supporting equipment, including the laser driver, waveform generator, and external clock source, was stationed outside the chamber to minimize interference and maintain a controlled testing environment.

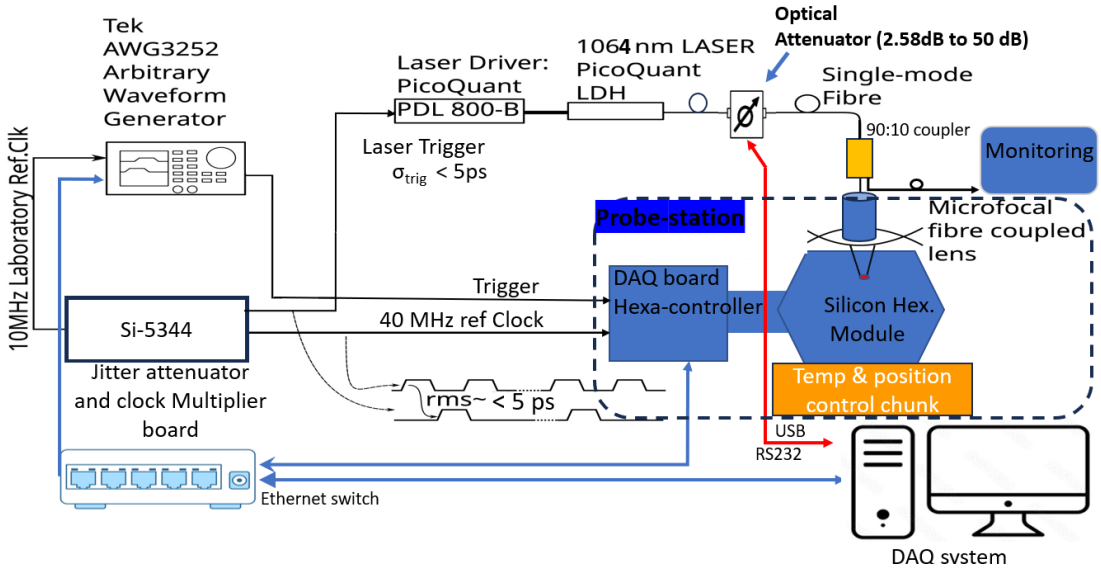
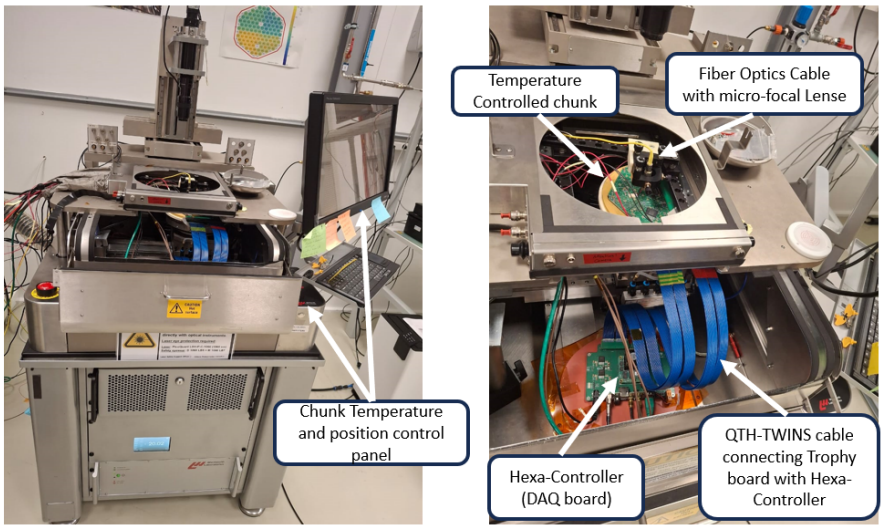


Figure 6.28: Laser setup block diagram: integrated with the probe station at the silicon characterization lab at CERN, featuring temperature control as the main component. The setup also incorporates the Si-5344 evaluation board for precise clock synchronization and jitter attenuation (5 ps RMS).

The experimental procedures for charge and time calibration are followed as described earlier in Sections 6.6.4 and 6.6.5. Data acquisition was performed using the Hexacontroller board, logging 10,000 events for each laser attenuation step. Laser attenuation was systematically varied from 21 dB to 2 dB in 0.5 dB decrements through an automated Python script. TOA jitter (σ_t) was extracted from the standard deviation of the TOA distributions obtained at each attenuation level.

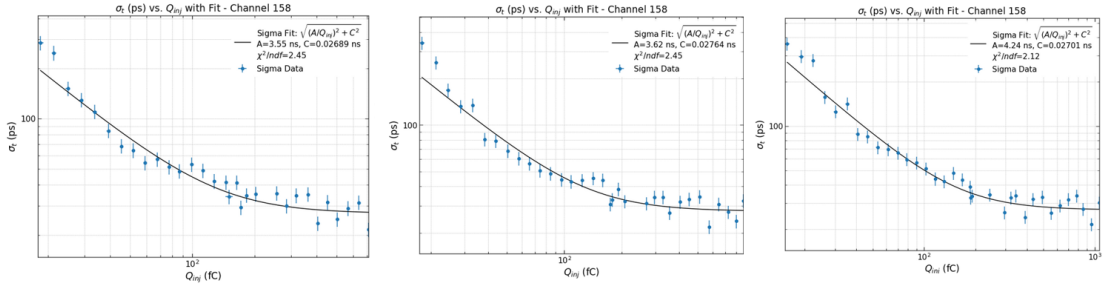


A: Probe station for HGCAL silicon sensor Lab CERN B: Probe statin with inside view

Figure 6.29: Probe-station setup for timing characterization: (A) Operational view of the probe station, (B) Close-up of the temperature-controlled chuck with vacuum holes for securely holding the silicon Hex-Module.

6.7.2 Temperature influence on timing resolution

The timing resolution of the V3-LD-Hex Module, equipped with a 300 μm *n*-on-*p* sensor, was examined across three temperatures: -20°C, 0°C, and 20°C. The TOA jitter (σ_t) was plotted against the signal-to-noise ratio (S/N), as shown in figure 6.30.



A: Laser Attenuation Scan at -20 °C B: Laser Attenuation Scan at 0 °C C: Laser Attenuation Scan at 20 °C

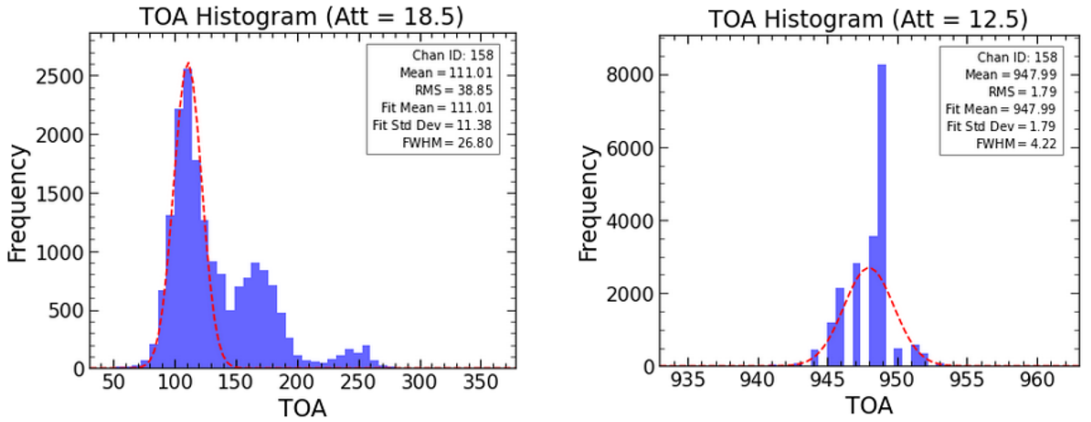
Figure 6.30: TOA jitter (σ_t) vs. injected charge (Q_{inj}) for channel 158 at $-20\,^{\circ}$C, $0\,^{\circ}$C, and $20\,^{\circ}$C. Curves are fitted with $\sqrt{(A/Q_{\text{inj}})^2 + C^2}$; parameter A increases with temperature, indicating higher noise. Maximum Q_{inj} range shifts with temperature: 713 fC ($-20\,^{\circ}$C), 868 fC ($0\,^{\circ}$C), and 1058 fC ($20\,^{\circ}$C).

The TOA jitter plots in figure 6.30 exhibit consistent behavior across the three studied temperatures. The extracted noise terms A from the fits are 3.55 $\frac{\text{ns}}{\text{fC}}$ (corresponding to $9.27\,\text{fC}/(S/N)$), 3.62 $\frac{\text{ns}}{\text{fC}}$ ($9.44\,\text{fC}/(S/N)$), and 4.24 $\frac{\text{ns}}{\text{fC}}$ ($11.06\,\text{fC}/(S/N)$) for $-20\,^{\circ}$C, $0\,^{\circ}$C, and $20\,^{\circ}$C, respectively, while the constant term C remains stable at approximately 27 ps. At low Q_{inj}, the jitter increases slightly, primarily

due to the presence of noise-triggered outliers. This is supported by the TOA histogram analysis in figure 6.31, which compares TOA distributions at two laser attenuation settings: 18.5 (∼22.34 fC) and 12.5 (∼16.18 fC). At lower Q_{inj}, the histogram shows significant broadening with an RMS of 38.85 TOA codes compared to a much narrower Gaussian fit width (σ = 11.38 TOA code), indicating that non-Gaussian tails arise from noise-induced triggers. Conversely, at higher Q_{inj}, both RMS and fit σ converge (1.79 TOA code), suggesting clean signal response with minimal noise contamination.

For instance, at Q_{inj} ∼22 fC, the TOA jitter values are ∼280 ps, ∼270 ps, and ∼260 ps at 20°C, 0°C, and −20°C, respectively. These variations fall within the expected stochastic behavior of charge generation and timing resolution in silicon sensors.

An additional observation is the temperature-dependent extension of the dynamic charge injection range. The maximum Q_{inj} observed increases from ∼713 fC at −20°C to ∼868 fC at 0°C, and further to ∼1058 fC at 20°C. This trend may reflect temperature effects on IR laser absorption or charge collection efficiency in the silicon, and warrants dedicated investigation.



(a) TOA histogram at Att = 18.5 (~ 22.34 fC)

(b) TOA histogram at Att = 12.5 (~116.18 fC)

Figure 6.31: TOA histograms for channel 158 at two laser attenuation settings: (a) Att = 18.5 (∼22.34 fC) and (b) Att = 12.5 (∼16.18 fC). At lower injected charge, the TOA distribution broadens significantly. A large difference between the RMS and the Gaussian fit σ (38.85 TOA codes vs. 11.38 TOA codes), where 1 TOA code corresponds to 24.5 ps, indicates the presence of non-Gaussian outliers likely caused by noise triggers. At higher injected charge, both metrics converge, indicating reduced timing noise.

In conclusion, temperature exhibits negligible influence on the timing resolution of the silicon HexModule. The module's robust timing performance across varying thermal conditions highlights its reliability and suitability for precise timing applications in the HGCAL system.

6.7.3 Study of injected charge range differences

During the study of the temperature dependence of the laser setup at the probe station, we observed an unexpected yet systematic behavior: the injected charge range extended consistently with increasing temperature. As shown in figure 6.30, the measured Q_{inj} range increased from 713 fC at −20°C, to 868 fC at 0°C, and to 1058 fC at +20°C.

To understand the observed differences in the S/N range across temperatures, the Q_{inj} versus attenuation data and the HGCROC gain comparison were analyzed, as shown in figure 6.32. The left plot

highlights that for the same laser attenuation, the charge collected varies significantly across temperatures (20°C, 0°C, and -20°C). These differences prompted an investigation into potential factors affecting charge collection.

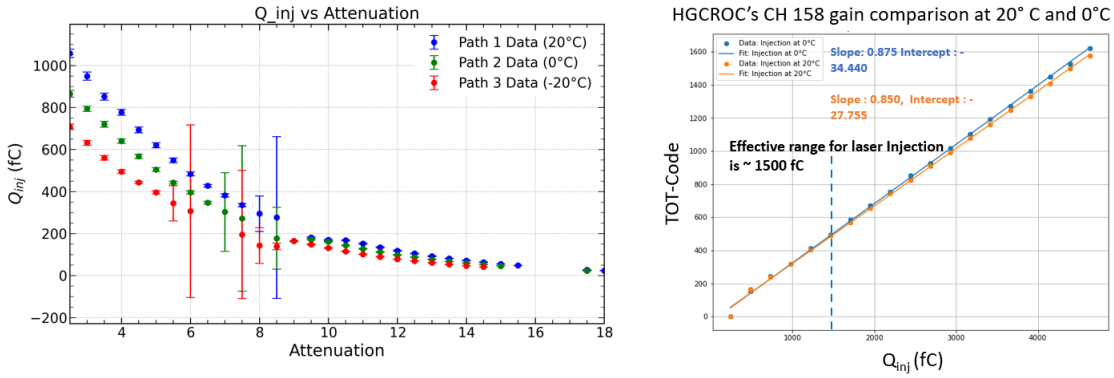


Figure 6.32: (Left) Injected charge (Q_{inj}) vs laser attenuation for channel 158 at 20°C, 0°C, and -20°C. (Right) TOT-code vs Q_{inj} comparison at 20°C and 0°C.

Potential factors influencing charge readout

Laser holder stability with temperature One hypothesis was that the laser holder might expand or contract with temperature variations, potentially causing the laser beam to go out of focus. However, this possibility is excluded due to the sophisticated alignment procedure employed at each temperature, ensuring precise laser focus on the silicon Hex-Module's cells.

HGCROC gain variability To investigate whether HGCROC gain variability could explain the observed charge differences, a comparison of TOT-code versus Q_{inj} at different temperatures was conducted and shown in right plot of the figure 6.32. While a slight variation in slope was observed with temperature, it was insufficient to account for the significant differences in charge collection seen in the left plot, especially within the effective charge injection range (<1500 fC). Therefore, this factor is also ruled out.

Charge collection efficiency The charge collection efficiency in silicon sensors is inherently temperature-dependent, governed primarily by variations in carrier mobility and recombination dynamics. At lower temperatures, reduced thermal agitation lowers recombination rates, which theoretically enhances charge collection. Consequently, one would expect a higher measured charge at lower temperatures for a given laser attenuation. However, as shown in figure 6.32 (left), a net decrease in Q_{inj} is observed at lower temperatures. This counterintuitive trend suggests that some other temperature-dependent mechanisms may dominate and offset the expected gain in collection efficiency.

IR Laser absorption coefficient Another critical factor is the temperature-dependent absorption coefficient of silicon. For a 1064 nm infrared laser, the absorption coefficient of silicon is known to decrease with falling temperature, as documented in [116] (figure 6). This reduction in absorption limits the amount of laser energy deposited within the sensor, thereby reducing the number of generated charge carriers. A corresponding trend in decreased charge generation with decreasing temperature is also observed in [117] (slide 18). The combined effect of temperature-sensitive charge collection efficiency and the IR laser absorption coefficient likely to be the primary reason for the differences in Q_{inj} at the same

attenuation across temperatures. Further exploration of these effects, including detailed modeling, is recommended to fully characterize this behavior. However, for the scope of this study, it is concluded that these variations do not significantly impact the timing resolution.

6.8 Comparison with TDR and ASIC designer's Reference

The target specifications for the timing performance of HGCAL silicon modules are presented in Section 6.6.2. According to the TDR [6], the expected benchmark parameters are a noise coefficient of $A = 5\,\text{ns}/(S/N)$ and a constant resolution floor of $C = 20\,\text{ps}$. Additionally, ASIC characterization studies [29], conducted under idealized bench-top conditions, report improved performance with $A \approx 1.15\,\text{ns/fC}$ and $C \approx 13\,\text{ps}$.

In our experimental investigations using fully assembled silicon Hex-Modules, the extracted noise coefficients A were 10.08, 11.89, and 10.36 ns/(S/N) for channels 35, 138, and 158, respectively. The corresponding constant terms C, derived at high injected charge levels, were found to be $\sim$26 ps, $\sim$31 ps, and $\sim$33 ps—substantially higher than both the TDR and ASIC reference benchmarks.

Furthermore, the lowest extracted value of the noise coefficient in our dataset was $3.45\,\text{ns/fC}$, remains notably above the value reported by the ASIC designers. These deviations illustrate the difficulty of reproducing idealized timing metrics in a full module environment where multiple noise sources and system-level effects are present.

To explore possible avenues for performance improvement, we investigated the influence of ambient temperature, with the hypothesis that lower operational temperatures might yield enhanced timing resolution. However, measurements revealed no significant reduction in either the A or C terms under cooler conditions.

The subsequent subsections provide a detailed analysis of the potential sources contributing to these deviations.

Sources of timing performance degradation

1. Broad and Non-Gaussian TOA distributions at low injected charge

A key factor contributing to the elevated noise coefficient A at low injected charge is the emergence of broad, non-Gaussian TOA distributions. As illustrated in Figure 6.31 (left), at an attenuation of 18.5 dB (corresponding to $\sim$22.34 fC), the TOA histogram displays a pronounced tail and significant deviation from Gaussian behavior. The measured RMS is 38.85 TOA codes, whereas the standard deviation from a Gaussian fit is only 11.38 TOA codes. This large mismatch points to the presence of noise-triggered outliers, which distort the distribution and inflate the extracted timing jitter.

These findings emphasize the need for precise TDC calibration and systematic TOA-threshold optimization. Identifying and mitigating the underlying sources of random TDC activations—such as electronic noise or unstable thresholds—will be critical to improving timing resolution, particularly in the low signal regime.

2. System-level jitter and clock path contributions

The minimum achievable time resolution C is influenced by several sources of system jitter. The primary 40 MHz reference clock, generated by either the SRS CG635 or Si5344, introduces a baseline jitter of 3–5 ps. This clock is internally multiplied within the Hexacontroller to 320 MHz and routed to the HGCROC, where its measured jitter increases to approximately 15 ps due to signal integrity losses and impedance discontinuities.

Inside the HGCROC, this 320 MHz input is used to recover the 40 MHz base clock, which is then passed to an internal PLL to generate higher-frequency clocks (160 MHz, 640 MHz, 1.28 GHz) required for TDC and other internal operations. Jitter accumulated in this distribution chain propagates through the PLL stages, resulting in effective timing noise in the range of 17–27 ps. This compounded jitter directly contributes to the observed C values and limits the achievable timing floor.

Similarly, the Power Distribution Network (PDN) design plays a significant role. A high-impedance PDN may fail to suppress voltage transients and high-frequency disturbances, introducing additional electronic noise into the analog front-end. Environmental variables, such as temperature drifts, supply ripple, and board-level EMI, further compound these effects. The imperfections in devices such as waveform generators, laser drivers, or optical components (e.g., aging of diodes or instability in attenuators) can also introduce jitter that is inseparable from the detector response. Continuous calibration and environmental control are thus essential to suppress these parasitic effects.

3. Real system Behavior vs. simulation and test bench conditions

Unlike controlled ASIC test boards or idealized simulations used in the TDR, the full Hex-Module environment introduces a host of real-world uncertainties. These include PCB parasitics, complex grounding schemes, sensor and bond-pad variability, and local temperature gradients. The measurement setup replicates actual operating conditions more closely, thereby uncovering effects not present in ideal models. These differences naturally lead to elevated values of A and C, particularly at higher signal levels where analog path nonlinearities and noise floor saturation become prominent.

In conclusion, while the timing performance achieved in our module tests remains close to the target, discrepancies with respect to the TDR and ASIC designer benchmarks persist. These are attributable to TDC calibration irregularities, system-level clock and PDN limitations, and unavoidable environmental effects inherent to real detector systems. Further improvements will require optimization of clock paths, reduction of front-end noise, and possibly implementation of differential laser injection schemes to eliminate common-mode noise.

6.9 Physics impact of timing resolution parameters and TOA threshold

The precise measurement of TOA in the HGCAL is critical for the accurate reconstruction of neutral hadrons (K_L^0) and photons (γ), which lack direct tracking from the tracker (see section 1.5.2) and timing information from the Endcap Timing Layer (ETL). Within the reconstructed shower composition, neutral hadrons contribute to approximately 15%, while photons account for around 30% as can be seen in figure 6.33 adopted from ref. [14].

Unlike charged particles, which benefit from tracking information in the inner tracker and timing tagging from ETL, the neutral hadrons and photons rely solely on the calorimeter system (ECAL and HCAL) for both spatial and timing measurements, making TOA resolution a fundamental parameter for their reconstruction. This dependence on HGCAL underscores the importance of precise timing information for key physics processes, including event reconstruction, pileup mitigation, and missing transverse energy (MET) calculations.

This section presents a detailed analysis of the physics impact of TOA thresholds and timing resolution parameters (Noise term 'A' and constant term 'C') based on a dedicated simulation study done by CMS Detector Performance Group (DPG). The study evaluates the sensitivity of neutral hadrons and photons to variations in TOA precision and its implications for calorimeter-based event reconstruction at the HL-LHC.

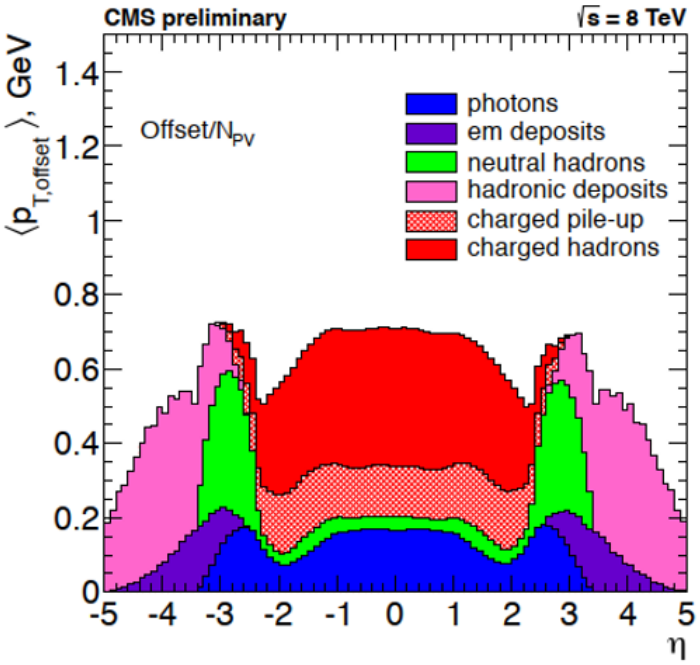


Figure 6.33: Breakdown of the average offset transverse momentum $\langle p_{T,\text{offset}} \rangle$ per primary vertex, shown as a function of pseudorapidity η, for events with a single pile-up interaction. The contributions from different particle-flow (PF) candidates are indicated: photons, electromagnetic deposits, neutral hadrons, hadronic deposits, charged pile-up, and charged hadrons. This figure is reproduced from figure 9.4 (left) of Ref. [14].

The timing performance extracted from selected channels of the silicon Hex-Module is summarized in Table 6.11. Among the studied channels, Channel 135 yields the lowest extracted values, with a noise coefficient $A \sim 10\,\text{ns}$ and a constant term $C = 26\,\text{ps}$. A comparable performance is also observed for Channel 158 under varying temperature conditions (Section 6.7), with $A \sim 10\,\text{ns}$ and $C \sim 27\,\text{ps}$. However, as this evaluation is based on only three channels, no definitive conclusions can be drawn regarding channel-to-channel performance uniformity. Within this limited dataset, the extracted parameters suggest that A is on the order of 10 ns and C is approximately 30 ps—both exceeding the TDR expectations of $A = 5\,\text{ns}$ and $C = 20\,\text{ps}$. A more statistically robust assessment will require broader sampling across multiple modules and operational conditions.

The increased noise term (A) suggests that TOA jitter exhibits highy sensitivity to fluctuations in the signal-to-noise ratio, potentially degrading timing precision, particularly at low signal amplitudes. Similarly, the elevated constant term (C) indicates systematic constraints in intrinsic timing resolution, likely arising from clock jitter, TOA Calibration procedures, and the power distribution response to high frequcncy transients. These deviations from the TDR expectations have direct implications for the reconstruction of neutral hadrons and photons, impacting energy resolution, pileup rejection efficiency, and time-tagging precision.

6.9.1 Simulation setup and timing performance evaluation

To evaluate the timing performance of reconstructed showers in HGCAL, a full simulation was conducted using a single-particle gun to generate neutral kaons (K_L^0) and photons (γ) within the energy range $1 < E < 120$ GeV at pseudorapidity $|\eta| = 2$. The simulation was performed in the absence of pileup effects to isolate intrinsic detector performance.

The GEANT4-based [118] simulation framework was employed to model particle interactions within the calorimeter geometry. The simulated ToA was computed using an energy-weighted average over all hit cells, where each contribution was scaled by the corresponding deposited energy. This approach reflects the typical behavior of electromagnetic showers, where high-energy deposits near the shower core arrive earlier and dominate the timing response. To incorporate realistic detector effects, the reconstructed hits were subsequently subjected to stochastic smearing. The timing resolution was modeled using a parameterization involving a noise-dependent term (A) and a constant term (C), with values extracted from laser-based timing measurements, as detailed in Section 6.6.6. These parameters, measured using laser injection as described in Section 6.6.6, are listed in Table 6.11 to ensure an accurate representation of the detector's intrinsic timing resolution.

The Cambridge-Aachen jet algorithm ($R = 0.4$) [119] was applied for hit clustering, followed by additional selection constraints restricting hits within a spatial cylinder of radius, $\rho < 3$ cm, ensuring that only primary interaction showers were retained. Scintillator-based hits were omitted to focus the study solely on silicon sensor performance.

A comprehensive simulation study (a super set of this study) of neutral hadron and photon reconstruction across the full pseudorapidity range ($1.8 < |\eta| < 2.8$) with TDR specifications ($A = 5$ ns, $C = 20$ ps) for the start-of-life conditions and for an aged detector scenario corresponding to 3000 fb^{-1} of integrated luminosity, was performed by DPG, and can be found in Refs. [30, 120].

Multiple simulation scenarios were defined by varying the noise term (A) and constant term (C) and are listed in table 6.12, where Scenario 1 corresponds to the baseline configuration, and subsequent scenarios introduce progressive modifications in the timing parameters to evaluate their effects on shower reconstruction.

Scenario	Noise Term A (ns)	Constant Term C (ps)
1 (TDR Baseline)	5	20
2	6	20
3	6	30
4	6	40
5	10	20
6 (Ch:158)	10	30
7	10	40

Table 6.12: Simulated scenarios for K_L^0 and photon timing resolution performance.

These scenarios allow for a comparative analysis of the impact of timing degradation on shower reconstruction, highlighting potential performance variations under different detector conditions.

To evaluate the impact of TOA threshold settings, the key efficiency parameters are define below:
Shower Time-Tagging Efficiency: The time-tagging efficiency (ε) quantifies the probability of correctly associating a simulated K_L^0 shower with the event timestamp. It is defined as:

$$\varepsilon = \frac{K_L^0(N_{\text{hits}}^{\text{rec}} \geq 3 \;\&\; q^{\text{rec}} > 12\,\text{fC})}{K_L^0(N_{\text{hits}}^{\text{sim}} \geq 3)} \tag{6.8}$$

Here, K_L^0 denotes the number of generated neutral kaons. The numerator counts events with at least

three reconstructed hits ($N_{\text{hits}}^{\text{rec}} \geq 3$), where a reconstructed hit is defined as a silicon sensor cell registering a signal with charge $q^{\text{rec}} > 12\,\text{fC}$ and crossing the ToA threshold. The denominator includes events with at least three simulated energy deposits ($N_{\text{hits}}^{\text{sim}} \geq 3$), without any applied threshold or timing conditions. Hits are not required to be adjacent and may be distributed across multiple calorimeter layers.

Efficiency Threshold ($Eff.Thr$): The efficiency threshold is defined as the minimum energy required to achieve 95% efficiency. As illustrated in figure 6.35 (left-top), the efficiency threshold corresponds to the value on the energy axis intersect by the red vertical dashed line.

Efficiency Width ($Eff.wdt$): The efficiency width represents the transition region between low efficiency and full efficiency. It quantifies how smoothly the efficiency rises from the minimum to 95% efficiency, shown by the length of double headed arrow in the figure 6.35 (left-top).

TOA Resolution Parameterization: The TOA resolution of the reconstructed shower is modeled as:

$$\sigma_{\text{ToA}} = \sqrt{\frac{A^2}{E^2} + C^2}. \tag{6.9}$$

In this expression, E represents the true energy of the incident particle shower, measured in GeV. The parameter A denotes the noise term, which dominates the resolution at low energies. The constant term C reflects the intrinsic timing resolution of the system and becomes the leading contribution at high energies.

The study systematically explores how variations in A and C of single channel, impact shower time-tagging efficiency and TOA resolution. The results, presented in subsequent sections, provide a comparative analysis of the effect of different timing configurations on the reconstruction of neutral hadrons and photons.

6.9.2 Effect of TOA threshold on shower time-tagging efficiency threshold

The efficiency threshold for shower time-tagging in the CMS HGCAL depends strongly on the ToA threshold set in the HGCROC. This threshold is defined as $V_{\text{ref-ToA}}$ at the channel level and is referred to as q^{rec} when discussing shower-level performance. Although the names differ, both represent the same physical threshold value. Figure 6.34 shows how the time-tagging efficiency varies with q^{rec}, comparing the response for neutral kaons (K_L^0) and photons (γ). The plot highlights the different sensitivities of these particles to threshold settings, reflecting their distinct shower characteristics.

In both panels of figure 6.34, the efficiency threshold exhibits a strong dependence on the applied ToA threshold, with the effect more pronounced for neutral kaons than for photons. As seen in both curves, increasing the q^{rec} threshold results in a higher energy threshold for achieving efficient time-tagging. In practical terms, applying a higher ToA threshold favors the selection of high-energy kaon or photon signals, but significantly suppresses contributions from lower-energy deposits—particularly in neutral hadron showers. This leads to a reduction in overall reconstruction efficiency, especially for particles such as K_L^0, which typically produce softer showers.

The efficiency of ToA tagging in the CMS HGCAL is highly sensitive to the effective ToA threshold (Eff-Th), which directly depends on the reference voltage $V_{\text{ref-ToA}}$ or, equivalently, the reconstructed threshold charge q^{rec}. To comply with the performance specifications defined in the HGCAL TDR, achieving a minimum threshold of 12 fC was established as a critical target.

However, this goal was not attainable in the early versions of the silicon Hex-Modules. The first and second prototype designs exhibited significant pedestal modulation (Δ-pedestal) across sampling phases, ranging from 100 to 180 ADC units, as shown in Tables 5.1, 5.2 and figure 6.4. Such large modulation values constrained the minimum achievable threshold, requiring $V_{\text{ref-ToA}}$ to be set as high as 120 fC, which would have led to substantial inefficiency in detecting low-energy shower constituents.

To overcome this limitation, I carried out a complete redesign and optimisation of the PCB stack-up (Section 5.6). I along the chip designer (from OMEGA, Paris) investigated the root causes of dig-

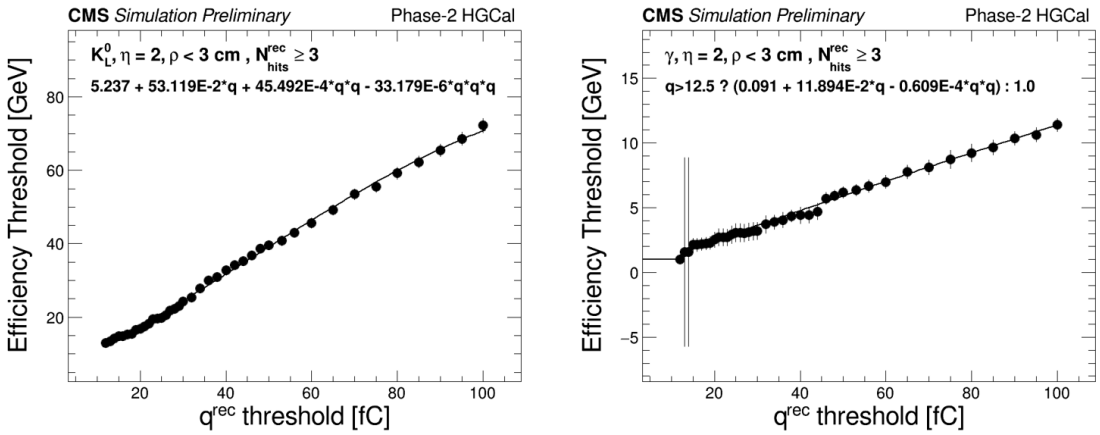


Figure 6.34: Efficiency threshold as a function of the ToA threshold q^{rec} for neutral kaons (K^0_L, left) and photons (γ, right) in the CMS HGCAL. The results are obtained from dedicated simulation studies performed at $\eta = 2.0$, using timing parameters consistent with test bench measurements. The simulations assume a noise term $A = 10\,\text{ns}$ and a constant term $C = 30\,\text{ps}$, corresponding to the performance observed in silicon Hex-Modules calibrated with a laser system.

ital pedestal modulation (Section 5.11), developed grounding strategies for both the Hexaboard and HGCROC package. I validated improvements through extensive PCB simulations and multiple prototype iterations, performed systematic lab tests and incorporated feedback from each development cycle into the next design version.

As a result of these efforts, both the V3-HD and V3-LD on-cassette Hexaboard designs have successfully achieved a stable ToA threshold near 12 fC. This significant improvement not only meets the TDR-defined specification but also enables improved time-tagging efficiency, particularly for low-energy shower components—ensuring optimal performance of the HGCAL timing system.

The choice of TOA threshold is therefore paramount in preserving optimal shower time-tagging efficiency, particularly for neutral hadrons. A threshold of 12 fC ensures a suitable balance between efficiency and detector noise suppression. Beyond this threshold, the efficiency for neutral kaon detection declines significantly, emphasizing the necessity of meticulous threshold optimization for ensuring robust calorimetric performance under high pile-up conditions.

6.9.3 Shower time-tagging efficiency at TOA threshold $q^{rec} = 12$ fC

The efficiency of shower time-tagging and the TOA resolution were systematically analyzed for neutral kaons (K^0_L) and photons (γ) under different single-channel timing resolution scenarios, as summarized in Table 6.12. Figures 6.35 and 6.36 illustrate the dependence of time-tagging efficiency and TOA resolution for kaons and photons, respectively.

Each figure consists of two rows:

- In the upper row, the figure shows efficiency versus shower energy, with details of Efficiency threshold and the Efficiency width.
- The lower row illustrates the TOA resolution as a function of energy with details of Noise term A and Constant term C.

Both figures are organized into three columns, each corresponding to a distinct timing resolution configuration:

- **TDR Baseline (Left Column):** Represents the nominal target performance defined in the HGCAL TDR [6], with $A = 5$ ns and $C = 20$ ps.
- **Channel 35 like case (Middle Column):** Reflects a representative measurement of Channel 35 or 158 fom Table 6.11, with moderately increased jitter parameters: $A = 10$ ns and $C = 30$ ps.
- **Assumed Worst-Case Scenario (Right Column):** Illustrates the impact of further degradation in constant term resolution, assuming $A = 10$ ns and an elevated $C = 40$ ps, to evaluate system performance under pessimistic timing conditions.

A detailed summary of the efficiency thresholds, widths, and TOA timing parameters across these scenarios is provided in Table 6.13.

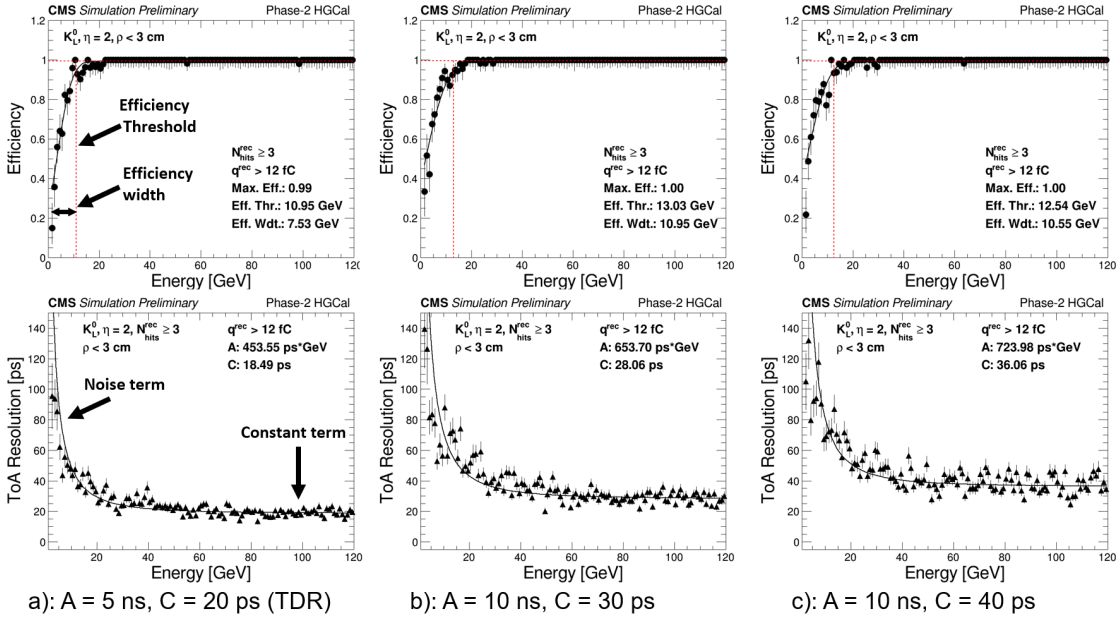


Figure 6.35: Time-tagging efficiency (top row) and TOA resolution (bottom row) for K_L^0 in HGCAL under different timing resolution scenarios. The vertical red dashed line in the top-left plot represents the efficiency threshold (Eff. Thr.), while the horizontal double-ended arrow denotes the efficiency width (Eff. Wdt.). The first column (left) corresponds to the TDR baseline ($A = 5$ ns, $C = 20$ ps), where the efficiency threshold is measured at Eff. Thr $= 10.95$ GeV and the efficiency width at Eff. Wdt $= 7.53$ GeV. The second column (middle) shows the performance for Channel 35 ($A = 10$ ns, $C = 30$ ps), where degraded timing precision increases Eff. Thr to 13.03 GeV and expands Eff. Wdt to 10.95 GeV. The third column (right) illustrates the worst-case scenario ($A = 10$ ns, $C = 40$ ps), where the efficiency threshold stabilizes at Eff. Thr $= 12.54$ GeV, and the efficiency width contracts slightly to Eff. Wdt $= 10.55$ GeV. The bottom row highlights TOA resolution degradation at lower energy, emphasizing its impact on neutral hadron reconstruction.

Impact on Neutral Kaon reconstruction Figure 6.35 illustrates the time-tagging efficiency and TOA resolution for neutral kaons (K_L^0). The efficiency threshold (Eff. Thr) and efficiency width (Eff. Wdt) are key parameters that determine the detection performance for different timing resolution conditions.

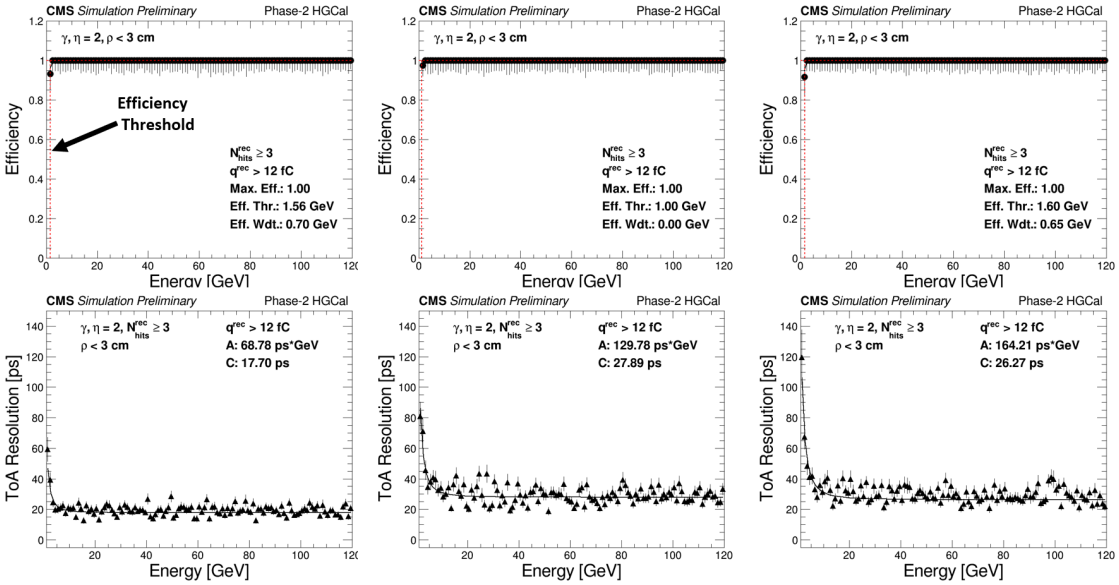


Figure 6.36: Time-tagging efficiency (top row) and TOA resolution (bottom row) for photons reconstructed in HGCAL under different single-channel timing resolution conditions. The left column represents the TDR baseline ($A = 5$ ns, $C = 20$ ps), the middle column corresponds to Channel 35 ($A = 10$ ns, $C = 30$ ps), and the right column illustrates the worst-case scenario ($A = 10$ ns, $C = 40$ ps). Unlike kaons, the efficiency threshold remains stable across scenarios, highlighting the minimal sensitivity of photon reconstruction to TOA parameter variations. The bottom row demonstrates the TOA resolution as a function of energy, revealing minor degradation with increasing A and C, yet maintaining robust photon reconstruction performance.

From the figure, it is evident that increasing A and C leads to a shift in the efficiency threshold towards higher energy values. In the TDR Baseline scenario, the efficiency threshold is observed at 10.95 GeV, while in Channel 35, it increases to 13.03 GeV. In the worst-case scenario, the threshold slightly decreases to 12.54 GeV. The efficiency width follows a similar trend, expanding from 7.53 GeV (TDR Baseline) to 10.95 GeV (Channel 35), before narrowing slightly to 10.55 GeV in the worst-case scenario.

These trends are quantitatively summarized in Table 6.13, which lists the efficiency parameters and TOA resolution across the different configurations. The table shows that the increase in A and C leads to an overall degradation in efficiency for kaon reconstruction, particularly affecting low-energy hadronic showers. The broadening of the efficiency width indicates increased uncertainty in kaon detection, which could contribute to energy mis-measurement in jet reconstruction.

These results highlight the sensitivity of neutral hadron reconstruction to TOA timing degradation. The increase in the efficiency threshold implies that fewer low-energy kaons are detected, leading to an underestimation of the hadronic shower energy. The efficiency width broadening further suggests a loss of precision in time-tagging, potentially increasing pileup contamination. Given these effects, maintaining a TOA threshold at 12 fC is critical to preserving the accuracy of neutral hadron reconstruction in HGCAL.

Impact on Photon reconstruction Figure 6.36 presents the time-tagging efficiency and TOA resolution for photons (γ). In contrast to neutral kaons, the efficiency threshold remains stable across all tested scenarios, with a value close to 1.56 GeV. This indicates that photon reconstruction is largely unaffected

Index	Particle	A [ns/(S/N)]	C [ps]	Eff. threshold [GeV]	Eff. width [GeV]	A [ps/GeV]	C [ps]
0	K_L^0	**5**	**20**	**10.95**	**7.53**	**454.00**	**18.00**
1	K_L^0	6	20	13.71	11.02	460.00	19.00
2	K_L^0	6	30	12.07	10.09	433.00	27.00
3	K_L^0	6	40	9.66	5.82	481.00	35.00
4	K_L^0	10	20	12.06	8.88	691.00	18.00
5	K_L^0	10	30	13.03	10.95	654.00	28.00
6	K_L^0	10	40	12.54	10.55	724.00	30.00
7	γ	**5**	**20**	**1.56**	**0.70**	**68.60**	**26.55**
8	γ	6	20	1.56	0.27	0	26.55
9	γ	6	30	1.11	11.93	69.17	27.54
10	γ	6	40	1.65	0.60	75.09	34.54
11	γ	10	20	1.58	0.69	158.08	18.09
12	γ	10	30	1.00	0.00	129.78	27.98
13	γ	10	40	1.60	0.65	164.21	26.27

Table 6.13: Efficiency and Timing Parameters for Simulated K_L^0 and Photon (γ) events. The bold text represents the TDR (or reference) scenarios. The second column indicates the particle type used in the simulation study. The third and fourth columns list the noise term A [ns/(S/N)] and constant term C [ps], which characterize the silicon Hex-Module channels. The next two columns provide the efficiency threshold and efficiency width. The final two columns represent the noise term A [ps/GeV] and constant term C [ps] for the reconstructed shower timing resolution.

by variations in TOA timing parameters.

Table 6.13 confirms this trend, showing minimal changes in efficiency width and TOA resolution across the three configurations. The worst-case scenario results in only minor timing degradation, but the overall impact on photon energy measurement remains negligible.

Unlike neutral hadrons, which exhibit a strong dependence on TOA resolution, photons demonstrate resilience to timing degradation. Even under the worst-case scenario, the efficiency threshold and width remain nearly unchanged, ensuring robust performance in high-luminosity conditions. These findings confirm that the 12 fC TOA threshold is particularly crucial for neutral kaon reconstruction, whereas photon detection remains stable across a range of TOA conditions. The Neutral kaons (K_L^0) are more sensitive to timing resolution degradation compared to photons is due to their distinct interaction mechanisms. Photons, as purely electromagnetic particles, produce showers through rapid energy deposition in the electromagnetic calorimeter (ECAL), resulting in localized and well-contained energy profiles. In contrast, neutral kaons, as hadrons, undergo complex hadronic interactions, leading to broader, more stochastic showers with delayed energy deposition [121, 122]. This delayed energy deposition increases susceptibility to timing resolution degradation, leading to a higher efficiency threshold and broader efficiency width in hadronic showers compared to electromagnetic showers.

6.9.4 Implications for pileup mitigation and event reconstruction

The increase in efficiency threshold (Eff. Thr) from 10.95 GeV to 13.03 GeV directly impacts pileup mitigation strategies and event reconstruction. To see this impact, an example of the $H \to \gamma\gamma$ process is adopted from reference [30] and shown in figure 6.37. The left panel illustrates the energy spectra of neutral hadrons, while the right panel presents the corresponding spectra for electromagnetic particles in VBF CaloJets (reconstructed jet from calorimeter energy deposits in a VBF-like event topology) [30]. The different curves represent various reconstruction techniques, including Raw, Soft-Killer (SK) [119],

and SK+Time tagging, allowing a comparative evaluation of their effectiveness in pileup mitigation.

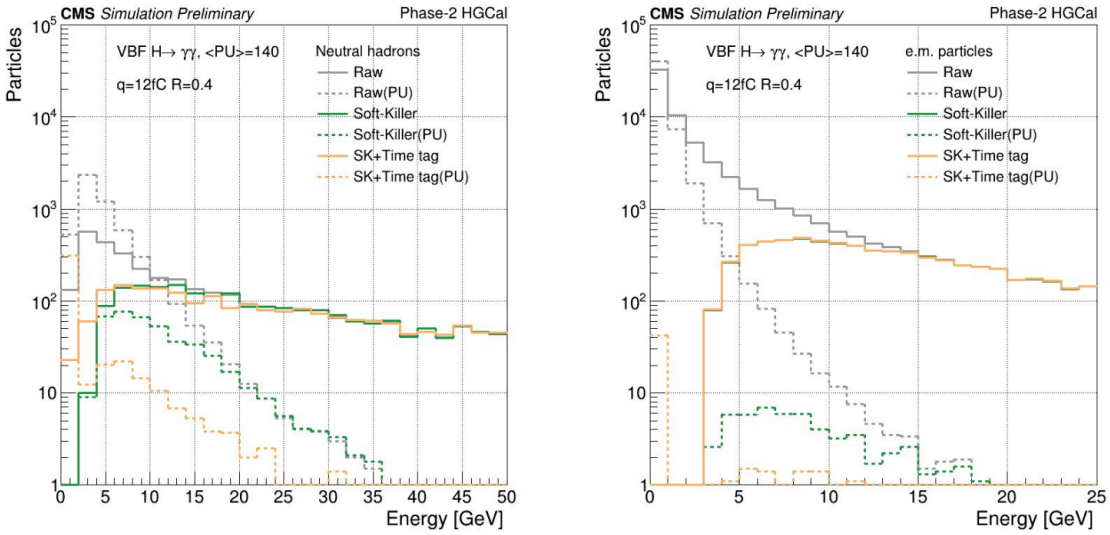


Figure 6.37: Energy spectra of stable neutral hadrons (left) and electromagnetic particles (right) in generator-level particle CaloJets with $R = 0.4$, reaching the HGCAL volume in VBF H$\rightarrow \gamma\gamma$ events with an average pileup of $\langle PU \rangle = 140$. The charge threshold for ToA is set at $q = 12$ fC. The spectra of the signal (solid lines) and pileup particles (dashed lines) are shown separately. The impact of Soft-Killer (SK) pileup mitigation and SK combined with time-tagging is illustrated by the energy distribution of the surviving particles within the matched CaloJets, adopted from [30].

Under TDR specifications, a 10 GeV energy cut effectively filtered out most pileup-induced energy deposits, with timing tagging employed to suppress additional contamination. However, with an efficiency threshold exceeding 13 GeV, the same cut results in loss of low-energy hadronic showers. Retaining events below this threshold, on the other hand, introduces pileup contamination that distorts jet energy resolution and affects event classification.

The fraction of affected events can be estimated from the reconstructed shower composition. As seen in figure 6.33, neutral hadrons contribute approximately 15% of the total reconstructed shower contents in the barrel region. This estimate can be reasonably extended to the endcap region, as the peak observed in the endcap primarily arises from the lack of a tracking detector in Phase-I. In Phase-II, this limitation will be mitigated with extended tracker coverage, ensuring a more uniform distribution.

Photons account for approximately 30% of the total reconstructed shower content, while the remaining fraction is predominantly composed of charged hadrons. While photon reconstruction remains robust against this threshold shift, a fraction of neutral kaons (which are $\sim$ 10% - 15% of shower contents), will be affected. However, given the relatively small contribution of neutral hadrons to the overall shower composition, the overall impact on the physics performance remains marginal and does not significantly affect the physics objectives of HGCAL.

These findings conclude the study, affirming that despite the increase in the efficiency threshold, the primary physics goals of HGCAL remain uncompromised. The analysis demonstrated that the impact of TOA resolution variations is most pronounced for neutral hadrons due to their exclusive reliance on calorimetric information. However, given that neutral hadrons constitute only a small fraction of the overall shower composition, this effect remains marginal in terms of its impact on the physics performance of HGCAL. The efficiency shift primarily affects a fraction of neutral kaons, but due to their limited contribution to hadronic showers, the overall event reconstruction remains robust. Photon reconstruction, on

the other hand, remains stable under TOA variations, reaffirming the reliability of the current timing and energy threshold settings.

Several advancements in the real detector environment are expected to further mitigate these effects. Some of these improvements are further elaborated in the next section.

These developments, combined with optimized reconstruction algorithms and enhanced timing calibration, will ensure that HGCAL meets its stringent performance requirements. The improved precision will be particularly valuable in high-pileup environments, maintaining accurate time-tagging for both neutral and electromagnetic showers while minimizing background contamination. As the system moves toward final implementation, continuous refinements in calibration, electronics, and software algorithms will further strengthen HGCAL's capability to operate in the demanding conditions of the HL-LHC.

6.10 Outlook and Future Work

Advancing the time resolution capabilities of the silicon Hex-Modules within the HGCAL system remains a critical objective. Future work will focus on refining the calibration processes, improving noise characterization, and implementing innovative measurement techniques to ensure the high level of precision. The following key areas highlight the path forward:

Enhancing TDC calibration methods

One of the primary steps in improving time resolution is the refinement of TDC calibration methods. Current practices have revealed challenges in achieving consistent bin widths and producing Gaussian-distributed TOA histograms. Moving forward, we will focus on refining these calibration procedures to reduce errors, eliminate noise-induced outliers, and enhance the uniformity and accuracy of timing measurements across all channels.

Implementing differential time jitter measurements

To obtain more accurate assessments of time jitter, an upgraded experimental setup which allows simultaneous signal injection into two channels, is recommended. By measuring the time jitter of one channel relative to another, we can effectively remove common-mode noise components. This differential approach is anticipated to yield a clearer, more accurate representation of the true timing performance of the silicon Hex-Modules.

Optimizing clock distribution and power management

The accuracy of time resolution in silicon Hex-Modules is significantly influenced by the quality of clock distribution and the stability of power supply systems. As such, future efforts must prioritize optimizing these areas to enhance overall performance. Although the Hexaboards are already in production, limiting the potential for further improvements at the PCB level, there are still crucial steps that can be taken to mitigate noise and reduce jitter in the system.

One of the primary strategies involves ensuring that all devices within the system operate with the lowest possible electronic jitter and noise levels. By providing a cleaner clock signal at the input of the HGCROC, the jitter associated with the Phase-Locked Loop (PLL) can be minimized, leading to an improvement in the module's minimum time resolution. Reducing PLL jitter is essential, as it directly impacts the precision of timing measurements and the overall performance of the module.

In terms of power management, it is strongly recommended to utilize the latest DCDC converter boards, which offer better shielding capabilities. Improved shielding is critical to preventing any potential increase in noise levels that could adversely affect the Hexaboard's performance. By focusing on these optimizations, cleaner clock signals and enhanced power supply stability, significant advancements in the time resolution of the silicon Hex-Modules can be achieved, ultimately contributing to the success of the HGCAL system in high-energy physics experiments.

6.11 Conclusion

This chapter evaluated the performance of HGCAL silicon sensor modules through three key phases: validation via beam tests, timing characterization using a laser system, and simulation-based analysis of their impact on HGCAL physics performance for neutral hadrons and photons.

A series of beam tests conducted in 2021, 2022, and 2023 systematically assessed the silicon modules, leading to iterative design refinements aligned with HGCAL requirements. The signal-to-noise (S/N) ratio for MIP detection was the primary performance metric, measured by directing focused electron or pion beams onto silicon module cells. The 2021 beam tests, using NSH-Silicon Modules with HGCROC-V2 and V3 ASICs, led to critical pedestal and noise corrections. Post-correction S/N values of 7.9 (at HGCROC's medium gain) and 9.9 (HGCROC's low gain) fell below the TDR target of 11 but guided subsequent optimizations. The 2022 campaign, featuring V3-LD silicon modules with 300 µm sensors, demonstrated substantial improvements, with S/N values of 14.5, 12.8, and 8.5 across high, medium, and low gain settings, surpassing the TDR goal for medium gain. The 2023 beam tests extended this validation to LD-Full, LD-Semi, and HD-Full configurations with 200 µm, 300 µm, and 120 µm sensors. All modules met or exceeded design specifications, with the HD-Full achieving an S/N of 4.8 (target: 4.5) and the LD-Full recording 8.4 (target: 6). The LD-Semi modules, with S/N values around 12, outperformed expectations, affirming the readiness of these designs for HGCAL integration.

To assess the timing capabilities of these modules, a dedicated laser-based system was developd, enabling precise charge injection into silicon sensor cells. The setup included a 1064 nm pulsed laser, an optical attenuator, and motorised XYZ scanning stages, with synchronised operation via a 10 MHz clock source to ensure accurate timing alignment. Initial laser jitter measurements showed a timing uncertainty of 15 ps; however, with an improved clock source, the jitter was reduced to 5 ps RMS, enhancing the precision of the timing measurements. The timing resolution study yielded a noise term of approximately 10 ns and a constant term of 27 ps, compared to the TDR objectives of 5 ns and 20 ps. Temperature-dependent studies indicated negligible variation in timing performance but revealed a temperature-linked dependency in charge collection efficiency, attributed to silicon band gap fluctuations.

The observed deviations from TDR benchmarks were attributed to multiple factors, including non-Gaussian behaviour at low signal amplitudes due to electronic noise, clock jitter from the HGCROC's Phase-Locked Loop (PLL), and systemic noise from impedance mismatches and environmental conditions. Despite these challenges, the laser system provided critical insights for refining module calibration and optimising detector timing performance.

The final phase of this study integrated the measured timing parameters into HGCAL physics simulations to evaluate their impact on the reconstruction of neutral hadrons (K_L^0) and photons (γ), as these particles rely entirely on calorimetric measurements. The study simulated single-particle gun events with energies up to 120 GeV at pseudorapidity $\eta = 2$, focusing on the influence of time-of-arrival resolution on shower efficiency and pileup mitigation. The results confirmed that timing resolution significantly affects neutral hadron reconstruction efficiency. The efficiency threshold for K_L^0 increased from 10.95 GeV (TDR baseline) to 13.03 GeV when using timing parameters from Channel 158 ($A = 10$ ns, $C = 30$ ps), indicating reduced detection efficiency for low-energy hadronic showers, which could influence jet energy measurements and pileup rejection. Conversely, photon reconstruction remained robust across all tested timing conditions, reflecting the inherently stable nature of electromagnetic showers in the ECAL. The broader fluctuations in hadronic interactions within the HCAL rendered neutral hadrons more sensitive to timing resolution degradation. However, given that neutral hadrons constitute approximately 10-15% of shower constituents, the observed reduction in efficiency has a marginal impact on overall HGCAL physics performance.

With the successful qualification of silicon module performance in beam tests and precision timing characterization, the production of readout boards has now reached an advanced stage, with most units having undergone initial testing. These developments mark a significant milestone in the integration of

HGCAL electronics, ensuring readiness for large-scale deployment in the upcoming experimental phase.

Chapter 7

Conclusion and future work

The HL-LHC, set to begin operations later this decade, promises an integrated luminosity of up to 3000 fb^{-1}, enabling unprecedented opportunities for refining the existing results and exploring new physics. However, the extreme conditions of higher collision rates, elevated radiation levels, and high pileup of 140 to 200 will push the CMS detector beyond its original design limits. Specifically, the endcap regions, subjected to the highest particle flux and radiation, will see a significant degradation in the performance of the electromagnetic and hadronic calorimeters (ECAL and HCAL), necessitating substantial upgrades to maintain the precision and reliability required for advanced physics analyses. By leveraging these advanced technologies, the HGCAL ensures that the CMS detector remains resilient under the harsh conditions of the HL-LHC and continues to deliver high-precision data essential for groundbreaking discoveries in particle physics.

The High Granularity Calorimeter (HGCAL) is an advanced detector tailored to address the unprecedented challenges of the HL-LHC. Its intricate architecture comprises 47 finely segmented layers, divided into electromagnetic (CE-E) and hadronic (CE-H) compartments. These layers provide a combined depth of 25 radiation lengths and 10 interaction lengths, ensuring complete shower containment. The CE-E utilizes absorbers, such as copper-tungsten and lead, while the CE-H employs stainless steel, complemented by silicon sensors and plastic scintillators as active media. To balance performance, silicon sensors are deployed in three thicknesses (120 μm, 200 μm, and 300 μm) and two pad sizes (0.5 cm^2 and 1.18 cm^2) in the CE-E and high-fluence regions of CE-H. In low-radiation regions of CE-H, plastic scintillators read by Si-PMs are used.

The HGCAL introduces 5D imaging capabilities, capturing spatial coordinates (x, y, z), energy (E), and time (t). This precision enables detailed shower reconstruction, effective pileup mitigation, and advanced physics object reconstruction. Combined with the extended coverage of the CMS tracker to $|\eta| < 4.0$, the inclusion of precise timing measurements allows for four-dimensional vertexing. By integrating time-of-arrival measurements with a resolution of approximately 30 ps RMS, HGCAL significantly reduces the number of pileup tracks misassociated with the primary vertex. This enhancement is critical for reconstructing events under the extreme conditions of the HL-LHC, where pileup densities touches 200 interactions per bunch crossing.

HGCAL's granular design ensures exceptional energy resolution, vital for processes like $H \to \gamma\gamma$. Simulation studies demonstrate an invariant mass resolution of $\sigma_M = 1.61 \pm 0.02\%$, corresponding to approximately 2 GeV, even under high pileup. Furthermore, HGCAL improves photon detection efficiency by 12%, enhancing the analysis of rare processes, such as Vector Boson Fusion decays. These capabilities establish HGCAL as a cornerstone of the CMS detector upgrade, enabling the precision and sensitivity required to explore new physics in the high-luminosity era of the LHC.

The objective of this Ph.D. research was to design, optimize, and implement a robust front-end readout system for the silicon region of the HGCAL in preparation for the challenging conditions expected during the HL-LHC phase. The work spanned several critical domains, including the design and optimization of Hexaboards, the development of testing systems for the Hexaboard characterization, the validation of the silicon module performance in beam tests, and the development of a laser system with control over timing and attenuation for the in-depth timing characterization of silicon modules. Each component of this effort was meticulously planned and executed, addressing unique challenges and contributing to the overall advancement of HGCAL technology.

The primary focus of this thesis was the design optimization of Hexaboards, the readout boards for the silicon region of the HGCAL, hosting 72-channel HGCROC ASICs. HGCROC play a critical role in signal readout, including charge and TOA measurements, as well as transmitting and processing data for DAQ and trigger systems. To accommodate the diverse geometries of the silicon sensors, 11 Hexaboard variants were developed, including two full hexagonal boards and nine partial designs tailored for the peripheral regions of the detector. The optimization process was highly iterative, involving multiple cycles of prototyping, designing, testing, debugging, and incorporating feedback into subsequent versions. Design validation was primarily assessed using two benchmarking parameters: pedestal noise (standard deviation of 10,000 ADC samples per channel) and Δ-pedestal (the amplitude of pedestal variation across 16 sampling phases of 40 MHz). These metrics, discussed in section 5.2, were central to evaluating the performance improvements across prototypes.

The prototyping and design optimization focused on the LD (Low Density) version, which was chosen as a starting point before transitioning to the HD (High Density) design. The three LD Hexaboard prototypes, shown in figure 5.7, represent the evolution of the design process, demonstrating progressive enhancements in performance, manufacturability, and compliance with the stringent requirements of HGCAL.

The first prototype, LD-HB-CMS-V1, introduced a stack-up inspired by the earlier 6" hexaboard design and incorporated stepped-hole structures for bonding. While this iteration served as an essential proof-of-concept platform, its performance was hampered by high digital noise levels (up to 50 ADC units for bare Hexabard and larger than 100 ADC units in silicon modules) and inadequate shielding between the analog channels and digital circuitry. Despite these limitations, it provided valuable insights into manufacturing challenges, yielding key feedback for improving the process, such as copper balancing, bonding pad enhancements, and glue-seepage mitigation. This version also contributed to the development of module assembly procedures and tools, forming the foundation for subsequent iterations.

Building on the lessons learned, the second prototype, LD-NSH-HB-V2, adopted the optimized Stack-up-II configuration, integrated PCB simulation into the design loop, and replaced the stepped-hole structures with non-stepped holes to reduce the manufacturing complexity and production time. This iteration significantly improved noise performance, with pedestal noise reduced to 1.3 ADC units for the bare board and 2.4 ADC units for assembled modules. The Δ-pedestal was also reduced to 4 ADC units for the bare board and $\sim$17 ADC units for the silicon module assembled with HGCROC-V2, marking a tenfold improvement over the first version. However, when these boards were assembled with the newer HGCROC-V3, a drastic increase in Δ-pedestal to 170 ADC units was observed, triggering new R&D efforts discussed in section 5.11. This investigation revealed the necessity of maintaining separate low-impedance return paths for analog and digital grounds, both at the package level and on the top layer beneath the BGA. These findings emphasized the importance of incorporating PCB simulations in the design loop to identify and resolve potential issues before fabrication. While this version validated the new stack-up and addressed many design limitations, further refinements were required to meet the stringent noise and signal-to-noise ratio targets specified in the HGCAL Technical Design Report (TDR).

The final iteration, V3-LD-Hexaboard-V1.3, represents the culmination of the design optimization process. Featuring the HGCROC-V3 ASIC and incorporating all enhancements from earlier versions, this design achieved exceptional performance metrics. Pedestal noise was reduced to 1.0 ADC units

for the bare board and 1.5 ADC units for modules (equivalent to approximately 1900 electrons), with a Δ-pedestal of 9 ADC units. The signal-to-noise ratio (S/N) for the final module reached 11, meeting the stringent TDR specifications. Additionally, the design was refined for manufacturability, addressing constraints such as on-detector mechanical integration, service routing, and compatibility with the MAC requirements. These advancements ensure the V3-LD-Hexaboard is fully prepared for deployment under the high-luminosity conditions of the HL-LHC. The results presented in Table 5.1 and figures 5.16 and 5.17 showcase a clear trend of design enhancement across iterations. While the initial version (LD-HB-CMS-V1) and its module suffered from excessive noise and instability, the V3-LD-HB and V3-LD-Hex-Module achieved significant improvements. Their alignment with the HGCAL TDR requirements and the ENC benchmark (Figure 5.3) underscores their suitability for high-precision detector applications.

Building on the LD Hexaboard experience, the HD Hexaboard design incorporated key recommendations, including isolated analog and digital grounds with low-impedance paths. The Via-in-Pad technique was adopted to minimize parasitic inductance, improve signal integrity, and optimize spacing beneath the BGA. Performance evaluation showed that the V3-HD-Hexaboard achieved average noise and Δ-Pedestal values of ∼0.93 ADC units and ∼2 ADC units, respectively, for the bare board. When integrated into an HD silicon Hex-Module with 120 µm silicon, these values remained well-controlled at ∼1.7 and ∼5.6 ADC units, compared to 2.5 and 175 ADC units for the NSH-Module with the same HGCROC-V3 ASICs, demonstrating full compliance with HGCAL Technical Design Report requirements.

The silicon modules underwent extensive validation across a series of beam tests conducted in 2021, 2022, and 2023, showcasing the iterative improvement of their designs. Each testing phase integrated feedback from prior evaluations, ensuring progressive enhancements in performance and compliance with stringent HGCAL requirements. Signal-to-Noise (S/N) ratio for MIP detection served as the primary benchmark, achieved by targeting silicon module cells with a focused electron or pion beam without an absorber plate, enabling precise signal analysis within a narrow beam profile.

The 2021 beam tests were conducted on the NSH-Silicon Module, incorporated with NSH-hexaboard and 300 um, assembled with HGCROC-V2 and V3 ASICs. These tests marked a crucial milestone, yielding algorithms for pedestal and common mode noise corrections to address varying noise contributions and ensure accurate signal reconstruction. After applying these corrections, the MIP signals achieved S/N ratios of ∼7.9 and ∼9.9 for preamplifier gains in medium (160 fC ADC range) and low (300 fC ADC range), respectively. While these results fell short of the target S/N value of 11 outlined in the HGCAL TDR [6], they provided critical insights that guided subsequent improvements in module design and data processing.

Building on these advancements, the 2022 beam tests evaluated V3-LD silicon modules, featuring the V3-LD-Hexaboard and 300 µm-thick silicon sensors. These modules demonstrated remarkable performance, with S/N ratios of 14.5, 12.8, and 8.5 for high (80 fC ADC range), medium, and low gains, respectively. Notably, the medium gain S/N value exceeded the TDR target of 11, validating the robustness of the V3-LD-Hexaboard design and establishing it as a reliable platform for silicon module integration.

The 2023 beam tests extended this validation to include four distinct module configurations: LD-Full, LD-Semi (left and right), and HD-Full, incorporating sensors with thicknesses of 200 µm, 300 µm, and 120 µm. The results demonstrated that all modules met or exceeded the design specifications. The HD-Full module achieved an S/N of 4.8 against a target of 4.5, while the LD-Full module recorded an S/N of 8.4, surpassing its target of 6. Both LD-Semi modules achieved S/N values of ∼12, exceeding the target of 11. These results conclusively validated the Hexaboard designs, confirming their reliability and readiness for deployment in the HGCAL detector system. Furthermore, the successful beam tests provided the final endorsement for the large-scale production of LD and HD Hexaboards, paving the way for their integration into the HGCAL detector.

Contributions to Test Systems: This thesis also contributed to the development of test systems for the characterization of Hexaboards and silicon modules. A key achievement was the design of the Trophy Board, a versatile platform supporting both LD and HD Hexaboards. Multiple variants of the Trophy Board are now widely employed at CERN and HGCAL Module Assembly Centers globally, facilitating efficient communication between Hexaboards and the Hexacontroller, a Zynq FPGA-based system. These boards integrate ADCs and level shifters to process analog status signals, ensuring compatibility and streamlined testing workflows.

Contribution to laser system development:

In parallel to Hexaboard prototyping and performance evaluations, the development of the laser-based test system for silicon module characterisation forms a cornerstone of this thesis. Designed to meet the stringent performance requirements of the HGCAL under the challenging operational conditions of the HL-LHC, this system plays a pivotal role in advancing module calibration and timing studies.

The system integrates a 1064 nm pulsed laser, an optical attenuator, and motorised XYZ stages, enabling precise charge injection and scanning across silicon module cells. Key components, including the waveform generator, hexacontroller, and laser driver, are synchronised by a 10 MHz laboratory clock source, ensuring precise timing alignment and stable operation for high-resolution measurements.

Comprehensive timing and charge characterization demonstrated the system's ability to achieve a noise term of approximately 10 ns and a constant term of 27 ps, compared to the TDR goals of 5 ns and 20 ps, respectively. Timing resolution studies across temperature variations (-20 °C, 0 °C, and 20 °C) revealed negligible dependence on temperature, validating the robustness of the system. However, it was observed that charge generation by photons in silicon exhibits temperature sensitivity, attributed to the temperature-dependent band gap variation, impacting charge collection efficiency and signal amplitude.

The deviation from TDR parameters is attributed to the following factors:

- **Non-Gaussian Signal Behavior**: At lower signal amplitudes, non-Gaussian timing distributions, influenced by electronic noise, broadened the measured data and increased the noise term.
- **Clock Jitter and Systemic Noise**: Jitter introduced by the HGCROC's Phase-Locked Loop (PLL), ranging from 15 ps to 27 ps, along with impedance mismatches and electronic noise, further impacted timing precision.
- **Real-World Testing Conditions**: Unlike idealized TDR simulations and ASIC designer tests, the experimental setup introduced environmental noise and operational variability inherent to silicon module testing.

Despite these challenges, the laser system successfully facilitated critical studies, including time-walk effects, charge injection profiles, and temperature dependencies, providing key insights into silicon module performance.

The final phase of this study incorporated the measured timing parameters into HGCAL physics simulations to assess their impact on the reconstruction of neutral hadrons (K_L^0) and photons (γ), which rely exclusively on calorimetric measurements. Single-particle gun events with energies up to 120 GeV were simulated at pseudorapidity $\eta = 2$, focusing on the influence of TOA resolution on shower efficiency and pileup mitigation. The results demonstrated that timing resolution plays a critical role in neutral hadron reconstruction efficiency. Specifically, the efficiency threshold for K_L^0 increased from 10.95 GeV (TDR baseline) to 13.03 GeV when utilising timing parameters from Channel 158 ($A = 10$ ns, $C = 30$ ps), indicating reduced detection efficiency for low-energy hadronic showers. This reduction has implications for jet energy measurements and pileup suppression strategies.

In contrast, photon reconstruction remained stable across all timing conditions, reflecting the inherently consistent nature of electromagnetic showers in the ECAL. The broader fluctuations in hadronic interactions within the HCAL resulted in greater sensitivity of neutral hadrons to timing resolution degrada-

tion. However, given that neutral hadrons constitute approximately 10-15% of total shower constituents, the overall impact on HGCAL physics performance remains marginal.

With the successful validation of silicon module performance in beam tests and the completion of precision timing characterisation, the production of readout boards has now progressed to an advanced phase. The majority of units have undergone initial testing, marking a significant milestone in the integration of HGCAL electronics. These developments ensure the system's readiness for large-scale deployment in the forthcoming experimental phase, aligning with the planned timeline for HL-LHC operations.

Future Directions

This Ph.D. research contributes significantly to the ongoing efforts to prepare the HGCAL for the HL-LHC era. The insights gained from the design optimisation, beam test characterisation, and laser-based timing studies will serve as a foundation for further advancements in detector technology. Key areas for future exploration include:

1. Large-Scale Production and Deployment: Scaling the optimised Hexaboard designs for mass production and integration into the HGCAL system.

2. Advanced Calibration Techniques: Developing refined calibration algorithms to enhance the accuracy of timing measurements and mitigate systematic uncertainties.

3. Integration with Full Detector Systems: Extending the testing and characterisation to multi-module setups, simulating full detector operation.

4. Using differential laser to measure the timing resolutio n of one channel with respect to the second pulse to avoid a common mode effect

Appendix A

List of publications

International conference papers

- **Khan, F.A.,** Noy, M., Steen, A., Monti, F., Ganjour, S., & CMS Collaboration. (2024). The development of a laser system for use in the timing performance measurements of CMS HGCAL silicon modules. *Journal of Instrumentation*, **19**(03), C03023.
- **Khan, F.A.,** CMS Collaboration, & others. (2023). Design and performance optimisation of the Hexaboards for CMS HGCAL silicon sensor readout electronics. *Journal of Instrumentation*, **18**(03), C03015.

HGCAL Publications

- **Acar, B.,** Adamov, G., Adloff, C., Afanasiev, S., Akchurin, N., Akgün, B., Alhusseini, M., Alison, J., Khan, F.A., & Noy, M. (2023). Performance of the CMS High Granularity Calorimeter prototype to charged pion beams of 20–300 GeV/c. *Journal of Instrumentation*, **18**(08), P08014.
- **Acar, B.,** Adamov, G., Adloff, C., Afanasiev, S., Akchurin, N., Akgün, B., Alhusseini, M., Alison, J., Khan, F.A., & Noy, M. (2023). Neutron irradiation and electrical characterisation of the first 8" silicon pad sensor prototypes for the CMS calorimeter endcap upgrade. *Journal of Instrumentation*, **18**(08), P08024.
- **Acar, B.,** Adamov, G., Adloff, C., Afanasiev, S., Akchurin, N., Akgün, B., Khan, F.A., Alhusseini, M., & Alison, J. (2022). Response of a CMS HGCAL silicon-pad electromagnetic calorimeter prototype to 20–300 GeV positrons. *Journal of Instrumentation*, **17**(05), P05022.
- **Acar, B.,** Adamov, G., Adloff, C., Afanasiev, S., Akchurin, N., Akgün, B., Khan, F.A., Alhusseini, M., Alison, J., & Alpana, A. (2024). Timing performance of the CMS High Granularity Calorimeter prototype. *Journal of Instrumentation*, **19**(04), P04015.
- **Aamir, M.,** Acar, B., Adamov, G., Adams, T., Adloff, C., Afanasiev, S., Agrawal, C., Agrawal, C., Ahmad, A., & Khan, F.A. (2024). Using graph neural networks to reconstruct charged pion showers in the CMS High Granularity Calorimeter. *Journal of Instrumentation*, **19**(11), P11025.

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