The CMS GEM Detector Front-end Electronics – Characterization and Implementation

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in fulfillment of the requirements for the degree of Doctor in Engineering Sciences and Technology (ULB - “Docteur en Sciences et technologies de l'ingénieur”)

Academic year 2021-2022

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CERN-THESIS-2021-246
21/12/2021

Abstract

This research work is a contribution to the CMS GEM upgrade. From 2026, the CERN Large Hadron Collider (LHC) will enter the High Luminosity phase, also known as phase-2, where the machine will almost double the number of proton collisions per second. This luminosity increase brings challenges to the LHC experiments, like CMS, particularly to their most forward detector sub-systems closer to the beamline. The higher particle rates and radiation levels challenge the detectors and their read-out electronics, the trigger, and the data acquisition systems of the experiment.

In CMS, new Triple-GEM detectors are being installed in the forward part of the muon spectrometer. A first ring, called GE1/1, has been deployed during the current LHC Long Shutdown (2019-2021), and two other rings, GE2/1 and ME0, will be installed within a couple of years. The objective of the new Triple-GEM detector sub-system is to improve the CMS's muon tracking and triggering capabilities.

This thesis is devoted to the VFAT3, a front-end chip that has been designed for the CMS GEM upgrade project. The VFAT3 is a 128 channel ASIC providing both trigger and tracking data. In CMS, the VFAT3 chip is assembled on a small (5 x 5 cm^2) PCB, called the VFAT3 hybrid. For GE1/1, 5,000 VFAT3 chips and hybrids had to be mass-produced. This mass production required a full characterization of the chip on the hybrid, including its radiation hardness and the study of the VFAT3 performance once it is integrated into the CMS GEM detectors. The objective of my work was to demonstrate the adequacy of the VFAT3 chip and VFAT3 hybrid for the CMS GEM phase-2 application and design the challenging hardware, software, and firmware tools required to reach that goal.

The thesis is structured as follows: Chapter 1 introduces the CERN, the LHC, and the CMS projects. The phase-2 upgrade of the LHC is also described, and planned muon endcap upgrades are discussed. Chapter 2 details the GEM detectors and the first CMS GEM ring, GE1/1. The GE1/1 performance parameters achieved over ten years of GEM global collaboration R&D are also presented. Chapter 3 elaborated the VFAT3 chip, its design, and architecture. The key design goals of the chip design and optimization for GEM charge are also discussed. Chapter 4 presents the functional characterization of the VFAT3. The dedicated setup is described in detail, and the VFAT3 characterization performance is discussed. The phase-2 compatibility results of the VFAT3 are demonstrated as well. Chapter 5 is then devoted to the comprehensive study of the radiation hardness of the chip. Different test facilities and test setups designed to perform the radiation characterization are discussed. VFAT3 radiation-tolerance conformance to GEM operation is presented. In Chapter 6, the performance of the VFAT3 with the first CMS GE1/1 detector prototypes is evaluated. Various compatibility chal-

lenges and their mitigation strategies are presented as well. Chapter 7 presents the production of the VFAT3 hybrid, the manufacturing issues which had to be tackled, and finally, the results and final yield of the production of 5000 pieces for GE1/1 is described. Ultimately, Chapter 8 introduces the future CMS GEM rings, GE2/1 and ME0. The impact of my GE1/1 work and its future prospects towards GE2/1 & ME0 are also discussed.

Dedication

*To **Isma,***
my Loving wife,
whose sacrificial care and help encouraged me to
pursue and complete this thesis work,
and to our four children,
Ayesha, Hania, Muhammad and Yusra,
who always provided me happiness.

Declaration

I declare that this dissertation is my original research report. It has been written by me and has not been submitted for any other professional qualification except where work which has part of joint-collaboration, publications have been included. The mentioned experimental work is mainly performed by myself or by our test team, where my involvement is substantial. The collaborative contributions have also been explicitly mentioned and acknowledged. Due references have been provided on all used literature and technical documents.

Acknowledgements

I would like to thank my supervisors Dr. Paul Aspell and Dr. Gilles De Lentdecker, for providing me the opportunity to pursue this Ph.D. work in GEM detectors and allowed me to become a part of the fantastic CERN community. Throughout this study period, they offered me full support at each step, including experimental work and thesis writing. I would like to mention how Dr. Aspell devised a comprehensive research plan for my Ph.D. work, which I followed unaltered throughout to complete my research. Dr. De Lentdecker always helped me keep focused and carefully monitored the whole creation. I remember my birthday celebration by Dr. Gilles on 22nd November 2019, when we were doing a beam test at Louvain-La-Neuve. We almost got stuck during the beam-test, despite that Dr. De Lentdecker surprised me with my birthday celebration, which provided me courage and strength to conclude the test with an acceptable outcome. It was an unforgettable and unique birthday celebration away from our homes in the Cyclotron facility cafeteria.

I would also like to thank my supervisor Prof. Frédéric Robert, who always pushed me to adopt scientific writing methodologies. A special thanks to my friend Jérôme Alozy for always helping me during my experiments and providing me endless support with equipment, tools, components. He saved a lot of our project time and made my stay in the lab fruitful. Indeed, I will miss his company the most of all things at CERN.

I would also like to thank my colleagues Mohsin and Ali for providing valuable technical support during this research work during the electronics developments phase.

I would like a special thanks to GEM project manager Archana Sharma and Deputy director Optics laboratory Farooq Ahmed, who believed in me and recommended me for this Ph.D. work. Finally, a special thanks to my wife for endless support throughout this writing endeavor.

Author's Contributions

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A couple of papers are still in print and not yet published.

Contents

Chapter 1

Introduction

1.1 Introduction to Particle Physics

Humanity has always been trying to understand its origin and the creation of the universe. The early explorers began to observe the stars and planets for navigation, which also helped them understand planetary motion. This initial understanding of outer space raised many more questions in their minds. How is the universe created? What is the nature of the underlying forces? What is the source of burning stars? Over the ages, scientists have done fundamental research to solve these puzzles. These efforts pushed our collective knowledge to understand the laws of nature better. Dark matter and beyond the Standard Model (BSM) are now central research topics for today's physicists.

Scientists are now in a better position to answer some of the fundamental questions reliably. However, as we understand the universe's laws; many more new questions arise in our minds. What is the origin of the underlying forces, and are there only three spatial dimensions in the universe, or do parallel universes exist? Why did all the antimatter created in the Big Bang disappear, leaving the universe made of matter? What is the origin of mass? These are some of the questions that current scientists are trying to answer with theories and experiments.

With the advent of modern electronic instrumentation and powerful computers, many large experiments, such as enormous telescopes, satellites and particle colliders, could be built worldwide. These very complex devices are helping our contemporary scientists to predict and validate their hypotheses with a faster turnover than in the past. Today's scientists are in some sense luckier as they have more chances to witness the confirmation of their theory during their own lives. One such recent example is the discovery of the Higgs boson, an elementary particle predicted by Peter Higgs in 1964 at CERN. The discovery of this particle was announced on the 4th of July 2012, exactly at CERN, after 48 years of intense research.

1.2 Introduction to CERN

After World War II, European science was not best-in-class, and many renowned scientists had left Europe. Some visionary scientists thought of creating a joint European atomic physics laboratory to recover scientific research in Europe. The main objectives were to unite European scientists and share the developing costs of nuclear physics facilities. French physicist Louis de Broglie and his contemporary scientists from Italy and Denmark initiated the first official proposal to create a European laboratory at the European Cultural Conference in Lausanne on December 9, 1949. In 1953 a meeting was held in Paris, under UNESCO's auspices, where 11 nations signed an agreement. Thus a provisional council was established, and the Conseil Européen pour la Recherche Nucléaire (CERN) was born.

The primary aim of CERN was **'What is the universe made of?'**. Its Charter was to build advanced particle accelerators and detectors to understand the nature of matter and the structure of the universe, to perform world-class particle physics research and to provide a common platform where scientists from all over Europe could freely collaborate. Geneva was chosen because of its central location in Europe and a very well-established reputation as an international city. So in 1954, in the fields around the village called Meyrin, just outside the outskirts of Geneva, work was started.

CERN has grown over the decades, building a series of particle accelerators to reveal the nucleus' structure. Each new accelerator was more energetic than the previous one and, in the process, providing a deeper understanding of the fundamental nature of matter. Figure 1.1 shows the CERN accelerator complex as of today. The first accelerator was the synchro-cyclotron (SC), which was commissioned in 1957. It supplied 600 MeV energy beams for particle and nuclear physics experiments. Then came the Proton Synchrotron (PS) in 1959, which primarily accelerates the protons provided by the Booster (PSB) or the heavy ions coming from the Low Energy Ion Ring (LEIR). It achieved an energy of 25 GeV with a 628 meters circumference ring. As CERN's first synchrotron, the PS was a vital component of the CERN accelerator chain. However, since new energetic accelerators were built after the 1970s, it has then mainly been used as injector of new powerful machines. Then came the Super Proton Synchrotron (SPS) in 1976 with a circular ring of 7 km with an energy of 450 GeV. It has been a mainstay of the CERN particle physics program and contributed to studying internal structure of the proton in more detail. It also opened a gateway for physicists to study antimatter and exotic forms of matter. In 1981, the SPS was transformed into a proton-antiproton collider. It helped to discover the "W" and "Z" particles in 1983. In 1984, Carlo Rubbia and Simon van der Meer, scientists behind the discovery, received the Nobel Prize in physics. This achievement was so significant that it helped to secure the decision to build next large accelerator, the Large Electron-Positron Collider (LEP) at CERN.

The main objective of the LEP was to mass-produce "W" and "Z" bosons to perform their detailed characterization. With its 27 km circumference, LEP was the largest electron-positron collider ever built. LEP was commissioned in 1989 and reached the maximum energy of 209 GeV in 2000. During 11 years of operation, LEP experiments helped physicists to understand the electroweak interaction in

more detail. On November 2, 2000, LEP was shut down to construct the current Large Hadron Collider (LHC) in the same tunnel. Presently, LHC is the world's largest and most powerful particle collider. It was commissioned in 2008 and is the last link in the CERN accelerator complex till date. It achieved a nominal proton collision energy of 13 TeV in 2015. LHC was instrumental in providing evidence for the Higgs boson and validated a well-known Standard Model (SM) of particle physics. This model explains the fundamental components of the matter. Nowadays, CERN encompasses a vast area predominantly involving two main sites, the Meyrin site in Switzerland and the Prevessin site in France, and of course, the LHC and the four main detectors on the main 27 km ring.

These days, CERN is much more than an European organization. What started with 12 member states from Europe has grown to 23 member states, seven associate member states, including India and Pakistan, with many more observer status and research agreements. There are over 600 institutes and universities around the globe that use CERN's facilities. All these traits make CERN a genuinely unique and international organization. More than 18000 people worldwide work together to achieve a common goal. These include physicists, engineers, mathematicians, computer scientists, and many more, plus, of course, the many support personnel as well. They represent over a hundred and ten nationalities. Although, the goal of CERN was to better understand nature, out of it, many applications have influenced society. The World Wide Web (WWW) was developed here, and so was the capacitive touch of the electronic screens that we utilize. PET scans and other medical technologies to diagnose and treat cancer directly applied the technology designed at CERN. Moreover, because CERN has to build many new instruments from scratch for its innovative work, the technologies developed here end up being used in other diverse industries such as Aeronautics, Manufacturing, Computing, and Medicine, to name a few. In short, started as a place to do cutting-edge research in Europe, CERN has now become global cooperation that enhanced our understanding of nature and positively impacted every individual on this planet in some way or another.

1.3 Introduction to LHC

The Large Hadron Collider (LHC) is the world's largest particle collider, accelerating the protons and heavy ions near the speed of light. These particles are then smashed together at four different points where large detectors observe the collision debris. The LHC consists of a 27 km ring of superconducting magnets lying in a tunnel under an average depth of 100 m below the Jura mountains.

The acceleration of protons in the LHC starts with a small bottle filled with compressed hydrogen. A controlled number of hydrogen atoms are injected into a source block of a linear accelerator called LINAC-2. A strong electric field is then applied to strip the electrons from hydrogen atoms to make proton packets. These protons are then accelerated and leave the LINAC-2 at one-third of the speed of light. Then the protons enter the first circular accelerator, the PSB. Next is stage-2, called a booster stage. Each proton packet is divided up into four bunches, one for each of the four booster rings. From this stage, linear acceleration is impractical, and here protons are boosted in circular rings. A pulsed

electric field is applied to accelerate the proton bunches at regular intervals.

The booster stage accelerates the protons up to 91.6 % of the speed of light. The high-speed proton bunches then recombine and enter into the Proton Synchrotron (PS) (see Figure 1.1).

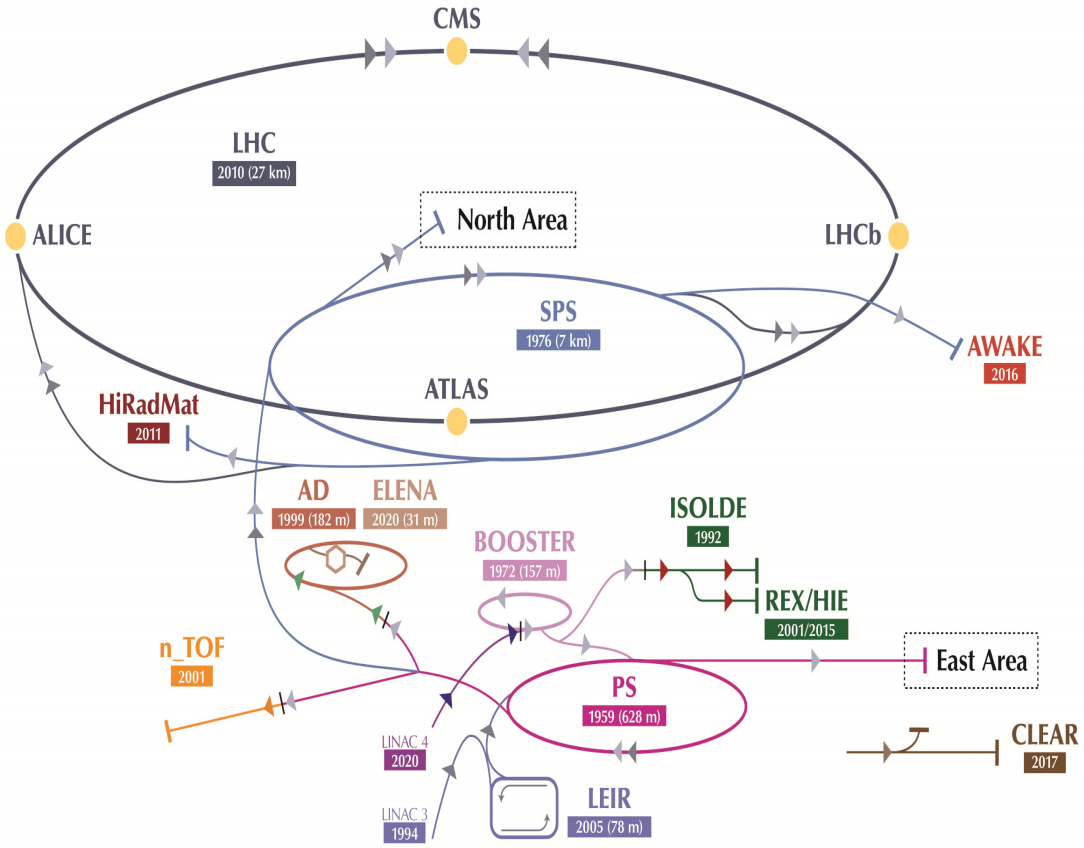


Figure 1.1: CERN accelerator complex

The PS is 628 m in circumference, and bunches circulate here for just 1.2 seconds, reaching over 99.9 % of the velocity of light. The transition point is reached at such a high velocity, and the electric field energy cannot further increase protons velocity. Instead, it is converted to increase the apparent mass of the protons. In the PS stage, the protons reach up to the energy of 25 GeV. In short, each proton is now 25 times heavier as compared to its rest mass. The bunches of protons are now injected into 7-km ring of the SPS. Here proton bunches are accelerated up to 450 GeV of energy and ready to be launched in the LHC orbit. LHC consists of two vacuum rings containing two proton beams orbiting in opposite directions. There are sophisticated kicker circuits that synchronize the incoming bunches with the already circulating bunches. The counter-rotating beams meet only in the four detectors, where these are forced to collide with double energy compared to the individual beam energy. What comes out of these four collision points is recorded by many layers of sensitive detectors. It is almost half an hour cycle in which SPS injects 2808 proton bunches in the LHC. During this time, LHC provides a maximum of 7 TeV of energy to the relativistic protons such that each proton revolves 11,000 times per second around the 27 km circular ring. At this stage, each proton has a mass 7000 times heavier than its rest mass. A large current of 12 000 A flows through the superconducting electromagnets to keep such

high-speed protons in the circulating orbits.

Finally, steering magnets force the proton beams for the collision to occur. The total collision energy of two colliding protons is 14 TeV and recreates similar conditions similar to few microseconds after the big-bang. There are four main detectors at the LHC, each with its unique purpose and use. These are called ALICE (A Large Ion Collider Experiment), ATLAS (A Toroidal LHC ApparatuS), CMS (Compact Muon Solenoid), and LHCb (Large Hadron Collider beauty). ATLAS and CMS are general-purpose particle detectors and were involved in discovering the Higgs boson. The other two are specialized detectors. ALICE is dedicated to the physics of heavy ions and strongly interacting matter at extreme energy densities, where a quark-gluon plasma phase forms. The LHCb experiment is dedicated to studying the slight differences between matter and antimatter by exploring a type of particle called the "beauty quark", or "b quark".

1.3.1 Performance parameters of LHC

The two most important parameters for LHC and other accelerators are beam energy and luminosity. The more energetic and intense is the beam of protons, the more powerful collisions are expected. In the LHC, not all of the protons collide with each other to produce exciting events. The luminosity measures how many particles are colliding in a particle accelerator at a given time. So in an accelerator, the luminosity is slightly more than just a simple collision rate. For the collision in the accelerator, two opposite beams are squeezed and forced to cross each other in a particular small area. So it depends on how well we can squeeze the two beams to precisely collide with each other. The particle physics interactions are not a definite phenomenon, and each event has a likelihood of occurrence, referred to by cross-section. The cross-section measures the probability that an event occurs. It is measured in barns (1 barn = 10^{-24}cm^2). There are some possible scenarios during beam interactions: the protons can miss each other or produce head-on collisions, producing any of a range of new particles. Each of these processes has an associated cross-section. The cross-section of the Higgs production (~40 pb), for example, is microscopic at the scale of the total LHC proton-proton cross-section (in nanobarns), which means that the Higgs particles will be produced very rarely. A possible beam collision is illustrated in Figure1.2.

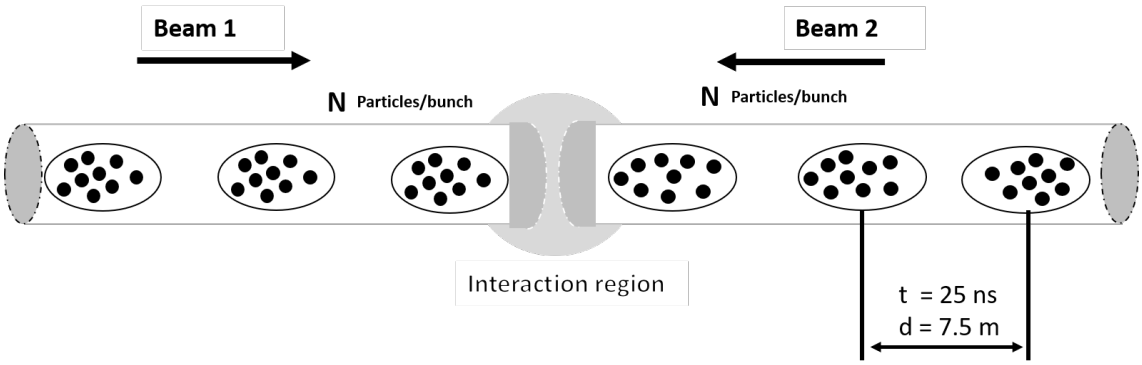


Figure 1.2: LHC bunched beam collision

To increase the likelihood of Higgs production in a given time, we need more

collisions, which will increase the likelihood to produce Higgs events. Upon multiplying instantaneous luminosity of the beam with the cross-section for any process, we get the rate of that process to happen. If we multiply the luminosity by the sum of the cross-sections for all possible processes, we get the total collisions. The luminosity can be defined as the ratio of the number of events detected (N) at a certain time (t) to the interaction cross-section. Mathematically, we can write:

$$\mathcal{L} = \frac{1}{\sigma} \cdot \frac{dN}{dt} \tag{1.1}$$

The instantaneous luminosity is measured in $cm^{-2}s^{-1}$. The simplified instantaneous luminosity of two circular colliding beams with bunches shown in Figure 1.2 is represented as:

$$\mathcal{L} = \frac{n_b N_p^2 f}{4\pi\sigma_x\sigma_y} F \tag{1.2}$$

Where n_b is the number of colliding bunch pairs, N_p is the bunch population, f is the revolution (11.25 kHz) frequency, F is the geometric loss factor due to the crossing angle, and $4\pi\sigma_x\sigma_y$ represent the cross-sectional area in x and y directions.

The nominal designed values of LHC beam parameters are shown in Table 1.1. The rightmost column describes parameters for a high luminosity upgrade of LHC, known as HL-LHC, which will be discussed in the next section.

Parameter	LHC nominal	HL-LHC
$N_p[10^{11}]$	1.15	2.2
$n_b[10^{11}]$	2808	2808
$\beta^*[m]$	0.55	0.15
$\epsilon_n[\mu m]$	3.75	2.5
Bunch separation $[ns]$	25	25
Crossing angle $[\mu rad]$	300	590
Pile-up	40 - 60	140 - 200
$\mathcal{L}_{peak}[cm^{-2} \cdot s^{-1}]$	1 - 2×10^{34}	5 - 7.5 $\times$ 10^{34}

Table 1.1: Table showing a comparison between LHC and HL-LHC collision parameters.

Using parameters from Table 1.1, the peak luminosity obtained for LHC Run-2 is $10^{34}cm^{-2}s^{-1}$. We have seen that luminosity is not merely the collision rate, instead it is a measures of how many particles have been squeezed through a given space and time, which might not all collide. Hence, larger the number of the particles into a given squeezed space, the more the chances are that they will collide. Since 2016, the LHC is colliding protons approximately at a rate of 1 billion times per second.

1.3.2 LHC upgrades

The first successful LHC physics beams were produced on November 20, 2009 since LHC continued to produce collisions with a gradual increase of energy until 2013. This period is now called LHC Run-1 (2009-2013). LHC Run-1 produced pp-collisions at a center-of-mass energy up to 8 TeV. The maximum instantaneous luminosity of 7 x 10^{33} $cm^{-2}s^{-1}$ was achieved, and the LHC delivered 30 fb^{-1} of integrated luminosity to the experiments. A detailed updated LHC plan is shown in Figure 1.3.

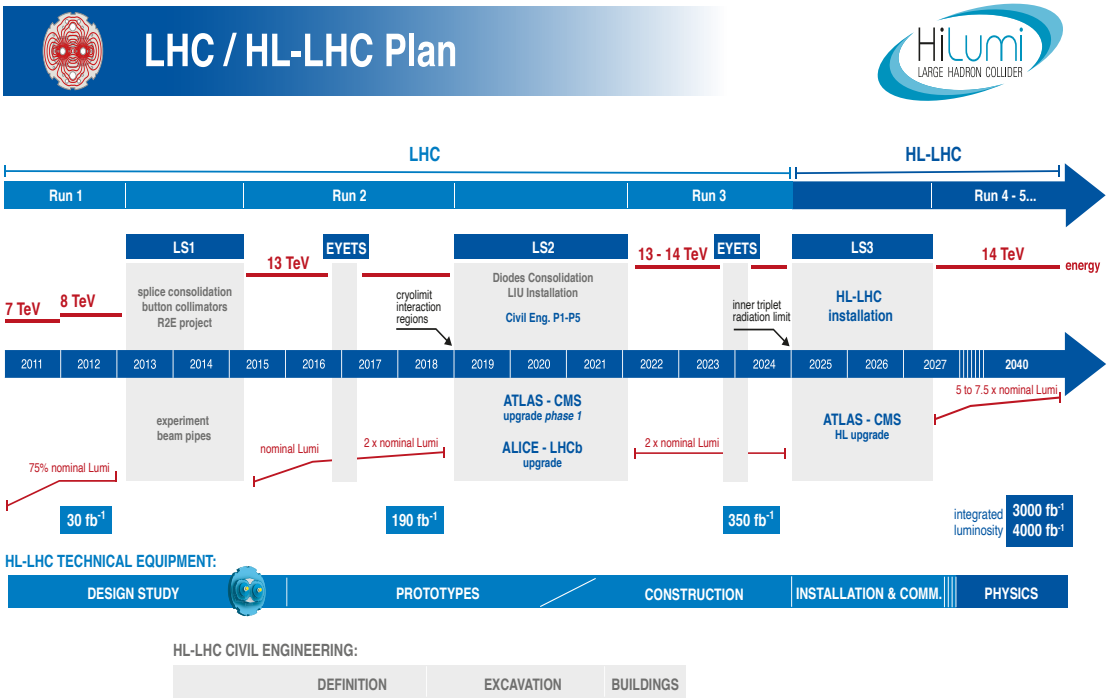


Figure 1.3: LHC upgrades detailed schedule including HL-LHC [1].

On February 13, 2013, after a successful run, the LHC was shut down for two years to accomplish necessary upgrades and replacements. This period is called LS-1 (Long Shutdown-1)(2013 - 2015). The primary goal of LS-1 was to enable the accelerator for high energy collisions at 14 TeV, improving its experiment detection capabilities and replacing the components and cabling damaged by the high-energy collisions from its first run.

In 2015, the accelerator began its physics program again for Run-2 (2015 - 2018), with almost twice the previous energy. The proton beams collided at a center-of-mass energy up to 13 TeV. The targeted instantaneous luminosity of 1 x 10^{34} $cm^{-2}s^{-1}$ was achieved and surpassed by a factor of two at the end of Run-2. Figure 1.4 shows the integrated luminosity delivered by the LHC from 2011 to 2018.

The total integrated luminosity delivered by the LHC to ATLAS and CMS amounts to ~160 fb^{-1}, and ~190 fb^{-1} for Run-1 and since the start of the LHC, respectively.

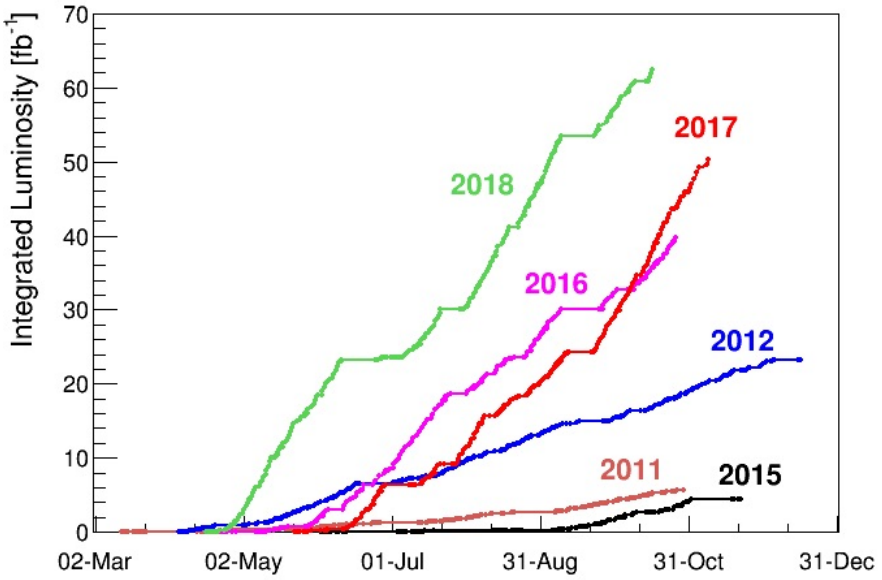


Figure 1.4: LHC integrated luminosity chart for Run-1 & Run-2

Physicists believe that to sustain and extend the discovery potential of the LHC, major upgrades are required to increase its instantaneous luminosity by a factor of 5 beyond the original design value of 10^{34}cm^{-2}s^{-1} [2]. This major upgrade is called High Luminosity LHC (HL-LHC). The integrated luminosity for HL-LHC is also expected to increase by a factor 10 to achieve 3000 fb^{-1} as summarized in Table 1.2.

Parameter	Design	Run-1	Run-2	Run-3	HL-LHC
Energy [TeV]	14	7/8	13	14	14
Bunch spacing [ns]	25	50	25	25	25
Bunch Intensity [10^{11} ppb]	1.15	1.6	1.2	up to 1.8	2.2
Number of bunches	2800	1400	2500	2800	2800
Emittance [μm]	3.5	2.2	2.2	2.5	2.5
Crossing angle [μrad]	285	-	300 $\rightarrow$ 260	300 $\rightarrow$ 260	TBD
Peak luminosity [10^{34} cm^{-2}s^{-1}]	1.0	0.8	2.0	2.0	5.0
Integrated luminosity [fb^{-1}]	40	30	160	300	3000
Peak pileup	25	45	60	55	150

Table 1.2: Key LHC parameters, showing the design values used during past Run-1 and Run-2. The estimated parameters for Run-3 and the HL-LHC are also shown [3]. The integrated luminosity shown is for the CMS experiment.

The high luminosity data taking period of LHC starting from 2027 is called 'Phase-2' and is expected to last until 2038. The current 'Phase-1' era will be concluded in the year 2024. The collision energy will be upgraded from 13 to 14 TeV and integrted luminosity for CMS and ATLAS will increase from 300 fb^{-1} to 3000 fb^{-1} in the next two decades.

1.4 The CMS Experiment

The CMS (Compact Muon Solenoid) experiment is one of the two general-purpose detectors to study particle collisions at LHC. The main goals of the CMS include validation of the Standard Model of particle physics, the discovery of the Higgs Boson and its characterization, and exploring the TeV scale physics to look for the signs beyond the Standard Model such as extra dimensions or supersymmetry.

The CMS experiment has an extensive scientific collaboration around the globe, engaging more than 5000 scientists and engineers from over 200 institutes in 50 countries. Since the beginning of the project, collaboration contributed to the design and construction of the detector, and components were brought to CERN for final assembly. The detector data is shared and stored with several computing centers through the LHC Computing Grid, which is accessible from all collaborative institutes for physics analysis.

1.5 CMS Physics performance and discovery of Higgs boson

From the physics point of view, both CMS and ATLAS made several breakthrough measurements during Run-1. For the first time SM processes were studied at $\sqrt{s} = 7$ and 8 TeV. All measurements confirmed, again with high precision, many SM predictions from past experiments carried out at much lower energies. The climax was reached on July 4th 2012 when CMS and ATLAS jointly announced the discovery of a new particle of a mass of 125 GeV/c^2, compatible with the Higgs boson, the missing piece of the SM puzzle [4, 5].

During 2015 - 2018, LHC Run-2 produced pp-collisions at center-of-mass energy up to 13 TeV. The maximum instantaneous luminosity of 1×10^{34} cm^{-2}s^{-1} was achieved and the LHC delivered 100 fb^{-1} integrated luminosity to the CMS experiment. A huge increase in cross-sections for different popular processes was expected, with an energy increase from 8 to 13 TeV. Figure 1.5 shows that this ratio ranges from 1.1 for minimum bias events to 6500 for Quantum Black Holes (QBH) processes [6].

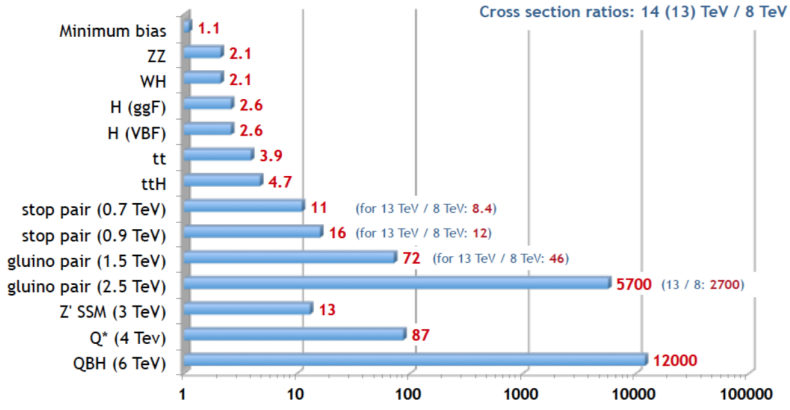


Figure 1.5: Cross-section ratios increase for selected processes after LHC Run-2

1.6 CMS construction and sub-detectors

The CMS experimental site is located in the French commune of Cessy, about 10 km away from CERN's main facility in Geneva. Excavation of the CMS underground cavern started in 1999. The CMS detector is a highly modular design and was assembled on the surface, with parts sent to Cessy from all over the world. Each of the constructed CMS slices was lowered through the shaft into the 100m deep experimental cavern and assembled on its floor. The most massive slice, weighing 2000 tonnes, took around ten hours to be lowered in a very delicate operation. A perspective view of the CMS detector is shown in Figure 1.6.

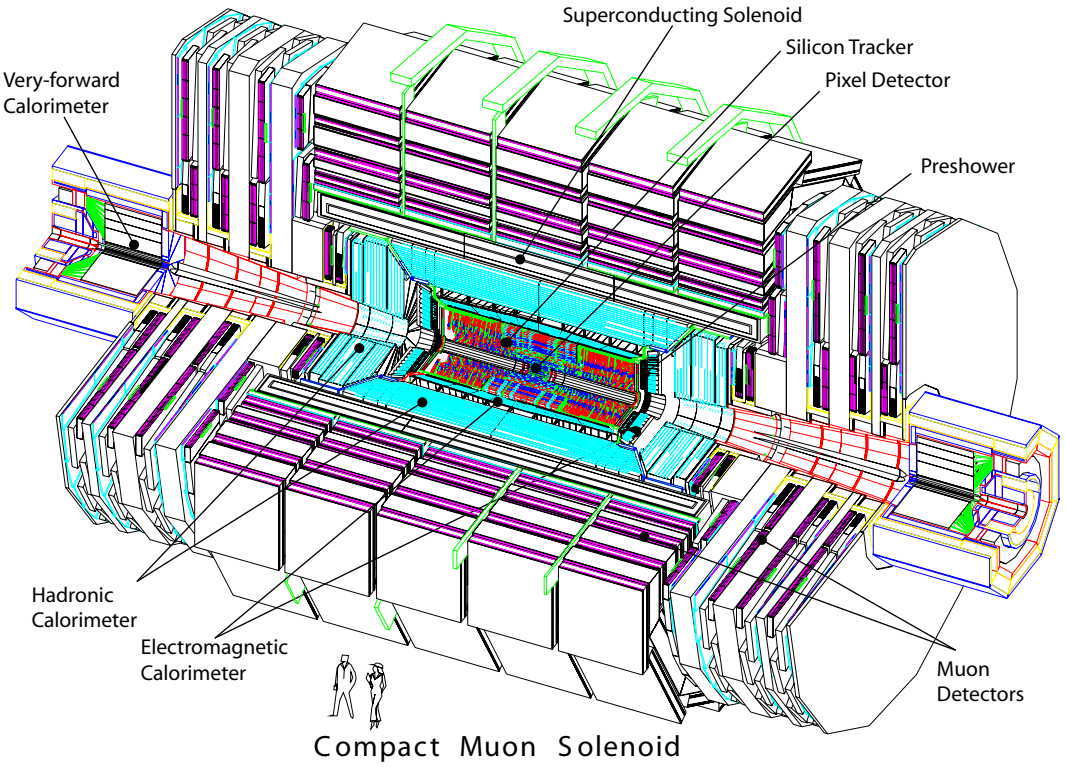


Figure 1.6: A perspective view of the CMS detector.

CMS itself is 15 meters high and 21 meters long and is relatively compact for all the detector systems it contains. One of the CMS detector main goals is to precisely measure the muon momentum up to the TeV range. Thus, bending muons at such high energies requires a powerful superconducting electromagnet, producing 4T of the magnetic field. This magnetic field returns through a surrounding return yoke, 22 m long and 14 m in diameter. The central part of the yoke, commonly called 'barrel', is arranged into 12-sided cylindrical sectors closed at each end by the endcaps. The sub wheels of the barrel yoke are called YB0, YB$\pm$1, and YB$\pm$2. Each endcap yoke is also divided into three disks, namely YE$\pm$1, YE$\pm$2, and YE$\pm$3. The detector weighs 14,000 tons and has around 75 million individual channels to detect and identify different particles. CMS comprises several layers, like a cylindrical onion: the innermost sub-detector is the Silicon Tracker, which registers charged particles' trajectories. The next layers are the Electromagnetic and Hadron Calorimeters, which collectively measure the ener-

gies of electrons, photons, and hadrons. Then comes the solenoid magnet itself and finally the muon detectors that make up the outer layers [7]. Three different kinds of muon detectors are used in the original CMS experiment:

- Drift tubes (DT): used in the barrel region
- Cathode Strip chambers (CSC): deployed in the endcaps and,
- Resistive Plate Chambers (RPC): both in barrel and endcaps.

1.6.1 Drift tubes

A CMS Drift Tube consists of a 4 cm small tube containing a 2.4 m long stretched wire within a gas volume. When a charged particle crosses the tube volume, it produces ionization. The ionization electrons drift towards the anode wire, multiplying in an avalanche because of the high (several tens of kV/cm) electric field. The moving charge (mainly the positive ions) induces a signal on the wire, amplified by the readout electronics. In a DT cell, the particle position is given by the drift time of the primary ionization to the anode wire. Combining the information from different DT layers, a DT achieves a 100 µm spatial resolution. Figure 1.7 shows Drift Tube chambers in the CMS.

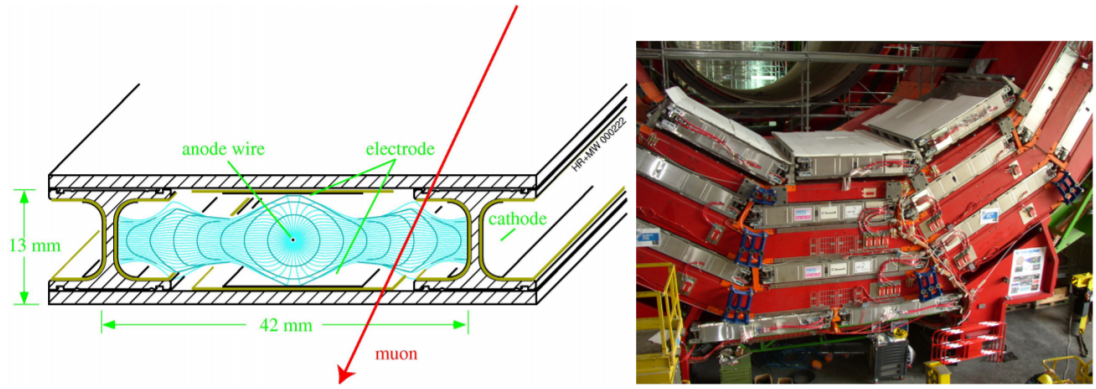


Figure 1.7: Left: Single DT cell. Right: DT chambers (aluminum) sandwiched between steel plates of the yoke (red), during installation

The drift tubes have been selected as tracking detectors in the barrel region because of the low particle rate (a few Hz/cm^2) and low magnetic field. Multiple drift tube structures are assembled in a single rigid structure to protect exposed wires and provide partial decoupling of adjacent cells to avoid cross-talk from electromagnetic debris along with the muon itself. The CMS DT system comprises 250 chambers mounted onto the muon barrel (MB) stations, interleaved with the steel yoke plates, as shown on the right of Figure 1.7, for a total of 172,000 sensitive wires. The spatial resolution of a DT layer is 1 mrad on the particle direction with a 5 ns time resolution.

1.6.2 Cathode strip chambers

The muon endcap region has an uneven magnetic field and high particle rates. Because of their high spatial and temporal resolution, cathode strip chambers

(CSCs) are selected for use in this region as a primary muon trigger source. CSCs showed spatial resolutions from 47 µm to 243 µm and timing resolution up to 5 ns per layer [8]. The CSC subdetectors have a trapezoidal shape, and a total of 468 detectors are installed in 8 rings of the CMS muon endcaps - 4 on each side. The outer detectors are considerably larger as compared to inner ring detectors. Every CSC chamber consists of six layers of detectors, each with anode wires stretched between two planar cathodes. One of the cathodes is continuous, while the other is segmented in strips for spatial measurements. A partially exposed view of a CSC detector is shown on the left side of Figure 1.8.

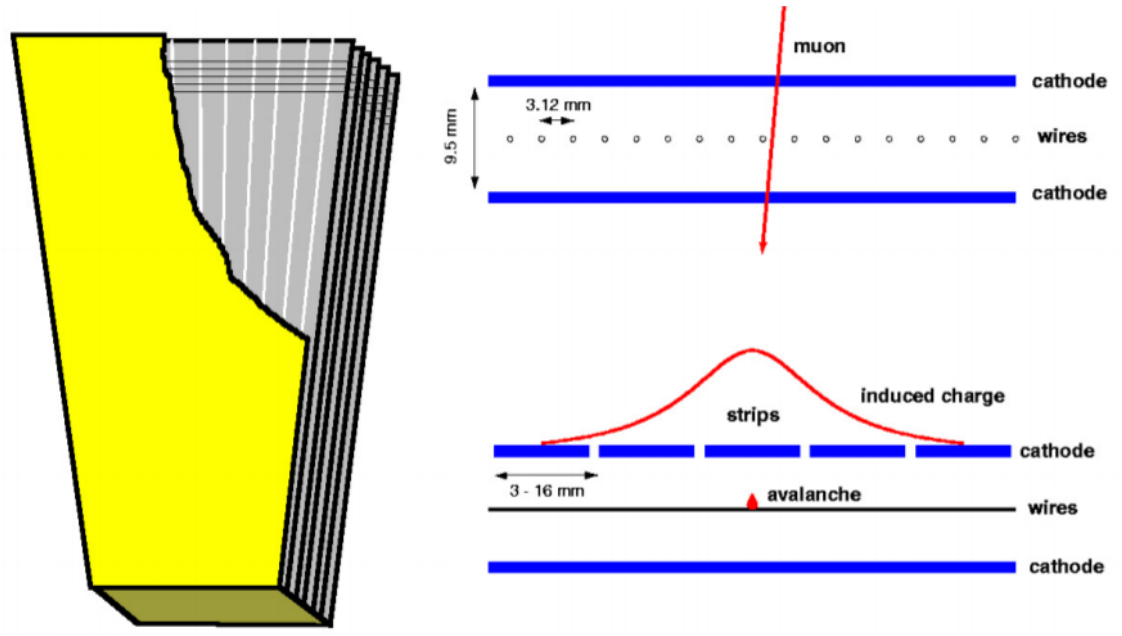


Figure 1.8: Left: Geometry of CSCs in CMS. Right: Working principle and signal formation

The whole structure is filled with a gas, and when muon passes through the detector, ionization of gas occurs, which ends up in the avalanche of electrons. Positive ions are detected by copper cathodes, while fast electrons move towards anode wires to produce negative charge pulses. The 2-D spatial tracks of particles are obtained due to the orthogonal placement of wire and cathodes, as illustrated in Figure 1.8 (right).

1.6.3 Resistive plate chambers

RPCs are used for their excellent time resolution, better than 3 ns. A CMS RPC consists of 2 gas-filled gaps as shown in Figure 1.9, and is made of four bakelite parallel plates with a resistivity of 10^{10} - 10^{11} $\Omega \cdot cm$. The outer plates are coated with conductive graphite paint to make high voltage and ground terminals, and an electric field of 5 kV/mm is applied between them. At the center of the structure, the Aluminium strips are used for charge readout.

There are 480 RPC chambers in the barrel covering an area of 2285 m^2 while 432 chambers in the endcap region cover 668 m^2.

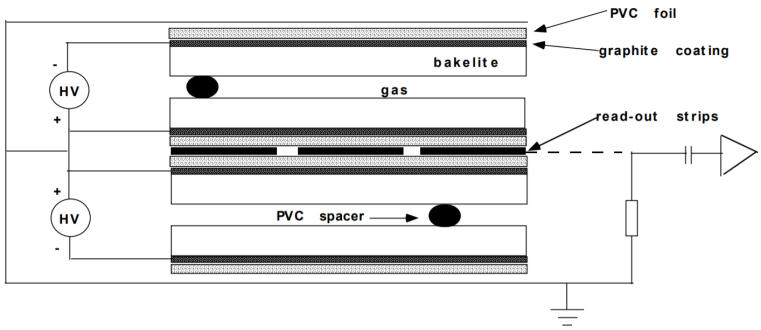


Figure 1.9: Schematic view of the double gap CMS RPC

1.7 Limitations of existing muon subsystem

The aging of gaseous detectors and their associated electronics in the radiation environment is always a concern. After years of detector operation, the charge deposition on anode wires can significantly decrease the gas gain and particle detection efficiency. To compensate for the reduced hit efficiency, one could slightly increase the gas pressure or the high voltage to boost the gain, which can sometimes lead to detector breakdown in high particle rates.

The detector electronics can be damaged as well by radiation effects during operation in the radiation environment. Radiation damage of metal oxide semiconductor (MOS) transistors can happen due to permanent or temporary accumulation of charge in the substrate channels, which can vary transistors' characteristics leading to device malfunction. In some cases, permanent damage to the detector electronics is also reported.

The interaction of radiation with the detector components is a complex phenomenon. Detector deterioration is generally associated with the accumulated charge in gas volume and measures in 'Coulomb/cm' for wires and 'Coulomb/cm^2' for surfaces. The aging of electronics is due to the hadron fluence or flux and is associated with total ionizing dose (TID), usually measured in the units of rad. The aging effects mostly become severe in the radiation environment and need to be accounted for as frequent data-taking disruptions which can also disrupt CMS data-taking operations.

The CMS muon system was designed to be highly redundant, using DT, CSC, and RPC for precise Level-1 triggering, and most of the barrel and endcaps area is covered by two different sub-detectors. The endcap region with $|\eta| > 1.6$ is only covered with CSC, and RPC were not employed in this region due to the limitations of RPCs to cope with the high (> 1 kHz/cm^2) background rates in this area [9]. Substantial efficiency losses in muon trigger are also expected for muons with $P_T < 25$ GeV/c after LS2 operation for almost 50 % of the endcap coverage [10].

A reliable triggering on muons in the very forward regions is highly desired for the HL-LHC. Moreover, the redundancy of the muon system must be improved to maintain an acceptable muon track reconstruction, keeping the rejection of wrongly identified tracks low at the Level-1 trigger. The Phase-2 muon detector upgrade must achieve an effective muon system in the forward region by adding new forward muon detectors, GE1/1, GE2/1, and ME0 GEMs (Gaseous

Electron Multipliers), which will be described in full details in Chapter 2.

1.8 CMS phase-2 DAQ & trigger system

CMS has devised a standard Data Acquisition (DAQ) and trigger framework to simplify data path and time decoupling between the synchronous detector readout and data reduction blocks. It also allows the asynchronous selection of interesting events and their permanent storage for offline analysis. Figure 1.10 shows a block diagram of the CMS phase-2 DAQ system.

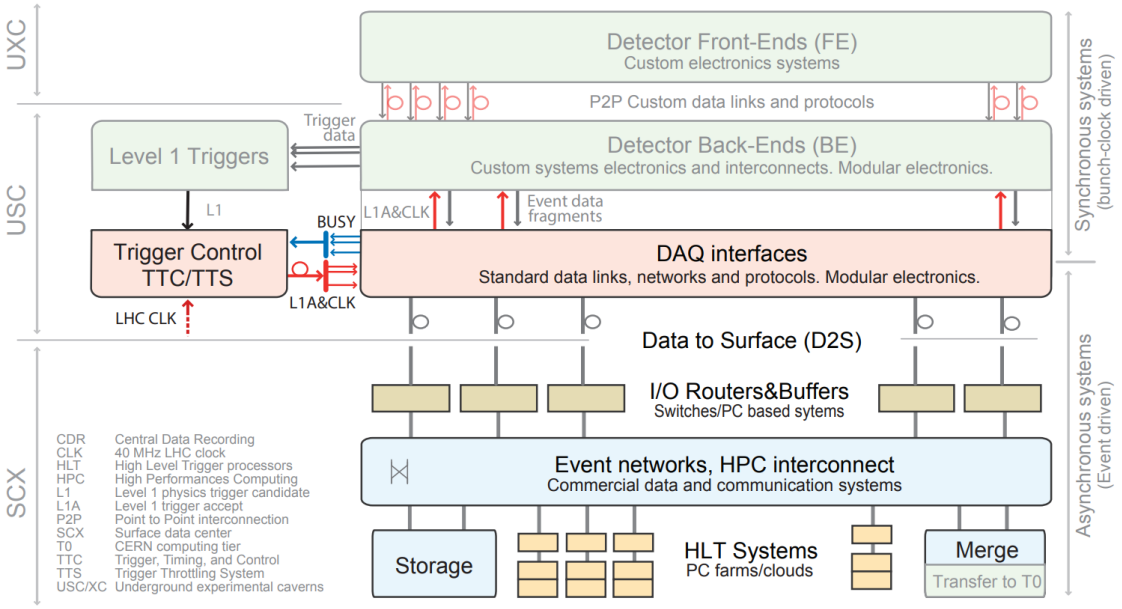


Figure 1.10: Conceptual block diagram of the overall CMS phase-2 DAQ and trigger system

The communication between sub-detector electronics and the central DAQ system is implemented through the DTH (DAQ and Timing hub) board. This DTH is consisted of hardware and software stacks that allow back-end electronics to control timing and control functions and uses SLINK Rocket links to read data from back-end systems [11].

The detector front-end (FE) and back-end (BE) use bidirectional optical links. The uplinks provide digitized detector data from FE to the BE electronics. The BE electronics further pre-process the data and re-routes the trigger data to the hardware trigger processors and the full tracking data to the DAQ system. It is essential to discuss that CMS trigger and DAQ hardware use a two-level trigger system and continue using it after the phase-2 upgrade. The Level-1 trigger uses an asynchronous hardware-based system consisting of custom electronics boards, generally with FPGAs. The level-2 trigger system uses software to select interesting events called high-level trigger (HLT). This HLT handles asynchronous data and algorithms run on standard computing processors. The synchronous part of the DAQ system provides a clock, trigger-accept, and fast control signals to the BE electronics. The synchronous part's primary goal is to guarantee the collection of all event data selected by the hardware trigger and minimize the effective dead

time between them. The synchronous part deals with the time scales of nano-seconds to micro-seconds. The maximum Phase-2 allowed latency is 12.5 µs. The event building process then uses a high-performance Event Network to interconnect I/O processors that assemble the individually accepted events in single computer memory. These constructed events remain on single computers until HLT processors pick them up for further analyses. The HLT processing timescale is of the order of 1 second, and the acceptable latency is in the range of 1-2 minutes. Next, accepted stored events stay on these computers until an attached distributed network storage system pick and assemble the events into larger dataset files for efficient long-term storage. Finally, large dataset files are moved to the central computing resources (tier0) over long-distance links. This process takes few days after the actual data taken was processed. The more intricate details of DAQ and its upgrades can be found in Phase-2 upgrade of CMS DAQ Interim TDR [12] for interested users.

1.9 Summary

This chapter introduced the research trends of particle physics in the world's renowned particle physics research laboratory, CERN. CERN has been designing and operating the world's largest particle physics accelerators since 1953. Several well-known discoveries have been made at CERN, such as the recent discovery of the Higgs boson. CERN is continuously working on enhancing the capabilities of its accelerator machines to operate them at higher energies to made more powerful collisions. During Run-2 LHC surpassed its nominal luminosity of 1×10^{34} $cm^{-2}s^{-1}$ and achieved twice of the nominal value. Currently, LHC is undergoing phase-2 upgrades, and a 5 times luminosity increase is expected, which would directly impact the performance of the current redundancy performance of the CMS muon endcap. The conventional RPCs are not good to cope with such high trigger rates, and there is a need for new detector technology good at trigger and tracking, i.e., GEMs, which are the subject of the next chapter. The GEMs will use the common CMS framework for trigger and DAQ data transmission.

Chapter 2

GE1/1 GEM detector system

2.1 Introduction

Gas Electron Multiplier (GEM) detector is a new member of the muon detector system in the CMS. The GEMs will enhance the existing muon detection and momentum measurement capability of the system. The existing muon endcap consists of two types of muon detectors, the CSC and the RPC, which demonstrated good performance during LHC Run-1 and Run-2. An upgrade is required in the existing system to cope with the increased particle rate expected during the HL-LHC. Three new GEM stations will cover the $1.5 < |\eta| < 2.8$. The installation and commissioning of the first GEM stations, GE1/1, has been done during LS2 (2018-2021). The two others, GE2/1 and ME0, will be installed in a couple of years. This chapter introduces the working principle of gas electron multipliers and their construction, mainly focusing on describing the GE1/1 GEM detector key parameters. The GE1/1 parameters have been assessed using various prototype generations by the different team members of GEM collaboration around the globe. A total of 10 GEM detector generations have been prototyped since 2010, each new generation with significant improvements over the previous detector. The critical parameters discussed include detector gain, detection efficiency, timing resolution, and discharge probability. These parameters have a direct influence on CMS GEM phase-2 operation. Finally, the GE1/1 electronics is described, mentioning both 'On-detector and 'Off-detector' electronics parts.

2.2 Introduction to Gaseous detectors

The detection of charged particles with gas-filled detector technology can be traced back to the early studies of the atomic structures by Ernest Rutherford [13]. He detected natural radioactivity trails through ionization in a gas enclosure. In 1908, together with Geiger, they instrumented a 'proportional counter' which successfully amplified weak primary ionizing signal (particles). This device consisted of a gas-filled cylindrical cathode enclosing a thin wire called the anode. An electron trail released from gas atoms by the collision of ionizing particles drifted towards the anode on applying a sufficient potential. These electrons produced further ionizing collisions and produced electron-ion avalanche near the anode. Thus, they obtained a detectable signal proportional to the primary charge. Pro-

portional counters of various sizes were successfully used for decades to detect ionization radiation. Gieger-Muller counters are still widely used for radiation monitoring.

However, due to the size constraints of proportional counters, their use in high-energy particle physics was limited and could not satisfy the particle tracking requirements. In 1930, this objective was achieved using photographic emulsions, which successfully recorded the tracks of fast-moving charged particles. The development of excellent imaging detectors such as Cloud Chambers in 1927 by Charles Thomson and Bubble Chamber by Donald Arthur in 1960 completely banished the use of emulsions in nuclear physics investigations.

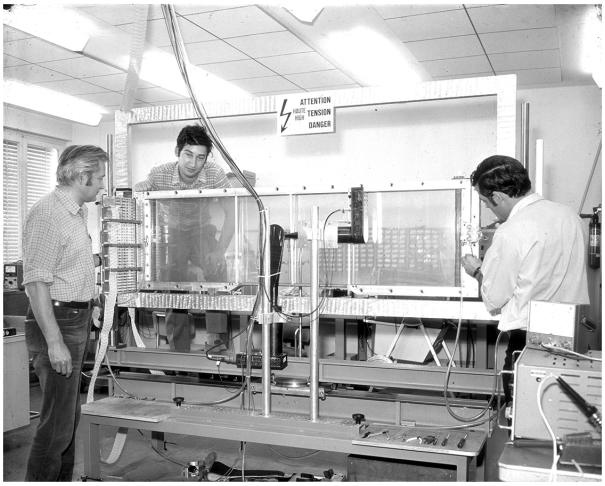
However, the use of these devices was limited to smaller acquisition time windows due to the requirement of external mechanical control and lack of correlation to the physical events under study. This limitation was overcome by the Triggered Spark chamber's invention, developed by Fukui and Miyamoto in 1959. This gas counter was made sensitive in coincidence with the selected events. A set of external scintillator counters provided a trigger signal to the spark chamber; thus, selective event (triggering) originated. Using a four-gap spark chamber provided a clear sampled image of particle tracks, detectable within a short duration. In the 1960s, CERN also developed PS11, an optical sparks chamber experiment, at Proton Synchrotron (PS) facility. These spark chambers also suffered from a slow picture recording process and quickly evolved by new faster electronic devices.

In the late 1960s, the need for large area and high-speed particle physics detectors obtained paramount importance. In 1967, Georges Charpak invented Multi-Wire Proportional Chamber (MWPC) at CERN. This invention revolutionized the field of position-sensitive radiation detectors. The MWPC showed time resolution of nanoscale with sub-millimeter position accuracy and high detection rate capability. Figure 2.1a shows Charpak's technician, R. Bouclier, standing next to the first MWPC having 24 anode wires and 10×10 cm^2 active area. Figure 2.1b shows one of the first large size working chambers, constructed by the Charpak's group in 1970. Charpak received Nobel Prize in 1992 for this invention and fundamental physics research. Charpak also led the Gas Detector Development (GDD) group at CERN.

The continuous advent of particle accelerators posed a challenge to develop faster and large area gas detectors for particle physics experiments. The GDD group experimented with gas mixtures and found a "Magic gas" mixture which enhanced the original MWPC's gain from 10^5 to 10^7, enabling the detector to produce large current pulses independently of the primary ionization release. It resulted in simplified readout electronics designs. This "Magic gas" consisted of argon-isobutane and freon. In 1970, the GDD group prototyped one of the world's largest (1.5m long) MWPC in CERN (see Figure 2.1b). In 1974, 40 large MWPC modules were deployed, which acquired particle data at several kHz rates. This kind of performance was unthinkable with other older tracking devices.

Several generations of MWPC detectors were developed during the next decade by many researchers [14, 15] and used in nuclear and particle physics applications. However, technology limits for these detectors had been reached for granularity and spatial resolution. In 1988, A.Oed invented the Micro-Strip Gas Cham-

(a) First MWPC at CERN (1968). Roger Bouclier, a technician of Charpak, is working with the new invention.



(b) A large MWPC chamber, with (left to right) Georges Charpak, Fabio Sauli and Jean-Claude Santiard, Picture CERN (1970).

Figure 2.1: Pictures of first small and large prototype MWPC detectors

ber (MSGC) that solved a fundamental rate limitation of wire chambers due to positive-ion accumulation in the gas volume [16]. This MSGC detector achieved localization accuracies and multi-track resolutions of 50 μm and 500 μm respectively for the particle fluxes up to 2.3 MHz/cm^2.

Despite the unbeatable performance of these MSGCs, detailed longevity studies of these detectors revealed two significant drawbacks, especially for particle physics collider applications. The first of these issues was the formation of charge deposition on electrodes, which reduces the gain, timing accuracy, and lifetime of these detectors. Secondly, beam tests with highly ionizing particles (HIP) of these detectors also revealed the generation of destructive discharges, which led to permanent damages to these detector structures [17].

In the late nineties, the gaseous detector development was boosted by enormous advancements in photolithography and micromachining techniques. The MWPC structures were then quickly replaced with new Micro-pattern Gas detector (MPGD) structures. These structures provided extremely small cell-size and excellent radiation resistance due to the simplicity of the microstructures. Soon after the MSGC, the GEM was introduced by F.Sauli in 1997, and Micro-mesh Gaseous Structure (Micromegas) by I.Giomataris in 1996 [18, 19]. Like the MSGC, these new detectors offered unprecedented spatial performance compared to past generations of gaseous detectors. These new technologies also showed long-term operational stability, large sensitive area, high time resolution, and rate capabilities [20, 21]. The development of highly integrated readout front-end electronics such as APV25 [22] and VFAT further allowed the design of MPGD detector systems with channel densities comparable to modern silicon detectors.

CERN deployed first of its GEM detectors in the COMPASS (COmmon Muon Proton Apparatus for Structure and Spectroscopy) and TOTEM (TOTal cross section, Elastic scattering and diffraction dissociation Measurement at the LHC) experiments, which already have proven to meet the claims of high resolution, fast

timing, and long term stability against radiation damages likely to occur in high radiation environments. COMPASS is a high-energy physics experiment at the SPS, started in 2002, to study hadron structure and investigation of quarks and gluons interactions that produce observable particles. Precise measurements of protons were performed in the TOTEM experiment. It is the 'longest' experiment of LHC with almost half a kilometer spread of detectors around the CMS interaction point. In 2015, the TOTEM and CMS collaboration started joint physics measurements.

In 2009, the CMS collaboration launched a dedicated R&D program to study the possibility of installing GEM detectors in the muon endcaps. This GEM upgrade comprises three different stations. The first GEM station, GE1/1, has been installed during the LS2 (2018-2021) and will be described in more detail in the following sections. The other two GEM stations will be discussed in Chapter 8.

2.3 Importance of the GE1/1 GEM upgrade

As seen in section 1.7, the CMS muon endcap is instrumented with four CSC layers only, in the region $1.5 < |\eta| < 2.4$. It is the only region of the CMS muon spectrometer where the RPCs have not been installed, while the background particle rate is the highest, above 1 kHz/cm^2. The CMS magnetic field is also lower and less uniform in that region, increasing the uncertainty on the muon momentum measurement.

Standard RPCs do not sustain particle rates above 1 kHz/cm^2, but Triple-GEM detectors easily do [9]. In addition, the thin profile of the Triple-GEM detectors, a few cm, allows them to be slid in the space left vacant by the RPCs (see Figure 2.2).

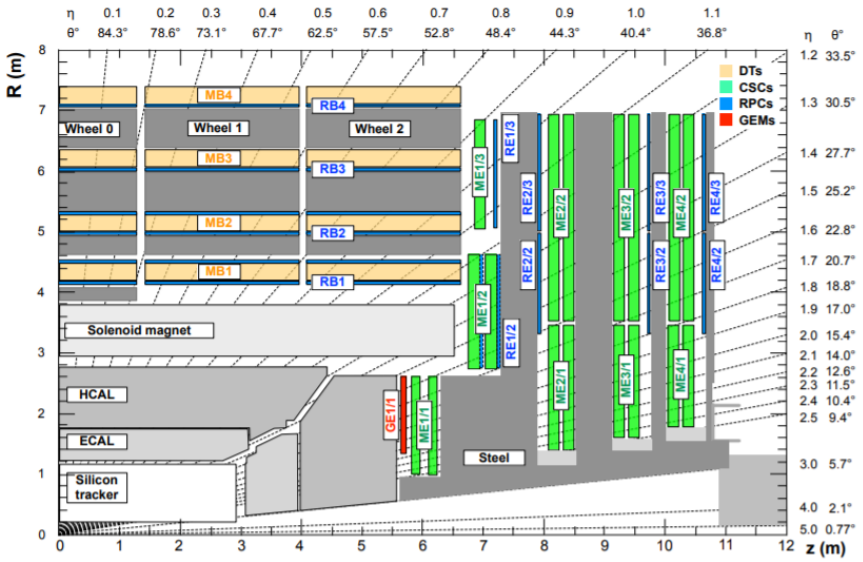


Figure 2.2: A quadrant of the R - z cross-section of the CMS detector, highlighting in red the location of the proposed GE1/1 detector within the CMS muon system.

GE1/1 will provide two additional hits to the muon track, which will improve the muon track p_T resolution. One can also notice that combining GE1/1 hits

with the CSC ME1/1 hits increases the path length traversed by muons within the first muon station by a factor of 2.4 - 3.5 over that of the six layers of the CSC ME1/1 hits alone. The increased path length, in turn, significantly improves the L1 stand-alone muon trigger momentum resolution and drastically reduces its disproportionately large contribution to the overall L1 muon trigger rate. The formation of lever arm by the incorporation of GE1/1 chambers in front of a CSC ME1/1 chambers within the CMS muon endcap is shown in Figure 2.3.

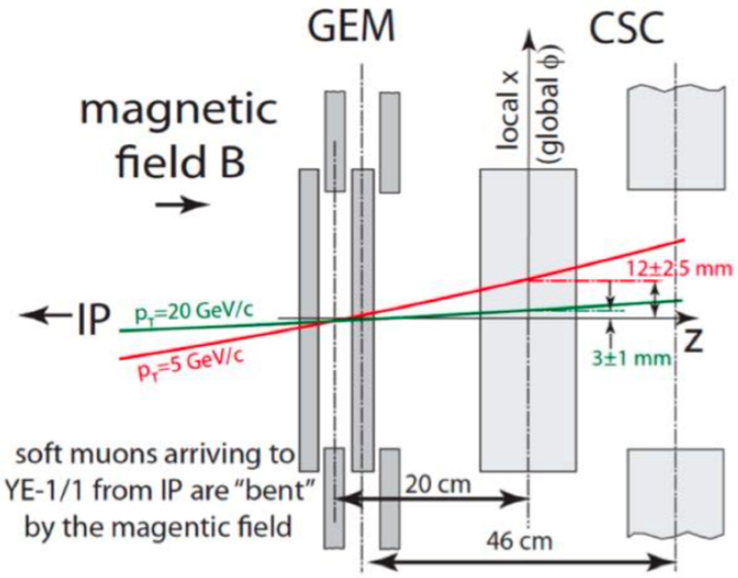
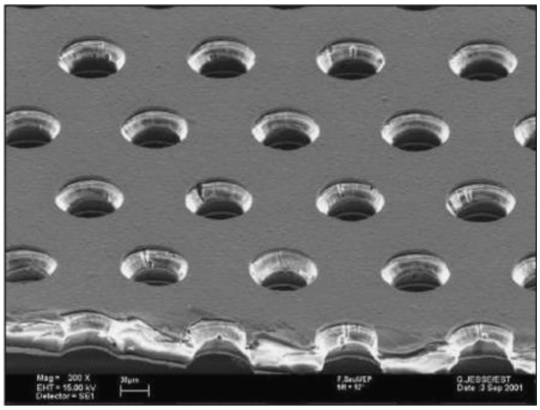


Figure 2.3: GE1/1 chambers in front of a CSC ME1/1 chambers within the CMS muon endcap

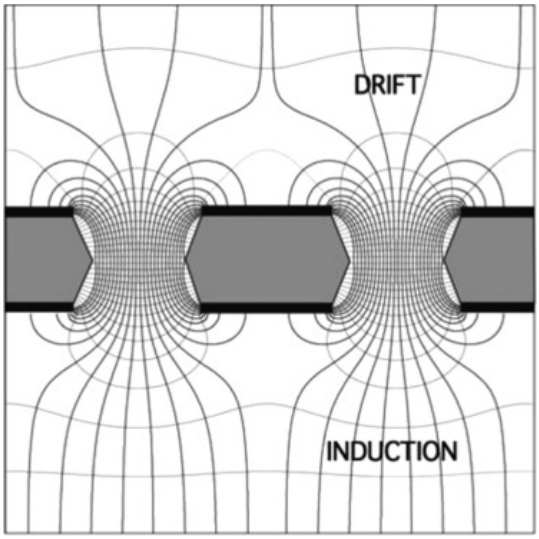
The creation of this large lever arm enables a good measurement of the muon "bending angle" within the first station and enhances the discrimination between lower and higher momentum muons.

2.4 GEM working principle

The Gas Electron Multiplier (GEM) detector is a gas-filled charge amplifier device invented by Fabio Sauli in 1997 [20]. The active element of GEM is a thin self-supporting composite mesh realized by photolithographic processes. A 50 µm thick polymer foil (Kapton) is coated with two 5 µm thin copper sheets on both sides and pierced with a high density of small holes. The etching pattern usually has 70 µm holes with 140 µm spacing on a hexagonal grid. The shape of holes is bi-conical, with the larger diameter on entry sides, due to double-side etching used in the process. This conical shape also helps to improve the dielectric rigidity of the foil. An electron microscopic picture of a GEM foil is shown in Figure 2.4a. A specialized etching and cleaning procedure is required to remove any residual metallic fragments or conducting deposits within the holes. On application of a suitable potential difference between both electrodes, an intense electric field (tens of kV/cm) develops within the micro holes as shown in Figure 2.4b



(a) Electron microscope picture of a section of typical GEM foil, 50 µm thick. The holes pitch and diameter are 140 and 70 µm, respectively.



(b) Simulation of the electric field in the region of the holes of a GEM foil.

Figure 2.4: GEM foil cross-section and electric field in the holes simulation.

The foil is placed in a gas, typically a mixture of Ar/CO_2, and in the presence of uniform potential between two electrodes, it becomes sensitive to detect incoming particles. Figure 2.5 shows the working principle. Once a particle enters the sensitive gas volume, it ionizes gas atoms/molecules along its track. The resulting electrons drift towards the micro holes where the high electric field accelerates the electrons and creates avalanches, multiplying the number of electrons. The resulting charge is detected by the readout electronics connected directly to the readout strips.

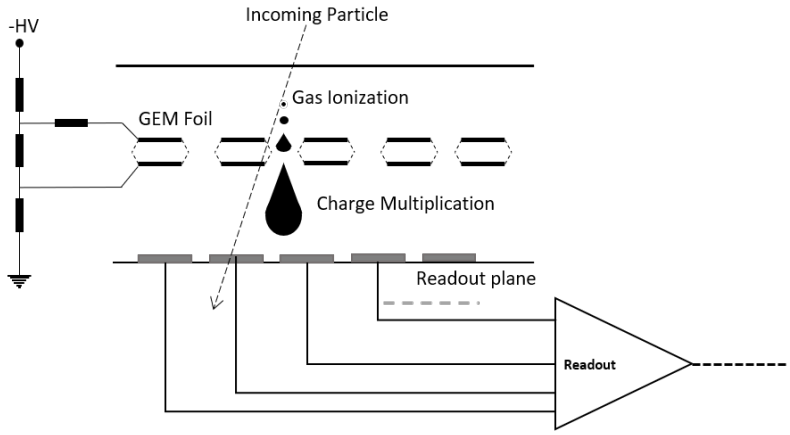


Figure 2.5: GEM working principal

Due to the GEM geometry and operating principle, it was quickly established that the charge obtained from the first stage of GEM foil could further be amplified by cascading additional GEM foils before reaching the anode strips [23, 24, 25]. The noticeable advantage of multiple GEM structures is that the desired gain can be reached with very low voltage per electrode, thus producing fewer gas

discharges than earlier gas detectors.

The most popular triple GEM scheme is adopted for GE1/1 detectors and is shown in Figure 2.6.

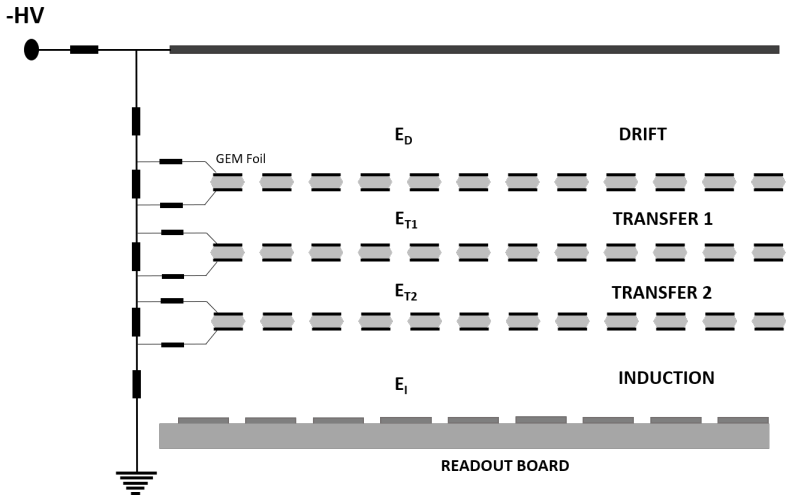


Figure 2.6: Schematic of a triple GEM detector

The GE1/1 triple GEM detector has 3 GEM foils with the following configuration: 3 mm drift gap, 1mm transfer-1 gap, 2mm transfer-2 gap, and 1 mm induction gap. A comparison of effective gain and discharge probability of single, double, and multiple GEMs is shown in Figure 2.7.

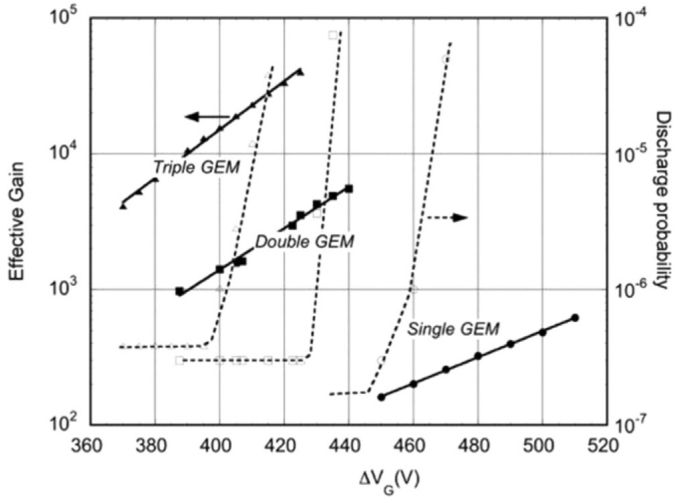


Figure 2.7: Effective gain and discharge probability comparison as a function of GEM electrode voltage in different multi-GEM detectors [20].

Several studies to cascade up to five GEM structures have also been done in [26] and [27]. These studies revealed that triple GEM configuration provided the highest ion backflow suppression.

2.5 Mobility and diffusion of charges in gases

When a charged particle crosses a gas volume, it produces primary and secondary ionization. The ions produced quickly lose their energy by colliding with gas molecules if no electric field is applied. The average thermal energy of electrons at normal temperature is $\epsilon_T = \frac{3}{2}kT \simeq 0.04\ eV$. By using the kinetic theory of gases, the energy loss of ions follows a Maxwell distribution [14]:

$$F(\epsilon) = C\sqrt{\epsilon}\, e^{-\epsilon/kT} \tag{2.1}$$

where T is the temperature of gas and k is the Boltzmann constant.
If there is no other external field present then local charges diffuse due to multiple scattering by following the Guassian law:

$$\frac{dN}{N} = \frac{1}{\sqrt{4\pi D\tau}} e^{-(x^2/4D\tau)} \cdot dx \tag{2.2}$$

where dN/N is the fraction of charges found at time τ in the region dx at an offset x from the primary ionization point. The D is the diffusion coefficient related to the nature of gas and charges. The standard deviation for this distribution is

$$\sigma_x = \sqrt{2D\tau} = \sqrt{\frac{2Dx}{v_d}} \tag{2.3}$$

On application of an electric field, these charges acquire a net drift velocity v_d in the direction of applied field E:

$$v_d = \frac{eE}{m}\tau \tag{2.4}$$

In the simplest case where the electric field has the least impact on the energy of the electrons, then mean collision time τ is considered constant. In these conditions, the drift velocity v_d varies linearly with the applied field. It is convenient to define a parameter μ as a ratio particle's drift velocity to an applied field, called mobility as,

$$\mu = \frac{v_d}{E} \tag{2.5}$$

The Einstein's relation for electrical mobility in gases shows that the diffusion coefficient D is related to the "mobility" as,

$$D = \frac{\mu kT}{e} \tag{2.6}$$

Substituting equations 2.5 and 2.6 in equation 2.3, we get

$$\sigma_x = \sqrt{\frac{2kTx}{eE}} \tag{2.7}$$

This expression shows the diffusion of ions, with a probability distribution expressed by eq. 2.2, moving over a length "x" in a time τ. It defines a thermal

limit to the diffusion of the ions. It can be seen that the root mean square of linear diffusion is independent of the ion and gas nature. The variations of σ_x at 1 atm pressure for different gas mixtures as well as the equivalent time dispersion σ_t, for several gas mixtures and 1 cm drift, are shown in Figure 2.8.

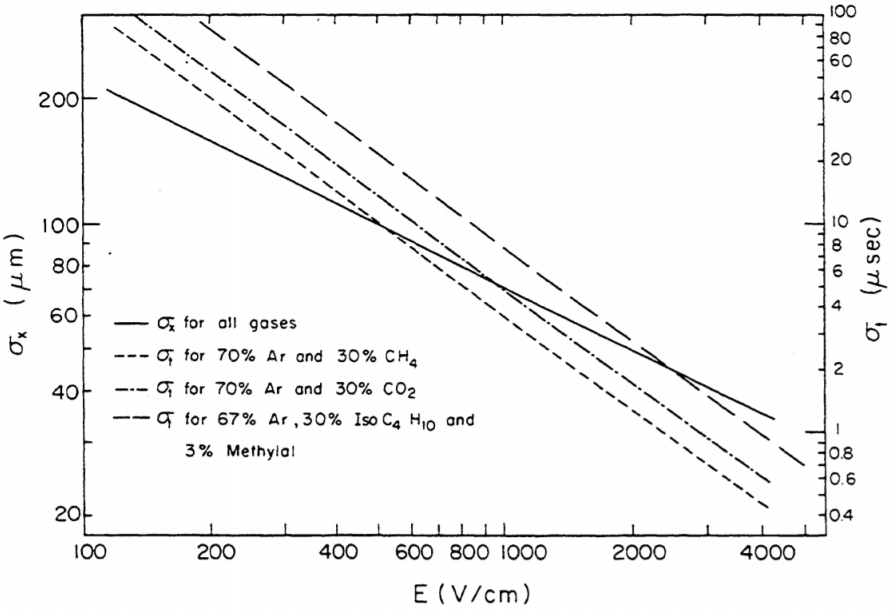


Figure 2.8: Positive ion diffusion in space and time for 1 cm drift length versus electric field.

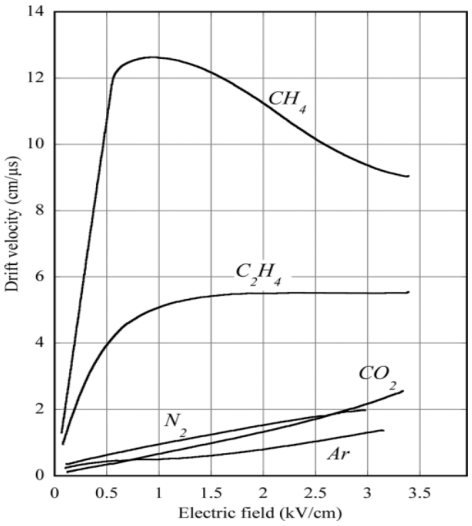
2.6 Electrons drift velocity

The presence of an electric field and nature of gas mixtures, both have a strong influence on acquired electron drift velocity. Several experimental studies showed that the addition of controlled amounts of impurities in the pure, noble gases provided a stable and high gain detector operation [20]. Figure 2.9a shows a wide variation of drift velocities of electrons in various pure gases at NTP (Normal Temperature and Pressure). The addition of a small fraction of other gases modifies the drift velocity of electrons in the same mixture. Variation of electron drift veocity with electric field for different Argon mixtures is shown in Figure 2.9b.

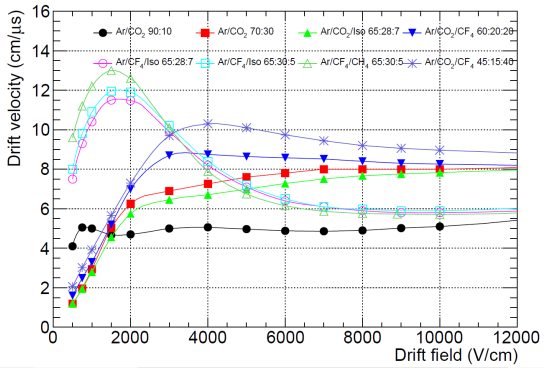
In the case of MPGDs, electron drift velocities have been measured up to very high fields, above 10kV/cm, and reported in [20, 28]. As an example, the electron drift velocity in Ar/CO_2 (70/30) reaches 80 µm/ns at 10kV/cm.

2.7 GEM avalanche phenomenon

Due to the intense electric field in the GEM holes, the ionization electrons gain sufficient energy and produce secondary ionization. Thus a chain reaction can be produced, called an avalanche, responsible for amplifying primary charge in gaseous detectors. The number of secondary electrons knocked out by the primary electrons per unit path length can be determined by the first Townsend



(a) Drift velocity of electrons as function of elctric field in pure gases at NTP



(b) Variation of the electron drift velocity with electric field for different Argon based gas mixtures.

Figure 2.9: (Left) Drift velocity of electrons in various noble gases, and (right) drift velocity of various Argon gas mixtures [28] in MPGDs

coefficient (α). If p is the gas pressure, then α is related to p by using Korff's approximation:

$$\frac{\alpha}{p} = Ae^{-Bp/E} \tag{2.8}$$

where the parameters A and B depend on the gas type and electric field. If we start with $n_\circ$ primary electrons, and α represents the average number of ionization collisions made by these electrons per unit length traveled in the electric field direction, at any distance x starting from primary ionization, the number of total electrons can be written as:

$$n = n_\circ e^{\alpha x} \tag{2.9}$$

The gain factor $M = \frac{n}{n_\circ}$ between x_1 and $_2$ can be written as:

$$M = exp\left[\int_{x_1}^{x_2} \alpha(x)dx\right] \tag{2.10}$$

If we increase the electric field, gas amplification exponentially increases and limits around M = 10^8, known as the Raether limit, and it corresponds to $\alpha x \sim 20$. This limit is attributed to the space charge's influence on the electric field and the avalanches' spread by photon emission.

2.8 GEM signal formation

The induced current for a specified electron motion can be estimated using the classic Shockley-Ramo theorem [29]. The instantaneous current i can be com-

puted as:

$$i = E_v e v \tag{2.11}$$

where e is the charge of the electron, v is electron drift velocity and E_v is the electric field component in the direction of v at the electron instantaneous position provided electron removed, given electrode raised to unit potential, and all other conductors at zero potential. In GEM devices, as soon as the free electrons are produced into the induction gap, a current pulse grows on the electrodes, which stops when all electrons are completely collected. Using equation 2.11, given n electrodes at different potentials $V_1, ..., V_j, ..., V_n$, the current flowing into k^{th} electrode due to a moving charge q can be written as:

$$I_k = \frac{-q\vec{v}(x) \times \vec{E}_k(x)}{V_k} \tag{2.12}$$

Where $\vec{E}_k(x)$ is the electric field produced by the k^{th} electrode raised to the potential V_k while ignoring effects of other electrode's potentials. As a special case, if $V_k = 1V$, then the resulting electric field is called 'weighting field' $\vec{E}_k^w$ and the instantaneous current can be written as:

$$I_k = -q\vec{v}(x) \times E_k^w(x) \tag{2.13}$$

In GEMS, we try to keep the electric field stable and thus drift velocity becomes constant too. It means the drifting electrons induce a constant current I, and if q is the charge collected, we know

$$\int_{t_{drift}} I \cdot dt = q \tag{2.14}$$

It can be seen that for a specific charge of q, a shorter drift time will result in a higher current. Thus a thin induction gap or a fast gas is always recommended to achieve short drift time [30]. The higher value of current I is desired for improved signal-to-noise ratio and detection of small charges, making the detector extremely sensitive and desirable for particle physics applications. Moreover, the fast signals are also desirable for LHC applications, where the beam collision period is as small as 25 ns; therefore, we need fast detector response and good timing resolution (better than 8 ns).

The charge produced by the triple GEM structure is eventually collected by anode strips individually connected to the readout electronics. Typically the anode strip pitch is 200 µm. One of the particularities of signal formation within GEM detectors is that the signal induced on the anode strips is purely caused by the drift of the electrons extracted from the GEM foil facing the anode strips. No ions exit the GEM holes towards the induction gap. Therefore the triple-GEM signal is exclusively due to the electrons, and the signal length is driven by the induction gap size, the electron drift velocity, and the induction electric field.

Figure 2.10 shows GARFIELD simulation of three typical induced current signals with the gas mixture $Ar/CO_2/CF_4$ (45/15/40) performed by [31]. On the first induced signal, two peaks between 40 and 70 ns come from two different clusters of electrons created in the Drift gap but spatially separated by $\sim$2 mm.

The geometry used for the simulation was 3/1/2/1 mm. The electric field

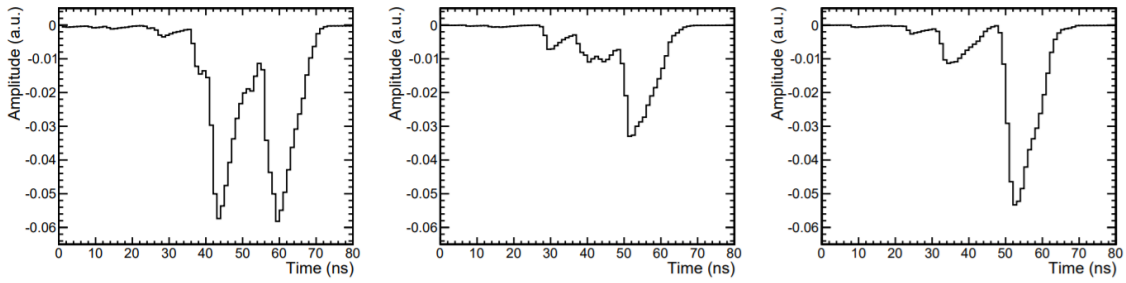


Figure 2.10: A GARFIELD simulation of three independednt induced signals for a gas mixture of $Ar/CO_2/CF_4$(45/15/40 [31].

for the Drift and transfer gaps was 3 kV/cm and 5 kV/cm for the Induction gap. The voltage applied to the three GEM foils was 400 V. The identification of the contribution of the primary ionization to the signal from the different GEM region are indicated by vertical dashed lines in Figure 2.11. An apparent correlation of

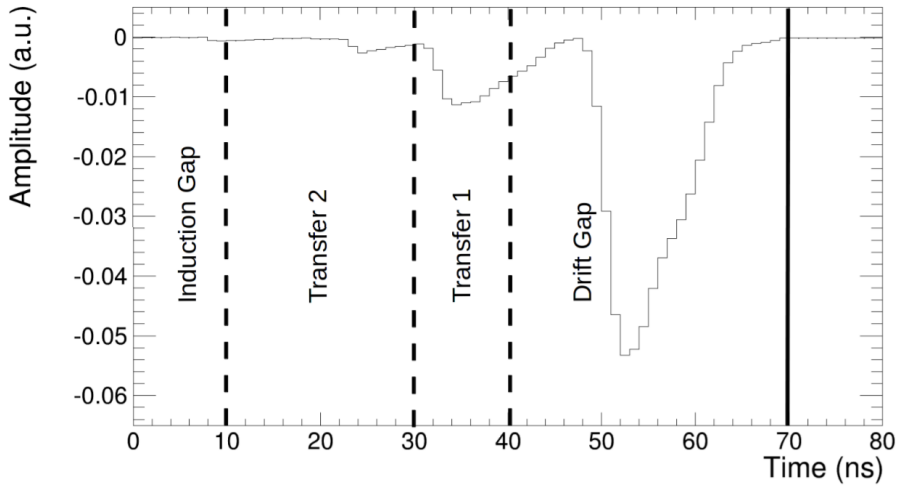


Figure 2.11: GEM GARFIELD simulation of Induced signal for a gas mixture of $Ar/CO_2/CF_4$ (45/15/40) [31].

induced signal by the electrons in different regions can be seen within a span of 0 to 70 ns. The large variations in the amplitude of the peaks within same regions (Induction, Transfer and Drift) are due to the statistical fluctuations of the ionization and the amplification of the electrons.

2.9 GE1/1 GEM detector

In 2009, the CMS collaboration proposed to instrument the very forward region of muon endcaps with triple GEM detectors. Consequently an extensive R&D program was started. It was decided to first instrument the GE1/1 GEM stations during the LS2 long shutdown. Over the years, ten generations of GE1/1 detectors were produced, improving robustness and improving the fabrication procedures with each new design [32]. The radiation hardness of GEMs is already demonstrated by beam test performed in [33]. The CMS GE1/1 detector

consists of a trapezoidal drift board, three stacked GEM foils, a readout board, and an external gas housing. The final used gap configuration is 3/1/2/1 mm, optimized for timing resolution and reduced gas discharges. Two GEM detectors are coupled together to make a super chamber. An exploded-view of a GE1/1 GEM detector is shown in Figure 2.12.

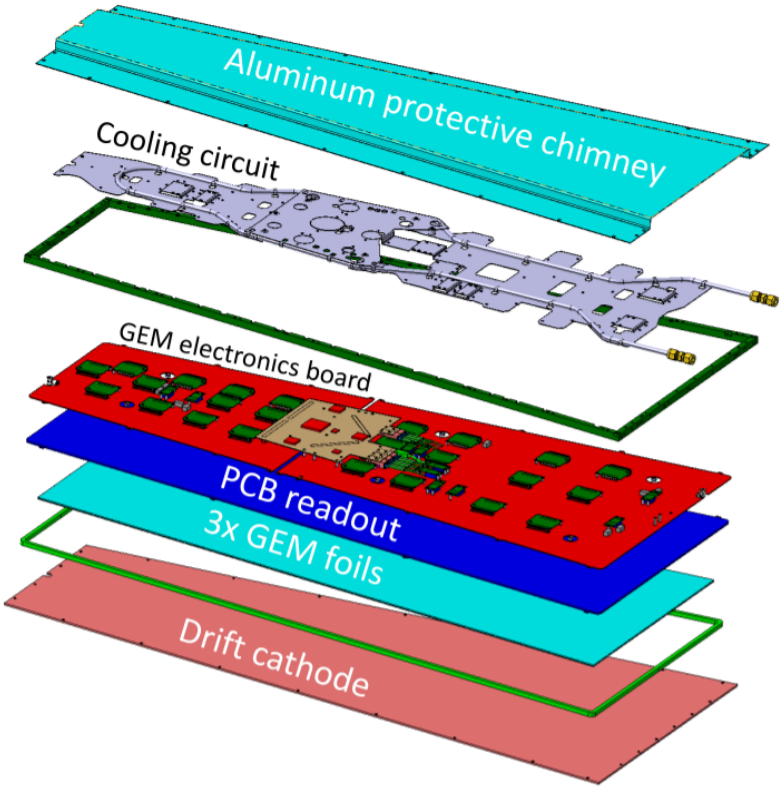


Figure 2.12: Exploded view of a GE1/1 GEM detector.

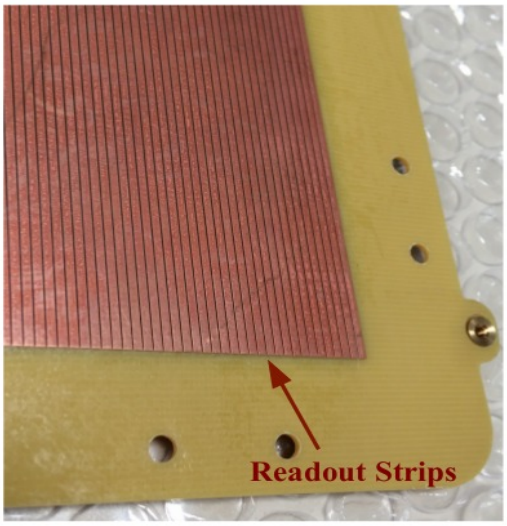
Due to mechanical constraints imposed by the structure of CMS endcaps, two different versions of chambers a 'long' one (128.5 cm) and a short 'one' (113.5 cm), were designed to achieve maximum detection coverage [34]. The key technical specifications for the GE1/1 detector are shown in the table 2.1. The GE1/1

Specification	Short	Long
Shape	Trapezoidal	Trapezoidal
Chamber length	113.5 cm	128.5 cm
Chamber width	(28.5 - 48.4) cm	(28.6 - 51.2) cm
Chamber thickness	74 mm	74 mm
Active readout area	3787 cm^2	4550 cm^2
Active chamber volume	2.6 liters	3 liters
Geometric acceptance in η	1.61 - 2.18	1.55 - 2.18

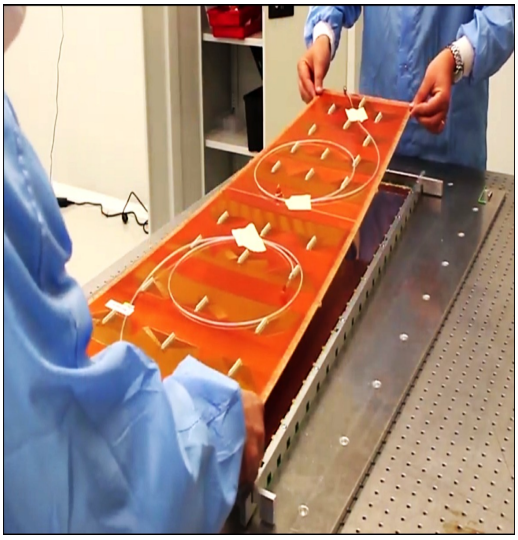
Table 2.1: GE1/1 GEM station key specifications

detectors are assembled in super chambers covering 10° in ϕ. A super-chamber consists of a combination of two fully assembled GEM detectors coupled. The long and short super chambers alternate in ϕ covering $1.55 < |\eta| < 2.18$ for long

and $1.61 < |\eta| < 2.18$ for short versions of detectors to enhance the coverage of available spacing. The total available width for GE1/1 is only 88 mm, and the final design of the detector measured only 74 mm of space, leaving a sufficient margin of 14 mm.



(a) Closeup of GEM readout strips



(b) Closing of Outer side of GE1/1 readout board showing $24(\eta, \phi)$ readout sectors, each with a male Panasonic connector for signal readout.

Figure 2.13: GE1/1 readout board is used to collect the charge produced in the GEM-3 bottom. The charge is collected by copper strips and readout by the front-end ASIC called VFAT3.

The GEM foils are segmented in 40/47 HV sectors and the readout board is segmented in 3 x 8 readout sectors in (ϕ, η) directions. Each sector has 128 readout strips, totaling 3072 readout channels per single chamber. Figure 2.13 shows a GE1/1 readout board partitioned in 24 sectors with Panasonic connectors mounted to connect the front-end devices on the bottom of the board. The chambers will use Ar/CO_2 (70/30) gas mixture to achieve a nominal gas gain of ~10^4.

2.10 Performance of GE1/1 detectors

Several GE1/1 detector generations were designed and tested to achieve optimum detector gain, efficiency, timing resolution, and discharge probability with two different gas compositions: Ar/CO_2 and $Ar/CO_2/CF_4$. Several experimental setups were designed to measure and tune for CMS operations' best achievable parameters. We discuss these performance parameters and their experimental setups briefly in the following sections.

2.10.1 GE1/1 gain measurement

In GEM-based detectors, the effective gas gain is defined as the ratio between the current induced on the GEM readout board and the primary current induced in the drift gap by the X-ray source. The total input current can be obtained by multiplying the rate of X-rays with the primary charge deposited by each photon in the drift gap. The effective gas gain G, thus can be written as:

$$G = \frac{I_{readout}}{I_{primary}}$$
$$G = \frac{I_{readout}}{R_s \times n_p \times q_{el}} \tag{2.15}$$

where:
$I_{readout}$ - Current collected at readout anode
R_s - Rate of source X-ray
q_{el} - elementary electron charge, and
n_p - average number of primary electrons released by individual X-ray photons in the drift gap

Gain measurements are performed by X-ray irradiation of the the detector in a customm designed closed copper chamber shown in Figure 2.14. A 4-Watt Amptek X-ray source with Silver target was used having operating voltage 20-40 kV and operating current of 5-100 μA

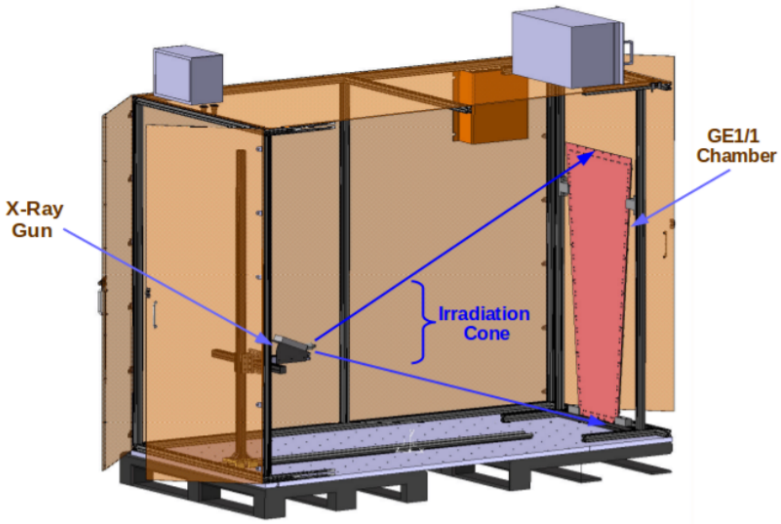
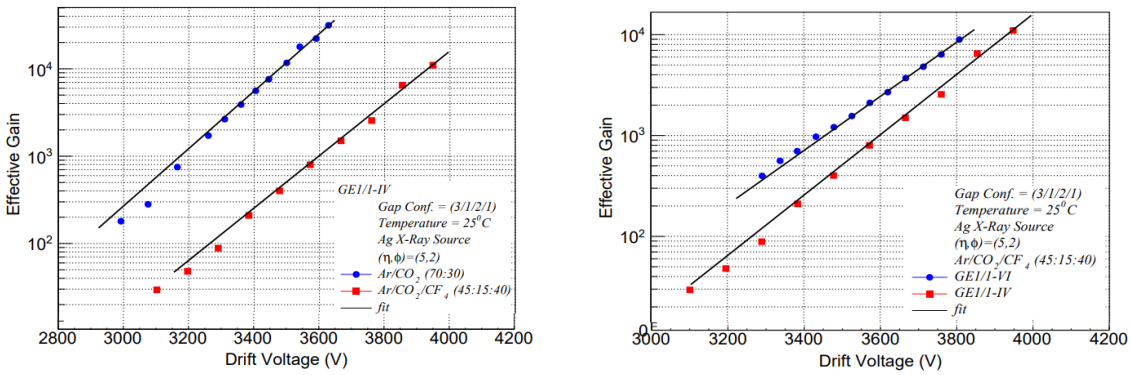


Figure 2.14: A custom designed setup used for gain measurements of GE1/1 detector using an X-ray tube inside the copper chamber [32].

The GE1/1 chamber was flushed by gas mixture at least 5 hours before the measurements to allow uniform gas flow inside the full detector. Two test gas mixtures were experimented at a rate of 5 liters/hr, namely Ar/CO2 (70/30) and Ar/CO2/CF4 (45/15/40). The gain measurements of various generations of GE1/1 detectors were computed and compared with each other to achieve optimum values suitable for HL-LHC conditions. Two such measurements are shown in Figure 2.15.



(a) Fourth Generation GE1/1 gain with gas mixtures Ar/CO_2(70/30) and $Ar/CO_2/CF_4$ (45/15/40).

(b) Gain Comparison between fourth and sixth generations of GE1/1 detectors

Figure 2.15: Gas gains for different generations of GE1/1 detectors [32].

Figure 2.15a shows the effective gain comparison of the 4^{th} generation GE1/1 prototype with two different gas mixtures. It was observed that the higher gains could be achieved with the gas mixture of Ar/CO_2 as compared to $Ar/CO_2/CF_4$. The small gain with the addition of CF_4 is the quenching property of CF_4, which absorbs electrons in the gas mixture. A comparison of fourth and sixth generations of GE1/1 effective gains with a gas mixture of $Ar/CO_2/CF_4$ is also shown in Figure 2.15b. It can be seen that the sixth generation of detectors has higher gains as compared to the fourth generation of detectors. This difference is the different orientations of single mask GEM foils used in GE1/1 of detectors. It was well established later on that orientation of single mask GEM foil also contributes to improve the effective detector gain. The CMS preferred orientation of GEM foils is the narrow side of holes face incident radiation, producing higher gains [35].

2.10.2 GE1/1 efficiency measurement

The GE1/1 detector efficiency was measured by using CERN beam facilities at the SPS (see section 1.2). A 150 GeV beam of muons was obtained by the bombardment of the primary proton beam at the beryllium target. The muons beam was then filtered and collimated before firing on the GEM detectors. A test setup to measure the GE1/1 GEM detector's efficiency is shown in Figure 2.16. Three plastic scintillators (shown in gray) were used for trigger reference and two 10×10 triple GEM detectors, having two-dimensional readout planes, for muon tracking measurements. The GE1/1 signals were readout by VFAT2, a digital output readout chip designed for the TOTEM collaboration project [36].

The efficiency measurements were done using one small sector of GE1/1 perfectly aligned with $10 \times 10\ cm^2$ GEM detector and a scintillator active area region.

The detector efficiency is defined as the ratio between the number of muons detected by the GE1/1 sector under consideration and the total number of triggers generated by three scintillators' coincidence. The efficiency of the detector can be written as:

$$\epsilon = \frac{N_1}{N - N_2} \tag{2.16}$$

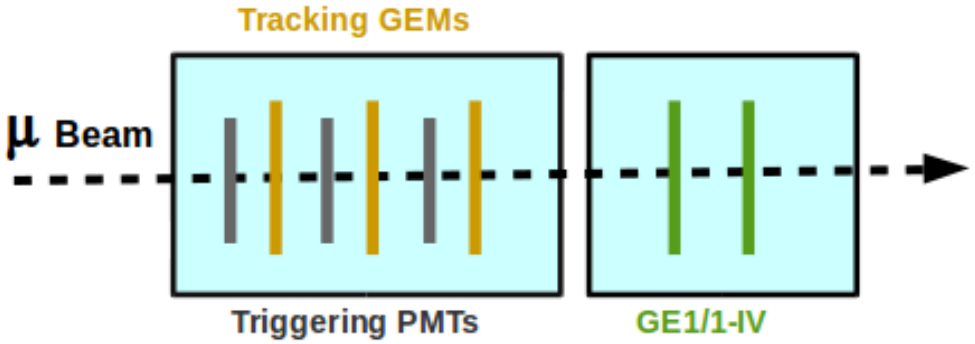


Figure 2.16: GE1/1 efficiency measurement setup , scintillator detectors are shown in dark gray, and 10 x 10 cm^2 GEM detector tracking GEM detectors are shown in yellow. A 4^{th} generation GE1/1 GEM is aligned with the setup and muon beam is orthogonal to all the detectors [37].

where:
N_1 - number of hits detected by test region
N - total number of hits detected by the coincidence of three scintillators, and
N_2 - number of hits recorded by neighboring regions of GE1/1 detector.

Due to slight misalignment between the GE1/1 detector and test detectors, a few hits were also detected by neighboring regions of GE1/1, which need to be subtracted from the total number of reference hits. An efficiency measurement plot with both gas mixtures of Ar/CO_2 and $Ar/CO_2/CF_4$ is shown in Figure 2.17 [32].

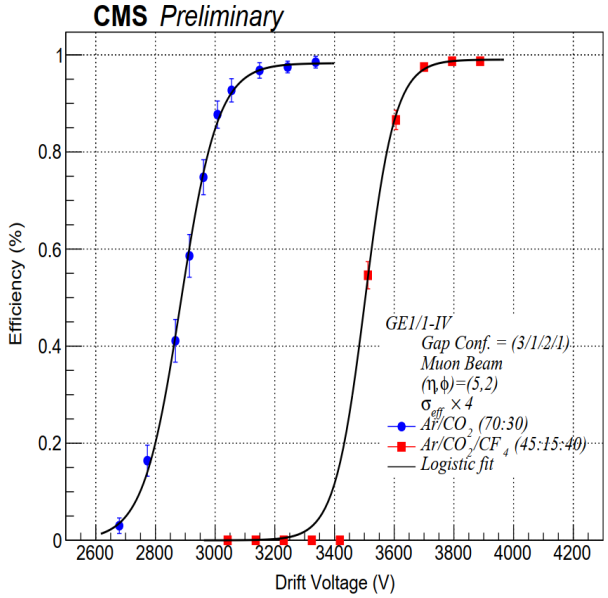


Figure 2.17: GE1/1 efficiency measurement plot [32].

Over 98% of efficiency was observed as a function of drift voltage. It was observed that the same efficiency figures were obtained with the Ar/CO_2 at 17% less drift voltage as compared to $Ar/CO_2/CF_4$. The lower desired drift voltage

also ensures less discharge probability.

2.10.3 GE1/1 timing resolution

The timing resolution of the GE1/1 detector was also measured using the same experimental setup explained in the previous section 2.10.2. The events formed by the coincidence of three scintillators were injected into a Time to Digital Converter (TDC) stage. In contrast, a delayed GE1/1 event signal was injected into the second input of TDC, acting as a stop signal. The time difference between both signals was calculated for each event, and the time difference distribution was obtained. The standard deviation of the distribution is the time resolution of the detector. A typical plot for GE1/1 time resolution as a function of the detector gain is shown in Figure 2.18.

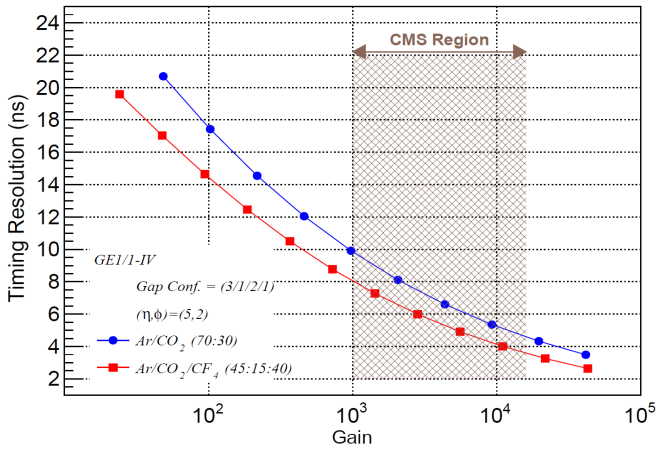


Figure 2.18: GE1/1-IV timing resolution for Ar/CO_2 (70/30) and $Ar/CO_2/CF_4$ (45/15/40) gases as a function of gain. The shaded portion 'CMS Region' is the expected operational region of the GEMs in CMS HL-LHC [32].

A time resolution suitable for CMS applications, better than 10 ns, is achieved for both gas mixtures, Ar/CO_2 (70/30) and $Ar/CO_2/CF_4$ (45/15/40). It is 24% better with CF_4, however Ar/CO_2 (70/30) has been finally chosen as it provides good enough time resolution for CMS while it is environment friendly.

2.10.4 GE1/1 rate capability

The expected rate at the GE1/1 position is expected from simulation to be less than 20 kHz/cm^2 [2]. An intense beam of variable-flux X-ray was used to calculate the rate capability. The amplified current was measured by a pico-ammeter connected directly to the detector anode. Figure 2.19 shows that effective detector gain is stable over the entire particle rate range of interest.

2.10.5 GE1/1 discharge probability

The gaseous detectors are known to produce gas discharges if operated at very high gas gains (>10^4). In the case of GE1/1, the higher gas gain improves the timing resolution. However, on the other hand, it increases the discharge probability,

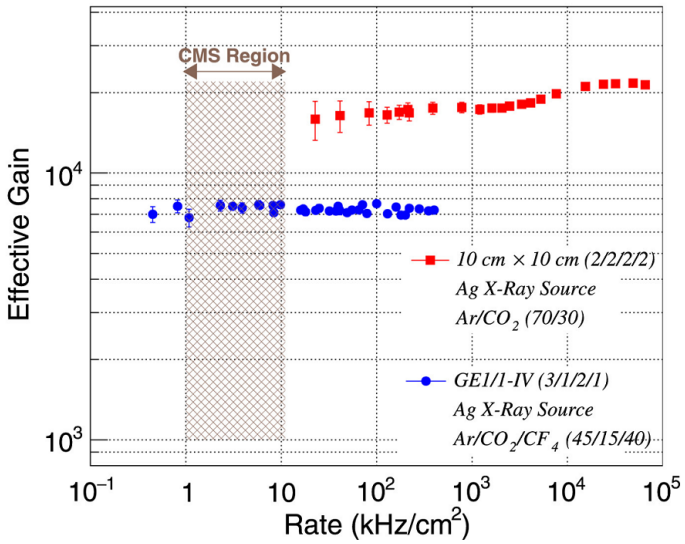


Figure 2.19: Rate capability of a GE1/1-IV chamber and a 10 $\times$ 10 cm^2 GEM detector. The shaded portion is the expected 'CMS Region' during HL-LHC [32].

and intense particle fluxes can quickly produce gas discharges, which ultimately damages the GEM foils or the electronics.

Gas discharges can be initiated when the amplified charge exceeds the Raether limit (see section 2.7). The electric field varies locally with the avalanche; turning them into streamers (uncontrolled avalanches that travel in both directions) which can provoke gas breakdown. In GE/1, slightly different voltages across three of the GEMs foils were applied. The voltage across GEM-1 was 3% higher than GEM-2, which was also at 5% higher potential than GEM-3 foil. This configuration reduced discharge probability to a significantly low level because of gain sharing by cascading of three amplification stages. Besides, these stages were made electrically isolated from the readout plane, which significantly limited the streamer's propagation to the anode plane.

GE1/1 has a large foil, and minor damage to a small foil section can discard the whole detector. This shortcoming was solved by making isolated sectors of 100 cm^2 on GEM foil' topsides (towards drift plane). Each sector is then connected to the electric voltage by the use of a 10 MΩ protection resistor. In the case of large discharges, these resistors limit the dissipation of excess energy in the GEM foils, thus increasing the GEM detector's robustness. CMS has adopted this foil partitioning after a detailed study of foil segmentation at CERN [38].

To measure the discharge probability, GE1/1 detector and 10 x 10 cm^2 GEM detector [39] were irradiated by highly ionizing α-particles from ^{241}Am. The discharge probability for third generation GE1/1 is shown in Figure 2.20. The discharge probability was evaluated at very high gains ranging from 4 to 6 x 10^5. The extrapolation to CMS conditions showed that discharge probability of less than 10^{-11} is expected for minimum ionizing particles (MIPs) in typical CMS operating conditions.

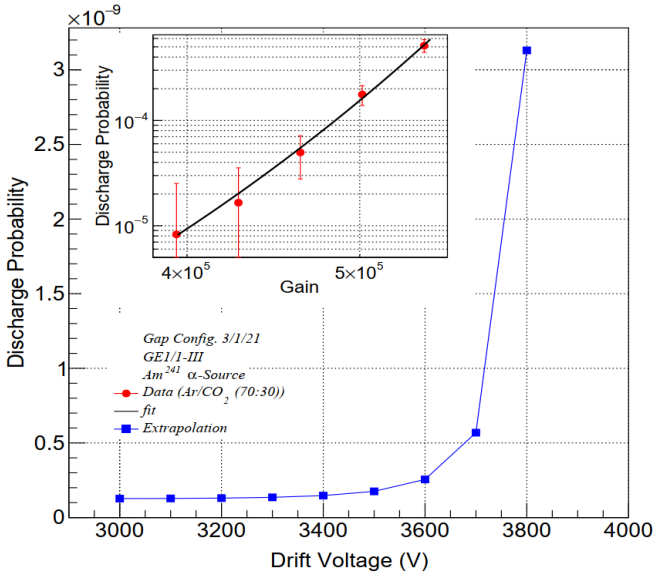
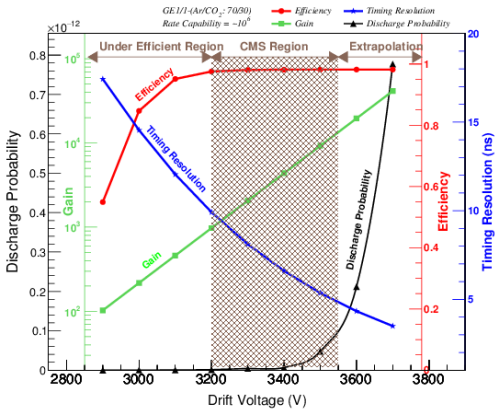


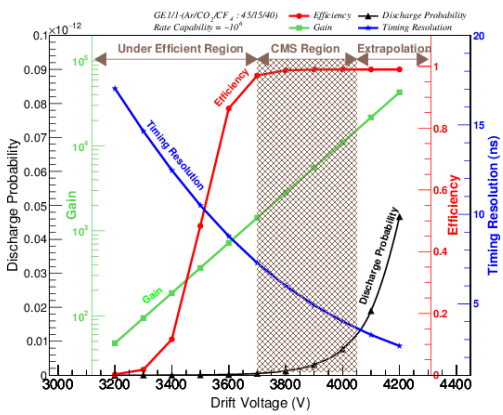
Figure 2.20: GE1/1-III discharge probability for Ar/CO_2 (70/30) as a function of drift voltage [32].

2.10.6 Optimum GE1/1 operating conditions

Several GE1/1 prototype generations of detectors were tested to find optimum timing resolution values, efficiency, gain, and discharge probability in CMS conditions. Two master plots are shown in Figure 2.21a and 2.21b, defining "under efficient", "CMS" and "extrapolation region" of detector operation with Ar/CO_2 and $Ar/CO_2/CF_4$ gas mixtures.



(a) GE1/1 Master performance plot showing gain (green), discharge probability (black), efficiency(red), and timing resolution (blue) for gas composition Ar/CO_2 as a function of GEM drift voltage.



(b) GE1/1 Master performance plot showing gain (green), discharge probability (black), efficiency(red), and timing resolution (blue) for gas composition $Ar/CO_2/CF_4$ as a function of GEM drift voltage.

Figure 2.21: GE1/1 GEM detector master performance plots showing trade off between selection of different performance parameters [32].

The detector can be operated up to a gain of 10^5 with a minimal discharge probability of 10^{-11} and rate capability of 10^6 Hz under CMS operating conditions. The chambers' beam test revealed an efficiency of 98% or better across the active GEM area with a timing resolution better than 10 ns. The observed data are fitted with various functions, and results are tabulated in Table 2.2 for the Ar/CO_2 (70/30) gas mixture.

Description	Drift voltage (V)	Gain	Efficiency	Resolution (ns)	Rate Capability (kHz/cm^2)	Discharge Probability
Under efficient region	2900	1.02×10^2	0.54	17.42	10^5	2.36×10^{-17}
	3000	2.17×10^2	0.84	14.54	10^5	8.68×10^{-17}
	3100	4.60×10^2	0.95	12.04	10^5	3.18×10^{-16}
	3200	9.74×10^2	0.97	9.912	10^5	1.16×10^{-15}
	3300	2.06×10^2	0.98	8.109	10^5	4.28×10^{-15}
CMS region	3400	4.36×10^2	0.98	6.60	10^5	1.57×10^{-14}
	3500	9.24×10^2	0.98	5.35	10^5	5.77×10^{-14}
	3600	1.95×10^2	0.98	4.32	10^5	2.11×10^{-13}
	3700	4.14×10^2	0.98	3.48	10^5	7.77×10^{-13}
Extrapolation region	3800	8.76×10^2	0.98	2.80	10^5	2.85×10^{-12}
	3900	1.85×10^2	0.98	2.25	10^5	1.00×10^{-11}
	4000	3.93×10^2	0.98	1.80	10^5	3.84×10^{-11}
	4100	8.31×10^2	0.98	1.44	10^5	1.40×10^{-10}

Table 2.2: GE1/1 performance parameters as a function of drift Voltage with Ar/CO_2 (70/30) gas mixture [32].

The plots show that 23 % better timing resolution is obtained with the same value of gas gain with the gas mixture of $Ar/CO_2/CF_4$ compared to a mixture of Ar/CO_2. Three different operational regions are defined and shown. The under-efficient region is not desirable as it reduces detector performance, and the extrapolation region must be avoided because of a sharp rise in discharge probability. The CMS region is the most suitable region to achieve optimum performance from the detector while keeping discharge probability low.

The GE1/1 GEM detectors will use the Ar/CO_2 gas mixtures with ~0.1 mm/ns of drift velocity through the gas volume. The use of this mixture leads to the most probable value (MPV) of charge per strip to be around ~4 fC with an average signal spread of 60 ns. In order to contribute to the level-1 trigger, the timing resolution of a single GEM should be better than 10 ns, which is reached with a drift voltage of 3.2 kV as shown in Figure 2.21

2.11 GE1/1 electronics

The concept of the GEM electronics is based on the use of common electronics components from CMS and the LHC groups to limit the custom development of specialized devices dedicated to the GEM project.

2.11.1 LHC & CMS common electronics

Every particle physics detector in an accelerator environment, especially LHC detector systems, needs to transmit particle detection information from the detectors to the back-end control room. Three kinds of electronics subsystems are required to implement the full chain of detector electronics. The first is the fast timing distribution system responsible for distributing the clock and fast trigger requests from the control room to the front-end readout chips. It also includes

fast signals from the detector to the control room for quick critical decisions. The second subsystem consists of particle detection hit and tracking data from the front-end ASICs to the back-end electronics. The third subsystem consists of a slow control two-way detector configuration data bus used to configure the detectors before data is taken in the beam.

For LHC upgrades, the GBT framework [40] provides a communication system between the front-end ASICS and the back-end electronics to all LHC experiments, combining these three functionalities. The Versatile link, a radiation hard, high-speed optical link designed for typical LHC applications, can be combined with the GBT chipsets to securely transmit data streams and control information from front-end detectors. A Versatile link project is a set of dedicated fiber optic cables and high-speed optical transceivers specially designed for LHC experiments. A typical LHC particle detector electronic system implementation and the GBT chipset and versatile link optical transceivers are shown in Figure 2.22.

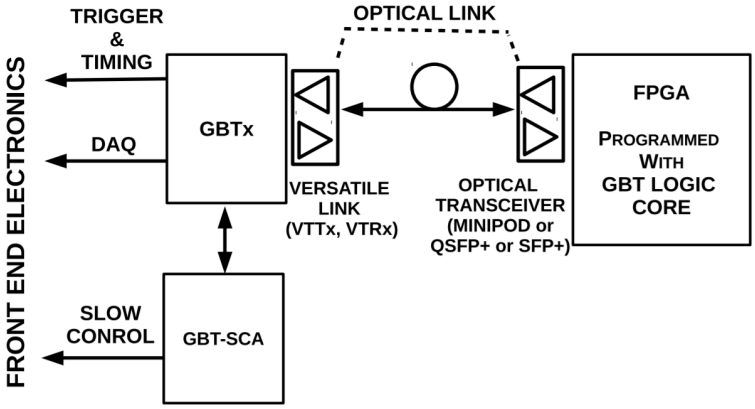


Figure 2.22: LHC detector electronics system using GBT chipset and Versatile link components [41].

The GBT project consists of four radiation-tolerant chipsets:

- GBTIA: a Transimpedance optical receiver,
- GBLD: a Laser driver
- GBTX: A Data and Timing Transceiver, and
- GBT-SCA: used for Slow control communication

The Versatile link subsystem consists of a VTRx transceiver located inside the front-end detector electronics, the back-end counterpart in the off-detector counting room, and passive optical fiber cables with dedicated connectors.

LHC has also chosen a common back-end electronics standard for its experiments. These are MicroTCA (μTCA), and Advanced TCA (ATCA) modular electronics standards, which have been adopted as the common platforms for many current and future upgrades of CMS off-detector systems [42, 43].

2.11.2 GE1/1 electronics overview

Since one of the main objectives of the GE1/1 detector is to improve the muon triggering capability and compensate for the loss of efficiency of existing cathode strip chambers (CSC), a dedicated trigger link has been implemented between GE1/1 on-detector trigger electronics and the CSC trigger system [44].

The GE1/1 system is expected to sustain a relatively high hadron flux in the range of a few kHz/cm^2, so only radiation-hardened electronics can be integrated directly on the detector and must sustain a total ionizing dose (TID) of several krad.

Therefore, the GE1/1 electronic system is subdivided into two kinds of electronic subsystems: "on-detector" electronics and "off-detector" electronics. A simplified block diagram of the GEM electronics system is shown in Figure 2.23.

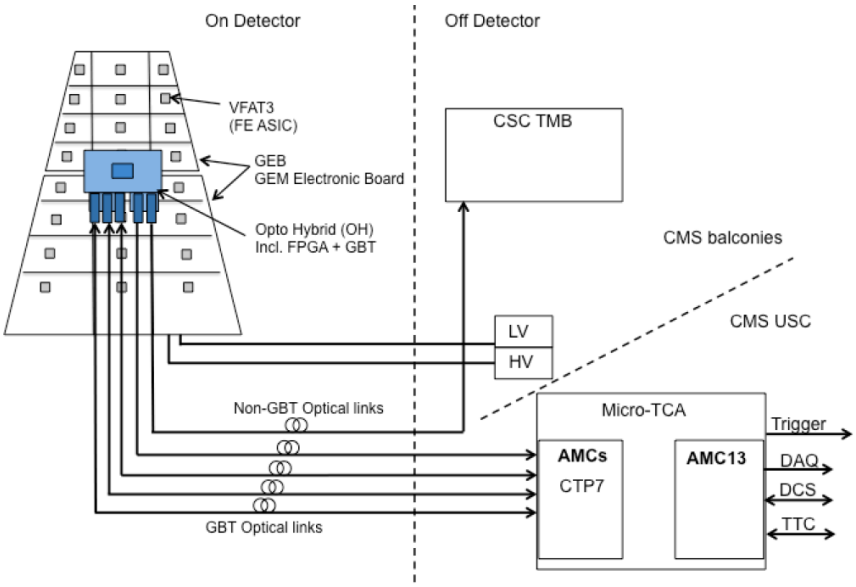


Figure 2.23: GE1/1 electronics and data acquisition system architecture [44].

The front-end electronics uses specifically designed radiation-tolerant ASICS. In contrast, back-end electronics located within the safety of the CMS service caverns include Commercial off-the-shelf (COTS) electronics components and modules. Both the front-end and back-end electronics will be discussed separately in the following sections.

2.11.3 GE1/1 Front-end electronics

The GE1/1 "On-detector" electronics' primary responsibility is to provide an accurate muon trigger and tracking information. In the TOTEM experiment [45], GEM detectors were already successfully used to provide trigger and tracking information. A readout ASIC, named VFAT2, was used as a 128-channel charge readout for GEM detectors. Consequently, the VFAT2 architecture is adopted as a baseline for the new front-end ASIC, the VFAT3 developed for CMS muon endcap GEM detectors. It is essential to mention that VFAT3 is a new design with many new functional and architectural improvements over its predecessor,

VFAT2. Figure 2.24 shows a GEM detector fully equipped with its front-end electronics including 24 VFAT3 chips.

Figure 2.24: GE1/1 detector fully equipped with front-end electronics. In the middle, an Optohybrid board is mounted which communicates with all 24 VFAT3 hybrids through a large splitted GEB boards.

As shown in section 2.9, Figure 2.13, the readout plane is divided into 24 sectors, each having 128 anode strips. Figure 2.25 shows a cross-section of connectivity between front-end hybrid and the GEM detector. A large electronics board, called GEM Electronics Board (GEB), is installed at the bottom of the GEM readout board, having 24 cut slots for the readout board to front-end hybrid connections. One end of each VFAT3 hybrid is connected to the GEM readout board

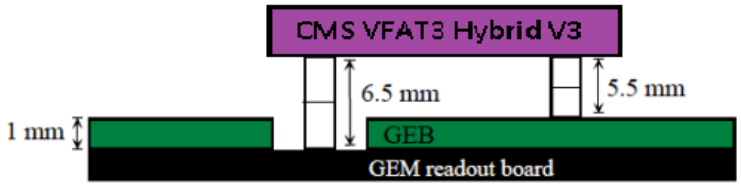


Figure 2.25: Cross-section of the readout board, GEB and hybrid assembly for GE1/1 detector.

connector, and the other end is connected to the GEB side 100-pin digital connector. One VFAT3 is used to read a sector of 128 strips. VFAT3 has two data paths: a fixed latency path for the trigger data and a variable latency path for the full granularity tracking data. Both data streams are sent to an Opto-hybrid concentrator card, situated in the middle of the two GEB sub-modules. Figure 2.26 shows a GEM Opto-hybrid concentrator module. Each Optohybrid has on-board radiation-hard Gigabit transceivers (GBT) [46] which handle tracking data and configuration of the front-end chips. The GBT uses bidirectional Versatile-links at 4.8 Gbps to transmit the data through optical fibers to the back-end crates. The VFAT3 operates at a 320 MHz master clock. The device's communication port is directly interfaced with GBT using a dedicated low voltage signaling (SLVS) differential standard, having a common mode of 600 mV. At 320 MHz, the bandwidth limits the number of VFAT3 to 10 per transceiver, so three GBTs are required to transmit the data from 24 VFATs mounted on one GE1/1 detector.

The trigger data in GE1/1 is transmitted to μTCA back-end electronics. A dedicated optical link is also provided to split the data to a CSC trigger processor named Trigger Mother Board (TMB), where it is combined with CSC trigger data

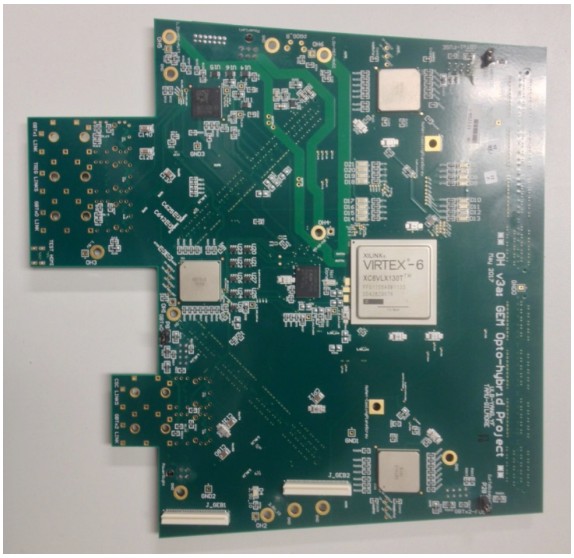


Figure 2.26: GE1/1 Optohybrid version-3

to improve the Level-1 trigger efficiency of the existing CSC trigger subsystem. Here, one remarkable difference from the standard LHC and GBT data flow (see Figure 2.22) is the use of a Xilinx Virtex-6 FPGA, which concentrates the trigger data coming from all 24 VFATs. The use of the FPGA instead of GBT is due to the constraint of using existing optical fibers to the CSC TMB, which can not handle GBT transmission protocol. The FPGA performs all the multiplexing, formating, zero suppression, and data transmission to CSC and micro-TCA back-end electronics. The SEU tests of the FPGA have been done [47] and extrapolations to the HL-LHC conditions foresee 9 SEUs/day. SEU mitigation strategies are also implemented and reported there for CMS operational runs.

2.11.4 GE1/1 back-end electronics

The GE1/1 back-end electronics provides a fast low latency interface between front-end electronics and CMS DAQ, TTC (timing, trigger & control) systems [48]. The off-detector electronics system is based on micro-TCA (μTCA) standard (adopted by CERN). μTCA is a hot-swappable, high-speed, compact standard with a high-speed serial data transfer backplane. It replaced the CERN VME standard and is adopted for HL-LHC upgrades as well. A block diagram of the CMS GEM 'Off-detector' electronics is shown in Figure 2.27.

A μTCA crate supports 12 dual-slot AMC modules and 2 μTCA carrier hub (MCH) modules. The first MCH1 slot houses a commercial MCH module used for standard gigabit ethernet communication and Intelligent Platform Management Interface (IPMI) control [44]. The second MCH2 slot contains a custom AMC13 board. The AMC13 is a standard module in CMS which interfaces μTCA crates to the CMS data acquisition system and also provides the CMS trigger Timing and Control (TTC) signals downlink [49] (see Figure 2.28b).

The bandwidth provided by 12 CTP7 (Calorimeter Trigger Processing) AMC boards (one μTCA crate) is sufficient to interface with entire GE1/1 GEM front-end electronics. Figure 2.28a shows a CTP7 featuring a Xilinx Virtex-7 FPGA with Multi-Gigabit Transceivers (MGT) supporting up to 10 Gb/s.

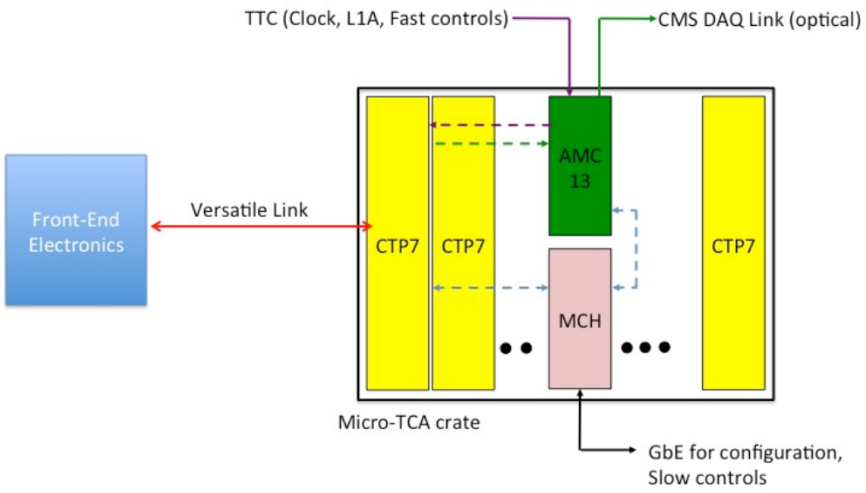
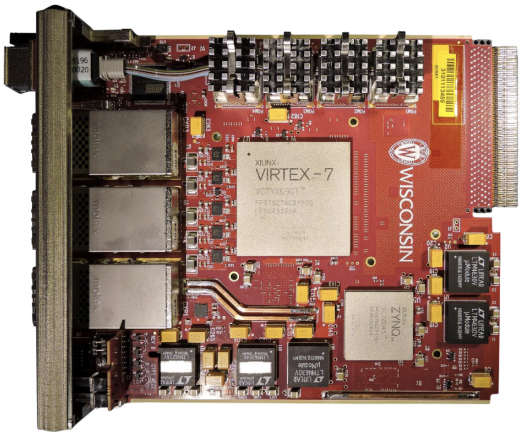
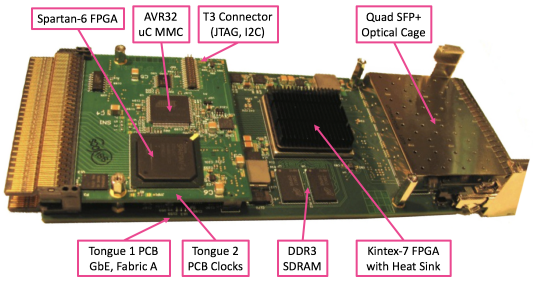


Figure 2.27: Layout of backend electronics for CMS GEM detector [44].



(a) Calorimeter Trigger Processing (CTP7) card [50]



(b) Photo of an AMC13 card [49]

Figure 2.28: CTP7 and AMC13 cards used for data processing in CMS GEM backend electronics

The CTP7 board was originally designed for, as the name suggests, the calorimeter trigger, which was further upgraded to handle the higher center-of-mass energy and pile-up that would be present after phase-2 upgrades [50]. However, the functionality of the CTP7 would conveniently fulfill the CMS GE1/1 backend processing requirements, so this card was adopted as the GE1/1 AMC card.

2.12 Summary

This chapter introduced the GEM detector technology, invented by Fabio Sauli in 1997 at CERN. As a part of the phase-2 CMS muon endcap upgrade, the first of three planned GEM stations, the GE1/1 GEM detector, has been installed during LS-2 (2018-2021). The addition of the GE1/1 detector in the current muon system will improve the muon track momentum resolution and increase the path

length traversed by muons within the first muon station by a factor of 2.4 - 3.5 over that of the 6 layers of the CSC ME1/1 hits alone. Secondly, the fabrication and operating conditions of the world's largest active area GEM detector, GE1/1, were shown. Then, the performance parameters of the GE1/1 detector were discussed, including detector gain, efficiency, timing resolution, rate capability, and discharge probability of the GE1/1 detector. Regarding detector gain, it was shown that the orientation of single mask GEM foil increases the effective detector gain. The narrow side of holes faces incident radiation, which produces higher gains has now become CMS preferred orientation. Over 98% of efficiency was observed as a function of drift voltage. A time resolution suitable for CMS applications, better than 10 ns, was achieved for both gas mixtures, Ar/CO2 (70/30) and $Ar/CO_2/CF_4$ (45/15/40). It is 24 % better with CF4; however, Ar/CO_2 (70/30) has been finally chosen as it provides good enough time resolution for CMS while it is environment friendly. The discharge probability of less than 10^{-11} was executed for minimum ionizing particles (MIPs) in typical CMS operating conditions. Finally, it was discussed that GE1/1 electronics is based on the common LHC detector electronics system development, composed of radiation-hard GBT chipset and Versatile link components.

Chapter 3

The VFAT3 architecture

3.1 Introduction

VFAT3 is a front-end ASIC explicitly designed for the readout of GEM detectors for the upgrade of the CMS experiment. The chip, made with the 130 nm commercial TSMC technology [51], consists of 128 concurrent analog channels composed of a charge-sensitive amplifier, a shaping network, and a constant fraction discriminator. A dedicated calibration, bias, and monitoring (CBM) block is embedded in the chip to configure the analog front-end. It provides in-system calibration of the chip during device operation in the CMS experiment. VFAT3 is produced in volumes into two different versions: one with standard input ESD protections provided by the foundry and the other with additional protection diodes to protect the input channels from rare discharges that can happen in GEM detectors. A block diagram of the VFAT3 ASIC is shown in Figure 3.1.

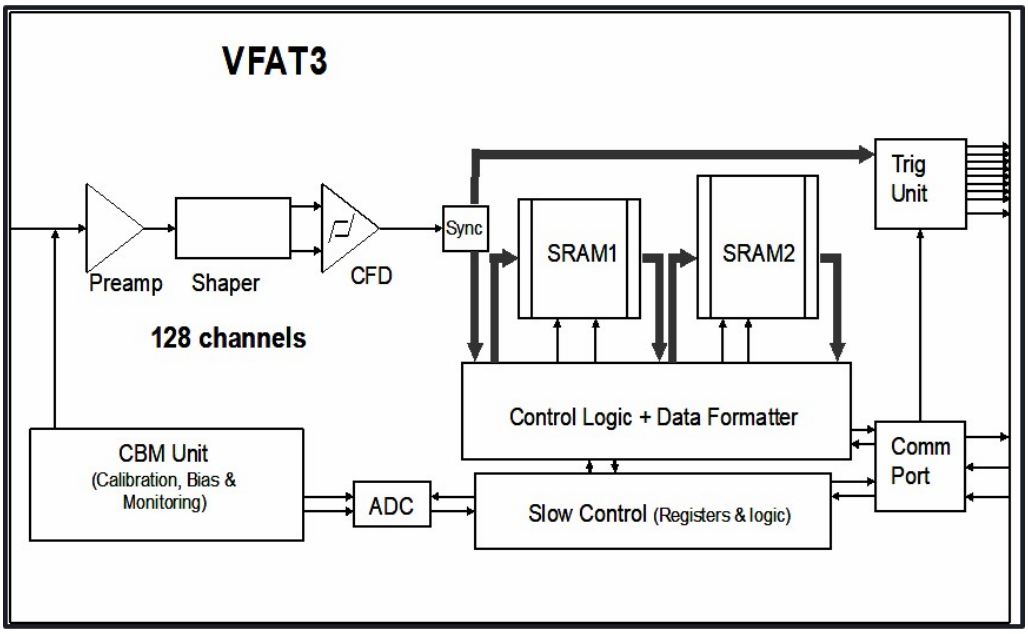


Figure 3.1: VFAT3 block diagram. [51]

Once properly biased and configured by the CBM, the VFAT3 front-end channel processes any fast GEM-like signal and produces a binary digital pulse at

the CFD output. A "sync" block then splits the signal in parallel towards trigger and tracking blocks. The trigger block transmits the fast data with fixed latency on dedicated trigger lines at each LHC bunch crossing clock frequency of 40MHz. The control logic and data formatter blocks attach the time tags and error correction checks to form the data packets and stores the packets in 1024-level internal deep memory. Upon request of a level-1 trigger, only the requested stored packet is transferred to the next 512-deep FIFO memory, which transmits the packet through a serial communication port (V3CP) out of the chip.

This chapter will describe some of the VFAT3 design features and functionalities as well as specifications which are relevant for this thesis work. First some features of the Triple-GEM signals will be reminded as they directly impacted many VFAT3 design choices.

3.2 Design for the GEM signal charge

The signal charge from a GEM detector has statistical randomness in its form, shown in Figure 3.2. The duration of the signal depends on the physical dimensions of the different GEM regions, and the drift velocity of the electrons [52]. The randomness of the signal shape is due to clusters of ionization occurring along the particle track. The signal shape is lumpy and unpredictable, thought to be due to clusters of ionization occurring along the particle track in the drift region. The addition of quenching gases such as CF_4 or CO_2 helps increase the number of clusters and reduce lumpiness [53].

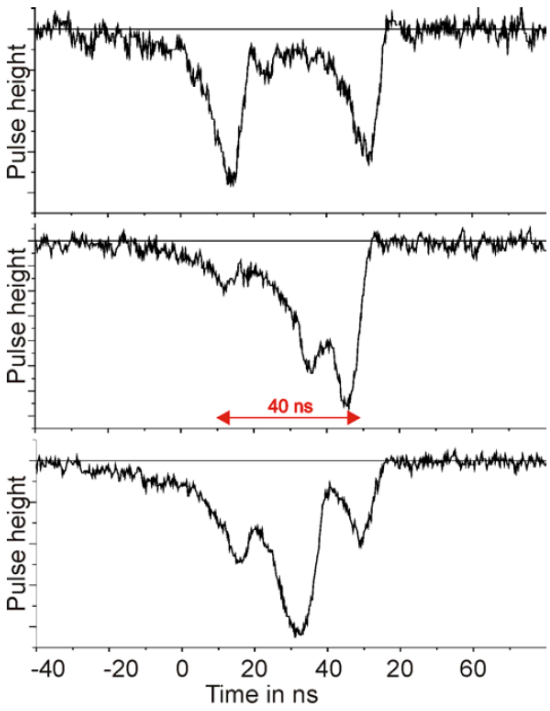


Figure 3.2: Typical signal forms recorded from three crossing particles [53].

To read-out GEM signals in a large variety of detector geometries (gas gap and anode sizes), and of gas mixtures, the VFAT3 chip has been designed with a

high degree of flexibility. VFAT3 has programmable shaping times and gains and can support detector capacitance up to 120 pF. Two additional key features of the VFAT3 are to provide a good timing resolution (typically better than 10 ns) and to provide a high rate capability per channel (up to 1 MHz per channel).

3.3 VFAT3 Specifications

The VFAT3 ASIC is designed under a wide range of design specifications required by the GEM detectors technology and CMS trigger and tracking conformances. In CMS, the distribution of the charge released by high momentum muons has a most probable value of ∼4 fC, and a long tail up ∼100 fC [54]. With Ar-CO_2 70-30% gas mixture, the CMS GEM signals are 40 – 60 ns long. The CMS trigger system imposes a Level-1 latency of 12.5 µs (see section 1.8) and a Level-1 accept rate up to 0.75 MHz. In addition to correctly identify the muons with the LHC bunch crossing, the CMS GEM detector should have a time resolution better than 10 ns. The GEM detectors in different regions of the CMS muon endcap should sustain varying levels of radiation and particle fluxes, which also poses a wide range of conflicting design demands for the front-end ASIC. The maximum integrated dose in ME0 amounts to 1 Mrad. Finally, depending on the CMS GEM station and the position along the detector, the VFAT3 should also be able to work with slightly different input detector capacitance, typically within the range 15-25 pF. The list of crucial design specifications for the front-end ASIC is tabulated in table 3.1, showing minimum required parameters for CMS versus final adopted for chip design.

3.4 VFAT3 analog front-end architecture

VFAT3 analog front-end is designed in TSMC-130 nm CMOS technology. It comprises 128 concurrent low power and high-speed channels to capture the GEM detector charge. Every single channel consists of a preamplifier, a shaper, and a single-to-differential stage followed by a Constant Fraction Discriminator (CFD) Comparator, where the signal is transformed from analog to discrete binary pulses. A front-end channel is shown in Figure 3.3. A charge pulse generated by the GEM detector is injected in the preamplifier input, which converts the current pulse to a voltage pulse with a high gain.

The signal then enters a shaper stage where pulse shaping is performed. Finally, a single-to-differential stage is added to convert the single-ended signal into bipolar to reduce the noise and make compatibility with the next comparator stage, where the analog signal is digitized into binary information. The detailed architecture of each analog stage is described in the following sections.

3.4.1 Preamplifier

The preamplifier consists of a high gain amplifier (HGA), which is based on regulated cascode architecture [55]. Programmable feedback capacitor C_f and resistor R_f banks are used to vary the preamplifier gain settings. A slow feedback

Feature	Minimum Required for CMS	Adopted Design Specification
No of channels	128	129 incl. test channel
Signal charge polarity	Negative	Both , suitable for silicon and gaseous detectors
Programmable gain	Yes	Low, Medium and High
Programmable shaping time	Yes	25ns, 50ns, 75ns, 100ns
Comparator	Yes	Arming + CFD
Rate per channel	1MHz	Up to 2MHz
Trigger path granularity	Fast OR of 2 channels 320Mbps	Fast OR of 2 channels 320Mbps Full granularity, DDR 640Mbps
Data Path: LV1A Latency Programmability	up to 12.5μs	25ns to 25.6 μs
Consecutive triggers	Yes	Allows multiple time slot readout per LV1A
Max LV1A rate	0.75MHz	Up to 2MHz
Zero suppression	Yes	Many options for ZS in the data packet Used to increase trigger rates beyond 2MHz
Directly compatible with GBTx and LpGBT	Yes	Yes
Calibration, bias and monitoring	Integrated	Integrated
Channel Threshold trimming	Yes	Yes
Temperature measurement	Yes	Internal & external temperature measurement read through slow control
Radiation tolerance	Ionising SEE	Up to 10s of Mrads, Triplication and SEL tolerance design

Table 3.1: Key VFAT3 design specifications [51].

amplifier is also added to correct the output DC level. The architecture of the preamplifier is shown in Figure 3.4.

The cascode amplifier used in the HGA provided high input-output isolation, high input impedance, and high bandwidth. The only disadvantage of the cascode amplifier is that it requires two transistors for the implementation, which is not an issue nowadays with the advent of modern 130 nm technology, which provides plenty of low supply voltage transistors. The HGA provided 90 dB open-loop gain and achieved a gain-bandwidth product (GBP) of 1.5GHz. The vital parameters of the preamplifier are tabulated in Table 3.2.

The phase margin of the preamplifier depends on the input capacitance. Simulations showed a phase margin of 95° at 0 pF detector capacitance, which drops

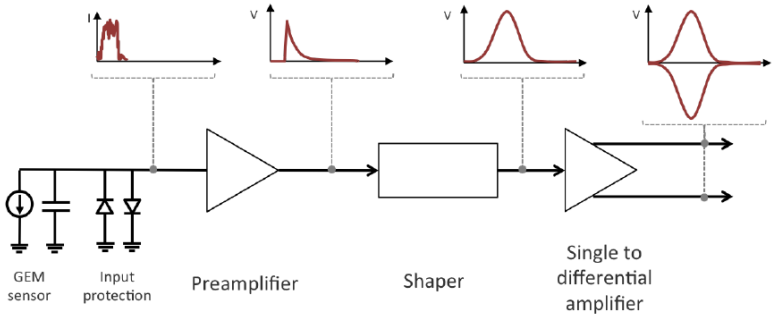


Figure 3.3: The VFAT3 analog-input channel [55].

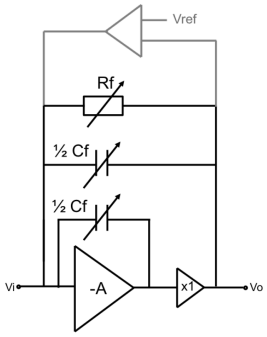


Figure 3.4: Architecture of the VFAT3 preamplifer stage [55].

C_f	120, 360, 720 [fF]
τ_{CR}	12.5 - 50 [ns]
signal-gain	6, 2, 1 [mV/fC]
power	606 μW

Table 3.2: preamplifier key parameters.

to 55° at 100 pF of detector capacitance. The positive phase margin rules out the possibility of unwanted system oscillations in the preamplifier, even with larger GEM detector capacitances up to 100pF. The size of the input transistor is also optimized for a nominal detector capacitance of 20 pF. The radiation tolerance of the transistors is increased by the use of an Enclosed Layout Transistor (ELT) configuration of the transistors. The preamplifier design is low power, consuming 450 μA of input current only. The overall preamplifier power consumption is only 606 μW.

An impulse response for different T_p for preamp stage is shown in Figure 3.5.

The plot shows a fast baseline restore in ∼50 ns for 25 ns peaking time. An increase in baseline restore time is observed at higher peaking times. The worst-case baseline recovery time is 250 ns at 100 ns peaking time. It shows that the minimum pulse processing rate is 4 MHz at the highest-peaking time.

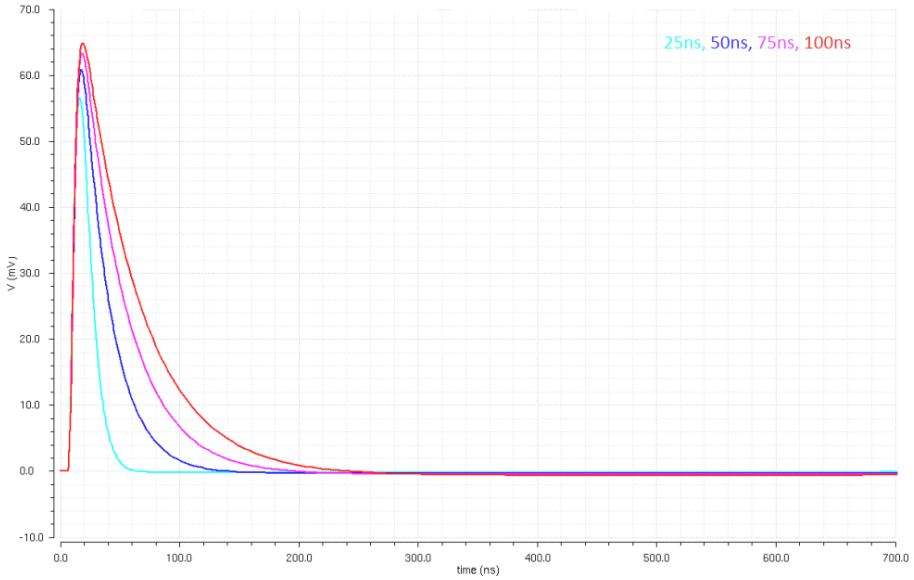


Figure 3.5: Preamplifier simulated impulse response for different T_p (High Gain, $C_d = 20pF$).

3.4.2 Shaper

The active RC filters have been widely used in various low-frequency application systems for a long time. However, active RC filters cannot work properly at higher frequencies over 50MHz due to opamp frequency limitations [56]. These types of filters are not suitable for full integration of fast GEM signal.

An operational transconductance amplifier (OTA) circuit is realized for VFAT3 shaper implementation. The OTA architecture has two main advantages over RC-based filters: its transconductance is controlled by changing the external dc bias current or voltage, and it can work at high frequencies. A block diagram of a two-stage OTA-C low pass integrator-based shaper for VFAT3 front-end is shown in Figure 3.6.

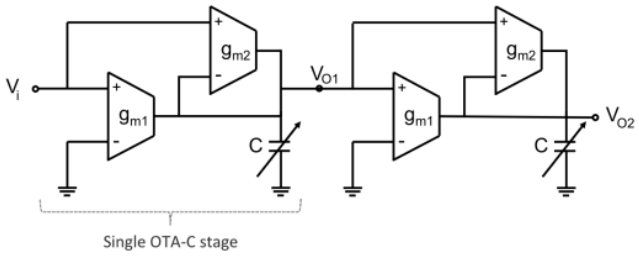


Figure 3.6: A two stage OTA-C based Shaper circuit [55].

Each integrator consists of two OTAs. The transfer function of single-stage OTA is given by equation 3.1.

$$\frac{V_0}{V_i} = (1 + \frac{g_{m1}}{g_{m2}}) \cdot \frac{1}{1 + s\frac{C}{g_{m2}}} \tag{3.1}$$

The time constant of a single stage is defined by the load capacitance at the output node of the integrator and the transconductance of one of the OTAs. In contrast,

the voltage gain is defined by the ratio of the transconductances of the OTAs.

The shaping time can be adjusted by programming switched capacitors at each stage. The total current consumption of the shaper is 200 (μA). A simulated impulse response of the shaper stage is shown in Figure 3.7.

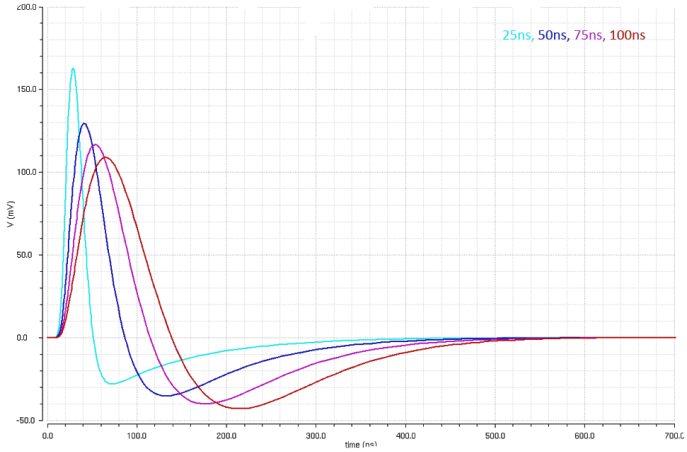


Figure 3.7: Simulation for the impulse response of the shaper.

The reduction in peak amplitude at higher shaping times is observed due to the ballistic deficit. The plot also shows that the baseline returns to normal within 500 ns. It shows that the shaper can process GEM pulses up to 2 MHz rates without any distortion. The CMS requirement is only up to 1 MHz, which is well below these limits (see table 3.1).

3.4.3 Single-to-differential Stage

The single-to-differential (SD) amplifier stage serves as an interface between the shaper and the constant fraction discriminator (CFD) in each front-end channel of the chip. SD stage converts the single-ended signal to a differential compatible with the VFAT3 CFD input stage. SD also provides further fixed amplification of the signal. This amplifier is based on a PMOS differential folded-cascode architecture, with resistive load and degeneration of the input pair. A block diagram of the stage is shown in Figure 3.8. The voltage gain of the SD is approximated by the load to degeneration resistance ratio and is 3.4 (V/V). The amplifier consumes only 50 (μA) and has a bandwidth of 210 MHz. A source-follower is also added at the output of the SD to drive the low-impedance of the CFD. A simulated impulse response of SD stage is shown in Figure 3.9.

The plot shows that the baseline returns to 0 mV before 500 ns. It shows that the SD stage can also process GEM pulses up to 2 MHz rates without any distortion. The CMS requirement is only 750 kHz, which is far below these limits.

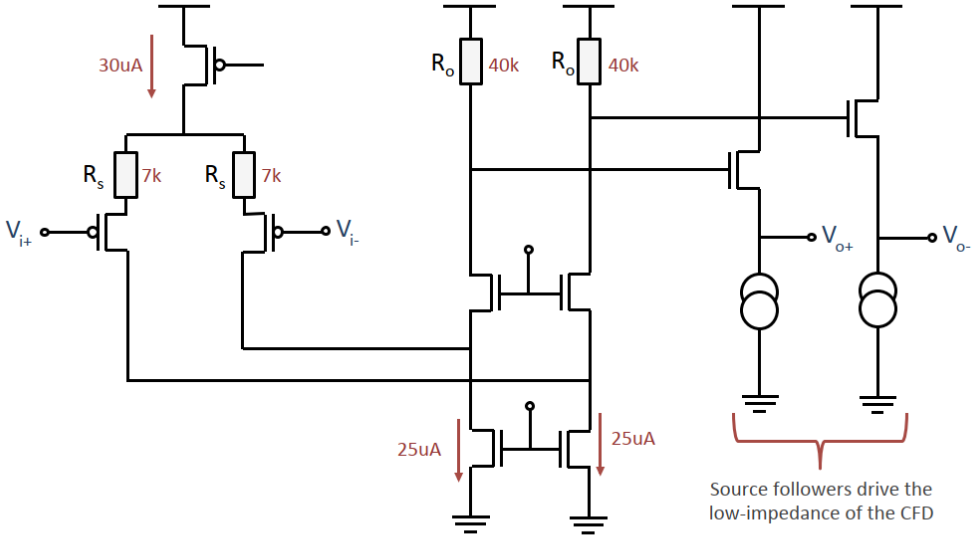


Figure 3.8: single-to-differential stage block diagram.

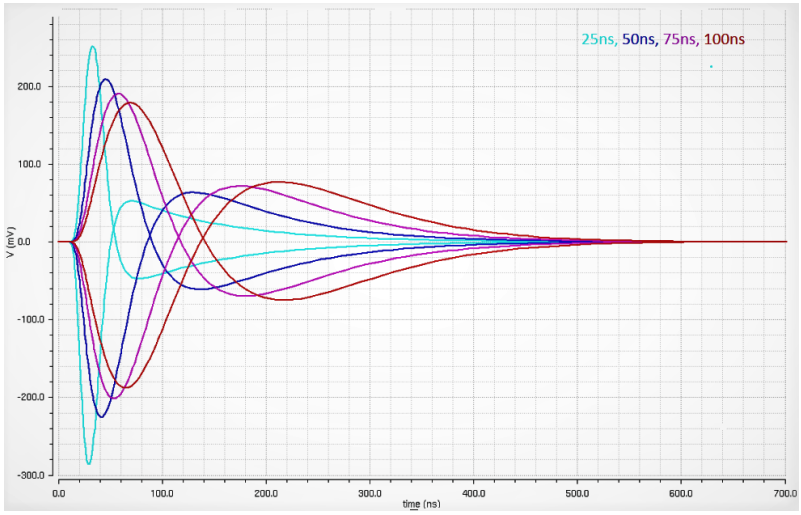


Figure 3.9: Simulation for the impulse response of the single to differential stage.

3.5 The Constant Fraction Discriminator (CFD)

A constant fraction discriminator (CFD) is an electronic circuit based on the mathematical operation of finding the maximum of a pulse by detecting the zero of its slope. This technique also provides amplitude-independent information about the arrival time of a signal. The principle of operation is based on detecting the zero-crossing of the bipolar pulse obtained by subtracting a fraction of the input signal from a delayed version of the original signal. The resultant bipolar signal always crosses zero at a fixed time regarding the start of the input pulse. The working principle of CFD is shown in Figure 3.10.

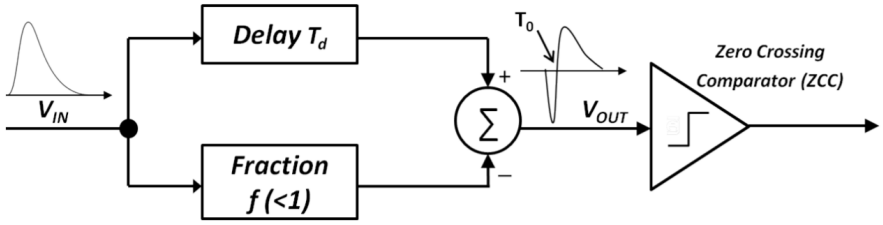


Figure 3.10: Principal of operation of a constant fraction discriminator. [57]

Mathematically, it can be represented as follows:

$$V_{out}(t) = V_{in}(t - T_d) - f * V_{in}(t) \tag{3.2}$$

In equation 3.2, the output bipolar signal V_{out} has a zero crossing time T_0 depending only on network parameters (T_d, f).

In VFAT3, the CFD implementation [57] is based on a fully differential architecture for better noise rejection. A block diagram of the VFAT3 differential CFD block is shown in Figure 3.11. The differential input signal from the SD stage enters a passive shaping network, which converts a differential signal to a bipolar signal that crosses the baseline independent of its amplitude.

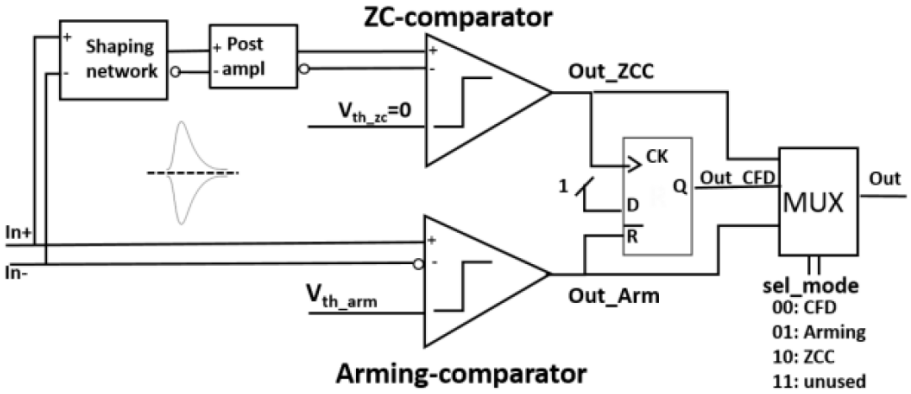


Figure 3.11: Block diagram of the differential CFD block used in VFAT3 [51].

The shaping-network is an implementation of equation 3.2. After the shaping network, a differential amplifier stage is added to compensate for the signal loss due to the attenuation within the shaping network. The amplified bipolar signal is then forwarded to a zero-crossing comparator (ZCC), which generates a digital pulse whenever its input signal crosses the baseline. A simple arming comparator stage is also added in parallel to provide the user control over CFD output by setting a threshold voltage (V_{th_arm}) through an 8-bit DAC at the arming comparator input. Finally, a user-selectable multiplexer is added to select either CFD or arming comparator output. Both arming and CFD outputs represent the presence of an input signal, which is above V_{th_arm} threshold. The only difference is the time walk compensation in the CFD output.

Following the comparator is a small synchronization stage that synchronizes CFD pulses to the LHC 40 MHz clock, which is discussed in Section 3.6.

3.6 Synchronization block

The asynchronous front-end pulses from the CFD block enter into a data "Synchronization and Pulse Stretching" block labeled as "Sync" in the block diagram of Figure 3.1. The asynchronous input signal is sampled and synchronized to an internal 40MHz clock, and then this data is split into trigger and tracking paths. A Pulse Stretching logic is used to stretch the output pulses from 1 to 8 clock periods. The stretching of the pulse is only available for the variable Latency path. The Fixed Latency path uses synchronized pulses of one clock period only. A schematic block diagram of the pulse stretching circuit is shown in Figure 3.12.

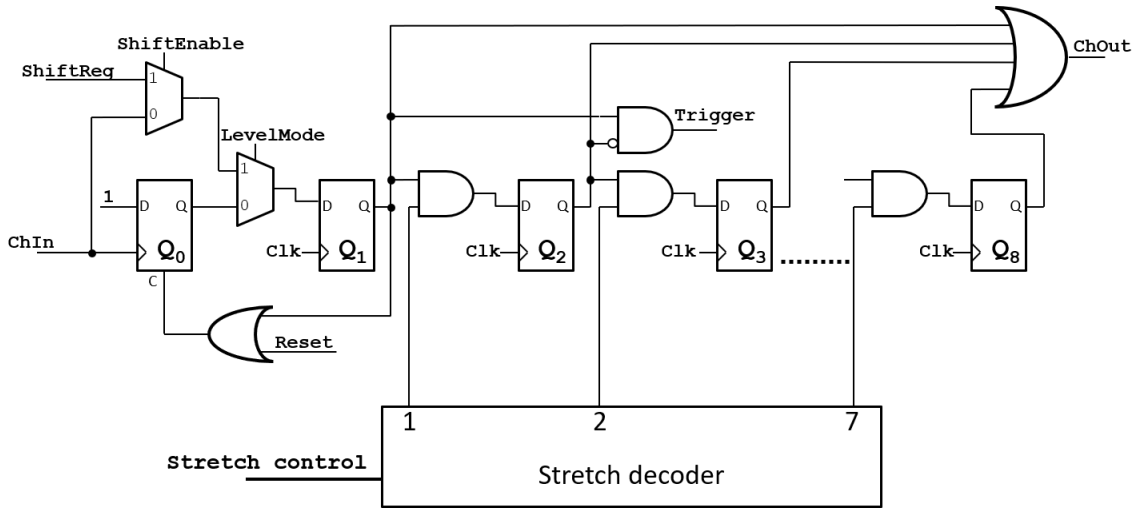


Figure 3.12: Block diagram of the synchronisation stage with pulse stretcher.

The "sync" block works in either "edge" or "level" mode [51]. In "edge" mode, the output pulse width is independent of CFD pulse width and is adjusted by a "PS" register up to 8 steps of 25 ns bunch crossings. In "level" mode, the width of the CFD pulses is sampled every clock cycle, and the "PS" pulse width is also added to the sampled width. If "N" is the width of the asynchronous CFD pulse, then the pulse width at the synchronizer output is $PS + N + 1$

3.7 Calibration, bias and monitoring block

In order to achieve the high programmability of the analog front-end channel, on-chip calibration, bias, and monitoring blocks are embedded inside the chip [58]. The main advantage of on-chip calibration is to perform in-situ calibration and response trimming. It also reduced the need for additional external components such as ADC and calibration DACs for the injection of external calibration pulses.

3.7.1 Calibration block

The calibration circuit can provide internal charge pulses either in voltage or in current mode. A block diagram of the calibration circuit is shown in Figure 3.13.

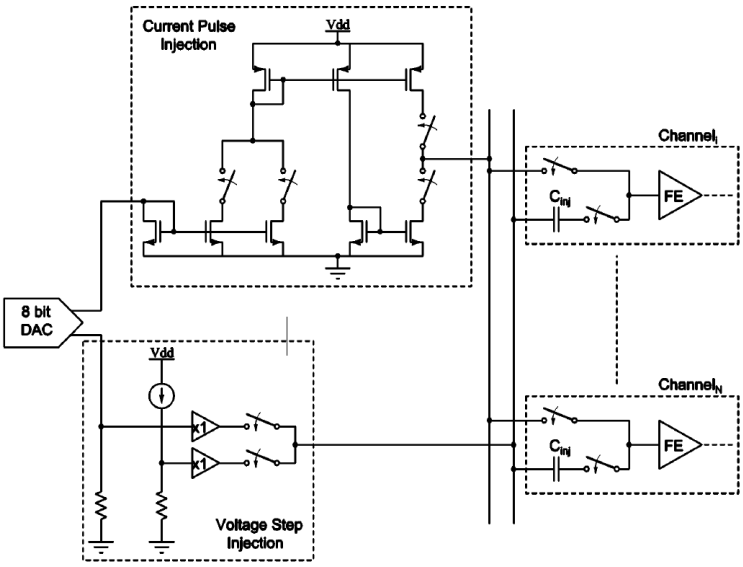


Figure 3.13: Architecture of the VFAT3 internal calibration circuit [58].

In the "Voltage Pulse" mode, a step is generated by an internal analog multiplexer circuit that switches between two different levels. Depending on the "polarity" settings, the circuit generates either a positive or negative pulse. This pulse is injected into an internal series capacitor of $1fF$, converting it to a charge pulse and injecting it into the analog channel. The injected charge ranges from $0fC$ to $63.75fC$ with an LSB of $0.25fC$.

The GEM-like current pulses can also be injected directly in the "Current Pulse" mode. The same 8-bit DAC can control the amplitude of the pulses, and pulse duration is programmable in steps of 25ns. The minimum charge pulse amplitude is 62.5 aC (1 fC = 1000 aC (atto Coulomb)) with an adjustable pulse width of up to 522 clock cycles.

3.7.2 Bias block

The response of each VFAT3 analog channel is slightly affected by process variations and transistor mismatches. Secondly, the channel response can also vary over time due to total ionizing dose (TID) effects in the device for long-term radiation exposure in CMS.

A programmable bias circuit is added to the chip to compensate for these device variations. This block consists of several 6 and 8 bits DACs, providing voltage and current references to achieve the expected analog response. A block diagram of this "Bias block" is shown in Figure 3.14

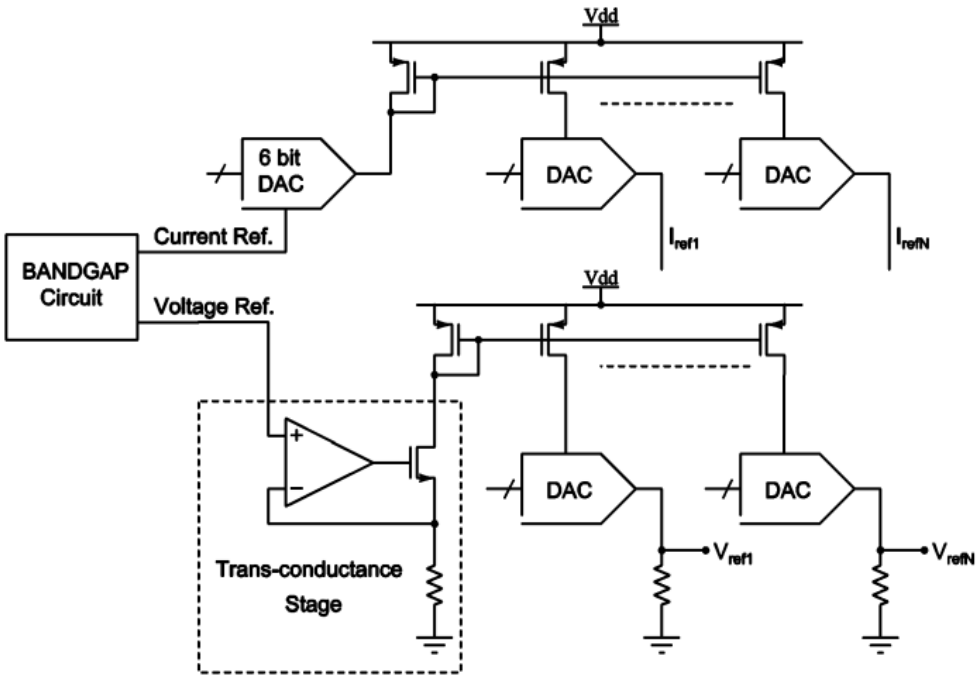


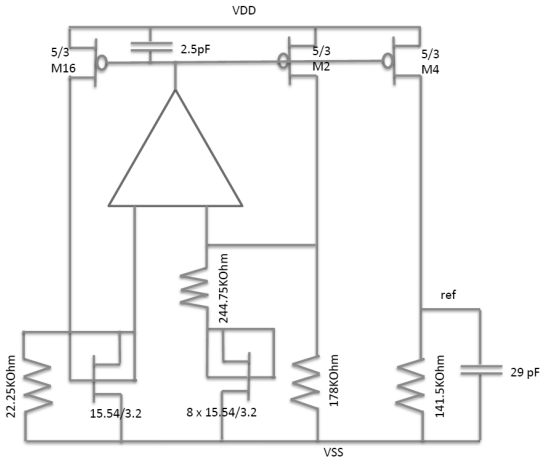
Figure 3.14: VFAT3 Bias circuit block diagram [58].

A bandgap circuit is used to generate stable voltage and current references independent of supply and temperature variations in the device. The bandgap circuit (see Figure 3.15a) provides a 350 mV reference voltage (VBG), converted into a current using a transconductance amplifier stage. Like all bandgap reference circuits, the principle is to generate two voltages: one proportional to absolute temperature (PTAT), one complementary to absolute temperature (CTAT). With proper dimensioning of currents and devices, the difference of those two voltages cancels the dependence on temperature. A temperature stability plot for the bandgap reference is shown in Figure 3.15b.

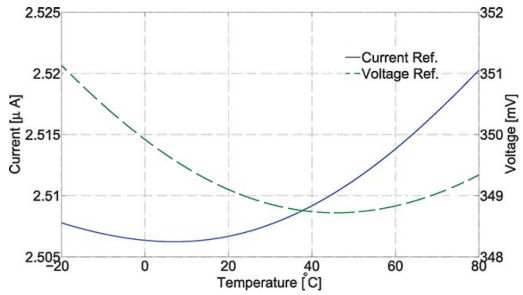
This plot shows that in a range between $-20°C$ and $80°C$, the maximum variation of both references is lower than 0.7% as compared to values at $27°C$. The transconductance amplifier is strongly process-dependent, and a 6-bit "IREF" DAC is also added to fine-tune and achieve a stable reference current. Several scaled and mirrored currents are generated with this "IREF" reference in the chip to achieve precise front-end biasing. The scaling is necessary to cover the actual current ranges for various DACs injecting currents at different nodes in the analog circuit.

3.7.3 Monitoring block

In order to monitor and adjust all the front-end biasing DACs, VFAT3 has 10-bit SAR ADC modules [59]. The SAR architecture was chosen because it has



(a) VFAT3 Bandgap circuit.



(b) VFAT3 Band gap temperature variation [58].

Figure 3.15: (Left) VFAT3 Band gap circuit, (right) VFAT3 Bandgap temperature variation.

negligible power consumption when not in use and can operate without a regular clock. The ADC power budget is in the range 32-37 fJ/conversion for sampling frequencies 10-40 MS/s.

Two instances of the same ADC are implemented within VFAT3; ADC0 and ADC1. ADC0 uses an internal reference derived from the bandgap, while ADC1 has an external reference of digital power rails. Figure 3.16 shows a block diagram of the monitoring block.

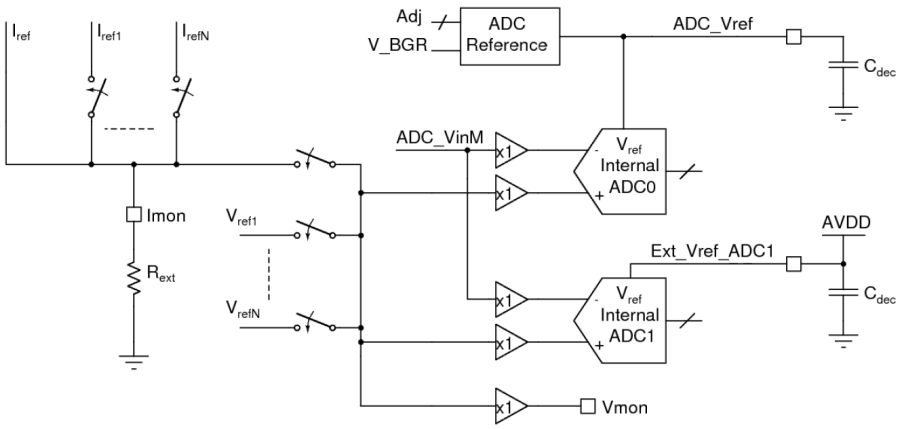


Figure 3.16: The monitoring circuitry, showing two internal ADCs with multiplexer switches to direct any desired DAC to external monitoring pin [58].

All internal reference current and voltage DACs are multiplexed toward an external pad where a precision R_{ext} resistor is mounted external to the chip. These current and voltages can be read through either an external precision ADC or by in-situ measurement by either of two internal ADCs are possible. The ADC0 internal reference (ADC_{V_ref}) is derived from the bandgap voltage V_{BGR} and can be adjusted by a 2-bit DAC in steps of 50mV to achieve 1V precise reference, which provides an LSB of 2mV.

3.8 VFAT3 communication Interface

3.8.1 Communication port

In the context of full GEM system integration in the CMS muon endcap, the key "on-detector" components of the electronics system are the VFAT3 and the Giga-Bit Transceiver (GBTX) [60], as shown in figure 3.17.

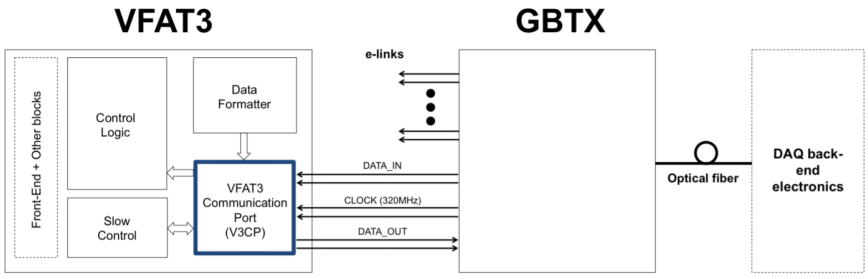


Figure 3.17: The connectivity between the VFAT3 chip and the GBTX chip in the CMS GEM Data-acquisition system [44].

The GBTX is a chipset for electro-optical reception and transmission of all data in and out of the multiple front-end ASICS supporting synchronous differential signaling. It has been developed as a common ASIC for use in many HL-LHC detector systems. A key design specification for the VFAT3 is to achieve direct compatibility with the GBTX through a VFAT3 Communication Port (V3CP). The V3CP is the communication port that connects directly to the GBTX [61], [44]. The main objective for the V3CP was to have a single port providing VFAT3 fast-control, high-speed channel readout, and bi-directional slow control configuration communications.

The V3CP operates with the differential e-links running at 320 Mbps. Several 8-bit fast serial codes are used to control the operation of the chip at an LHC bunch crossing frequency of 40MHz. The backend DAQ system can send synchronization, trigger, and several internal counters reset commands through these fast commands. A complete list of fast commands which can be sent to VFAT3 are tabulated in Table 3.3

Synchronization of the V3CP link is necessary before starting any other communication with the chip. This is achieved by sending three consecutive CC-A characters to the chip via V3CP. These characters are phase insensitive and not allowed in any other commands sent to the ASIC. After CC-A detection, an internally derived 40 MHz clock is phase-aligned to the LHC clock. Once synchronization is done, all other codes can be detected correctly by the chip. The synchronization phase can be seen in Figure 3.18.

The fast commands are used to control the operation of tracking data paths with extremely low latency mechanisms. For example, "LV1A" is used to send the trigger request, and "Calpulse" injects the internal calibration pulses into the selected channels. Time-tag counters can also be reset on receipt of "EC0" or "BC0" commands with options of sending several composite commands to reset several counters simultaneously.

Fast Command	8-bit represenatation	Function
EC0	00001111	Reset of Event Counter (EC)
BC0	00110011	Reset of Bunch-crossing Counter (BC)
CalPulse	00111100	Injection of calibration pulse
ReSync	01010101	Reset all VFAT3 state machines
SCOnly	01011010	Force "Slow control Only" Mode
RunMode	01100110	Return from "Slow control Only" Mode
LV1A	01101001	First level trigger
SC0	10010110	Sends "0" to the slow control
SC1	10011001	Sends "1" to the slow control
ReSC	10100101	Reset of Slow Control
LV1A + EC0	10101010	First Level Trigger and reset of the EC
LV1A + BC0	11000011	First Level Trigger and reset of the BC
LV1A + EC0 + BC0	11001100	First Level Trigger and reset of the EC and the BC
EC0 + BC0	11110000	Reset of EC and BC
CC-A	00010111	Sync character, needs to send 3 consecutive for sync
CC-B	11101000	Sync verify character

Table 3.3: List of the Fast Synchronous Control Commands (FSCCs) [51].

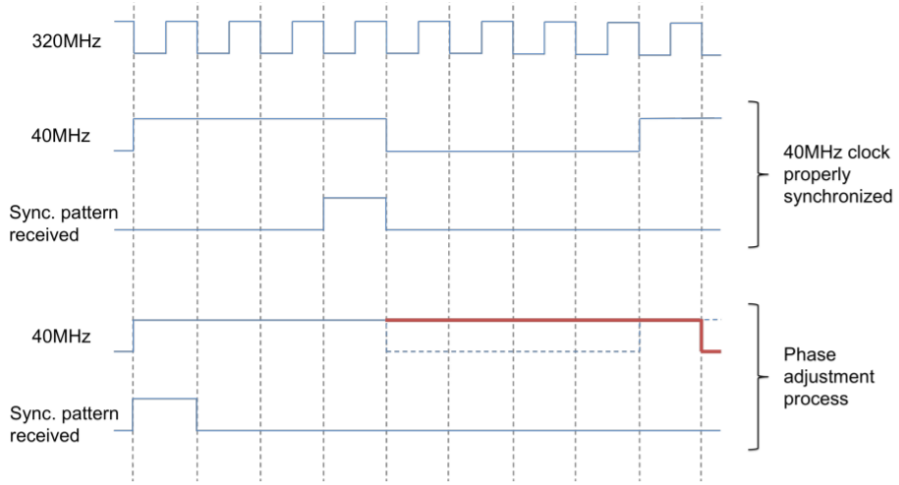


Figure 3.18: 1) Relation between the phase of the 40 MHz clocks and the reception of the synchronization characters. 2) The phase adjustment of 40 MHz clock [61].

The slow control communication is done by using only two control characters, "SC0" and "SC1," which represent a logic "1" and "0," respectively. Each of the slow control bits (SC0 and SC1) contain 8-bits at 320 MHz, it follows that each slow control bit is communicated at 40 MHz.

A priority system is implemented in the V3CP to avoid conflict between slow-control tracking data commands. The data packet transmission and fast commands have priority over slow-control unless "SC Only" is sent to switch the default priority to slow-control. The return to normal priority is done by sending a "Run Mode" command.

3.8.2 VFAT3 Data-out formats

The data transmission from VFAT3 is continually active by transmitting IDLE characters in a toggling state during "Idle" periods. In Slow Control communication, the returning characters are also SC0 and SC1 to indicate slow control logic

Fast Command	8-bit represenatation	Function
SC0	1001 0110	Slow Control "0"
SC1	1001 1001	Slow Control "1"
F1	0111 1110	IDLE character 1
F2	1000 0001	IDLE character 2
SyncAck	0101 1010	Synchronization Acknowledge
VerifAck	0110 0110	Verification Acknowlwdge

Table 3.4: List of the Fast Synchronous Control Commands (FSCCs) [51].

"0" and "1," respectively. The SyncAck and SyncVerifAck codes are returned after the reception of successful synchronization codes or a request for SyncVerify commands, respectively. These return codes are tabulated in the table 3.4 below.

A data priority system is implemented in the V3CP. In the default configuration, the channel data through the tracking path has priority over slow control transmission. On receiving an "LV1A" trigger fast-command, VFAT3 sends data packets containing channel information at the corresponding bunch crossing over the dataOut lines. An illustration of the data packet format can be seen in Figure 3.19.

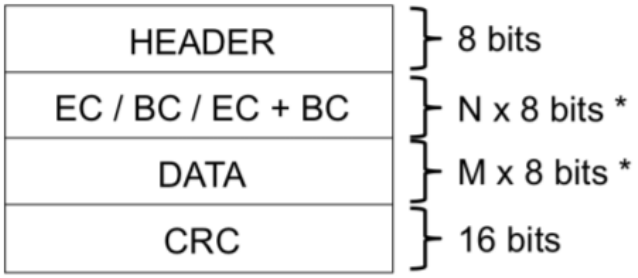


Figure 3.19: VFAT3 tracking data packet format [61].

Each data packet starts with a header byte, followed by time tag counters, channel binary data, and a CRC checksum for error detection. The data packets are highly programmable in the content to achieve high bandwidth and trigger rates. VFAT3 uses four different headers in data packets, depending on the chosen configuration [51].

3.8.3 Slow Control Communication protocol

Communication with the slow control block is done by using only two codes, SC0 and SC1, already mentioned in the above Table 3.4. The bitstream for slow control communication is multiplexed inside the primary bitstream running at 320 Mbps to produce slow control communication at 40 MHz. Each SC0 or SC1 bit takes eight clock cycles at 320 MHz to transmit 1-bit information. An encoding scheme is also used to transmit the slow control data stream based on a subset of the High-Level Data Link Control (HDLC) protocol. The structure of the HDLC frame implemented in the VFAT3 is shown in Table 3.5.

8	8	8	Variable	16	8
FS	Address	Control	Payload	FCS	FS

Table 3.5: HDLC packet format. Each of the field is constructed by slow-control bits (SC0 & SC1) [51].

The HDLC packet starts and finishes with a unique 8-bit pattern of "0111 1110". This pattern contains six consecutive 1's and is not permitted in the rest of the data string. This is achieved by using a bit-stuffing technique which inserts an additional '0' whenever five or more consecutive 1's need to be transmitted. When it receives five consecutive 1's, the receiver block discards the next '0' to recover the original bitstream.

The next two bytes in the packet are a device address and a control byte. The address used in the first production hybrids is 0x00, and the control byte is always fixed to 0x03, defined by the HDLC standard. [62].

The "Payload" field in the packet contains IP-Bus command or response, which are used to read or write the individual VFAT3 slow-control registers.

The frame check sequence (FCS) field is a 16-bit CRC-CCIT standard checksum used to detect bit errors in the packet. The polynomial used to construct CRC is: $FCS = X^{16} + X^{12} + X^5 + 1$
This checksum is used only to detect single-bit errors in the slow control transactions. In the case of bit-error, the transaction needs to be repeated by the sender.

3.8.4 IPbus transactions

IP-bus is a secure and straightforward IP-based protocol used for controlling hardware devices by CERN backend μTCA/ATCA electronics [63]. It supports only fixed 32-bit addresses and data transactions. The IP-bus transaction explained in more detail in [64] starts with a header that contains a transaction ID, type ID, and Info code types of description about that particular transaction. The IP-bus header structure is shown in Figure 3.20.

31 28	27 16	15 8	7 4	3 0
Protocol Version (4 bits)	**Words** (12 bits)	**Transaction ID** (8 bits)	**Type ID** (4 bits)	**Info Code** (4 bits)

Figure 3.20: IP-bus packet header structure.

The "Protocol Version" is fixed for each version of the IP-bus. The "Word" field represents the number of 32-bit words which need to write or read in the current transaction space. The "Transaction ID" is added for the client/host to keep track of transaction numbers. The "type ID" defines if a particular transaction is either a request or response transaction. The "Info code" field defines the direction of a particular transaction, either read or write. This field also contains transaction error information, which describes if a particular transaction is terminated incorrectly or completed with errors.

3.9 VFAT3 radiation hardness

The VFAT3 is designed as a radiation-hard chip as its aim to be used in a harsh radiation environment. All the logic inside VFAT3 is implemented using Triple Modular Redundancy (TMR). Moreover, all flip-flops (FFs) outputs are voted using three independent voters, and outputs of three voters are feedback to the three FFs. The result is that for every clock cycle, FFs are updated with the corrected value. In total, two versions of VFAT3, named VFAT3a and VFAT3b, were fabricated. VFAT3a had two static RAMs that suffered from a single event latchup (SEL) will be discussed in chapter 5 in detail. The Velopix team at CERN reported this latchup right after VFAT3a had been submitted to the foundry. A single event upset test was performed by the CERN Velopix group, which used the same memory cells in their device [65]. They recommended the replacement of problematic SRAMs with a new robust design. VFAT3b was then produced, replacing the problematic SRAM blocks with more robust memory blocks.

3.10 Summary

VFAT3 is a fully custom ASIC explicitly designed for the front-end readout of CMS GEM detectors. It has been chosen as the only front-end readout of GEM chambers within the CMS experiment at CERN, foreseeing a 10-year operation during the high luminosity phase of the LHC.

The device has a highly programmable front-end with low noise levels of $600e^- + 30e^-/pF$. Front-end can be configured in three different gain settings and shaing times can be adjusted to desired charge read mode from 15, 25, 35 and 45 ns. The hit data is trasmitted with low latency to contribute in muon trigger. The tracking data can be stored in large onchip memory for up to 25.6 µs and can be provided on level-1 request. The VFAT3 communication protocol is compatible with the existing and future data acquisition formats of the CMS trigger and tracking electronic systems.

Chapter 4

VFAT3 functional characterization

4.1 Introduction

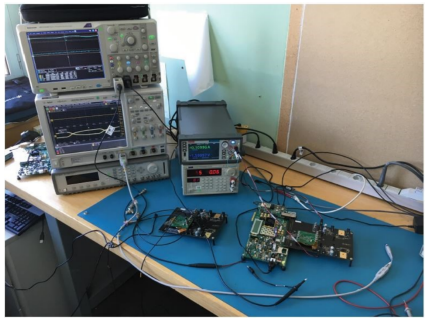
The adopted design strategy for VFAT3 was a full-chip design. In this approach, chip's internal modules were only simulated but no prototype chips with sub-functionalities were realized before full chip submission. This strategy saved design time and budget but contributed to the addition of extensive programmable, calibration and debug features inside the chip. This design strategy relies on the comprehensive and thorough characterization of the chip after production. The VFAT3 characterization also implies the validation of the on-chip calibration modules against external references. This was a crucial step before the VFAT3 could be operated with CMS GEM detectors and relied on the design of several test benches, including custom boards, firmware and hardware.

A custom verification platform has been designed to characterize the VFAT3 chip. The chapter begins with an explanation of the architecture of the verification platform. The design of test system for a complex chip like VFAT3 faced several design challenges like development of low noise PCBs with high speed sognals and impedance control circuits. The firmware also needed to be highly flexible with a lot of programmability options. These constraints led us to chose a classic system on chip (SoC) firmware design approach which works with a tight integration of a soft processor to provide desired flexibility and HDL modules to provide desired speed and test functions through a fast AXI bus system. After test system design, VFAT3 characterization procedures with detailed results are discussed, mentioning the suitability of the VFAT3 for phase-2 CMS GEM operation.

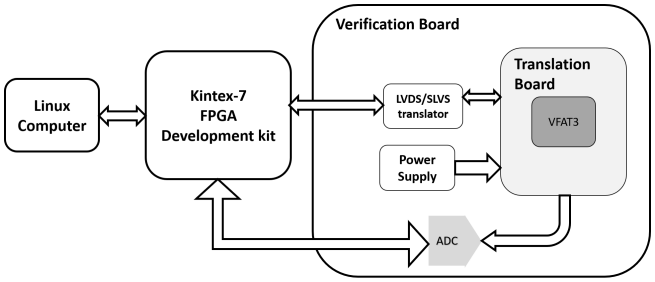
4.2 Development of VFAT3 verification platform

A VFAT3 verification platform has been designed for functional testing and detailed characterization of the internal blocks of the chip. It includes the development of necessary hardware, firmware, and software functions to perform the necessary characterization. Several high-end, small pitch printed circuit boards (PCBs) are designed and developed to mount the chip on board (CoB) directly through Aluminium wire bonding. Several interface boards are also developed to power and communicate with the ASIC in different configurations. The final

prototype version of verification platform is shown in Figure 4.1a.



(a) A functional VFAT3 verification platform



(b) Block diagram of VFAT3 verification platform.

Figure 4.1: VFAT3 verification platform

4.2.1 Hardware architecture

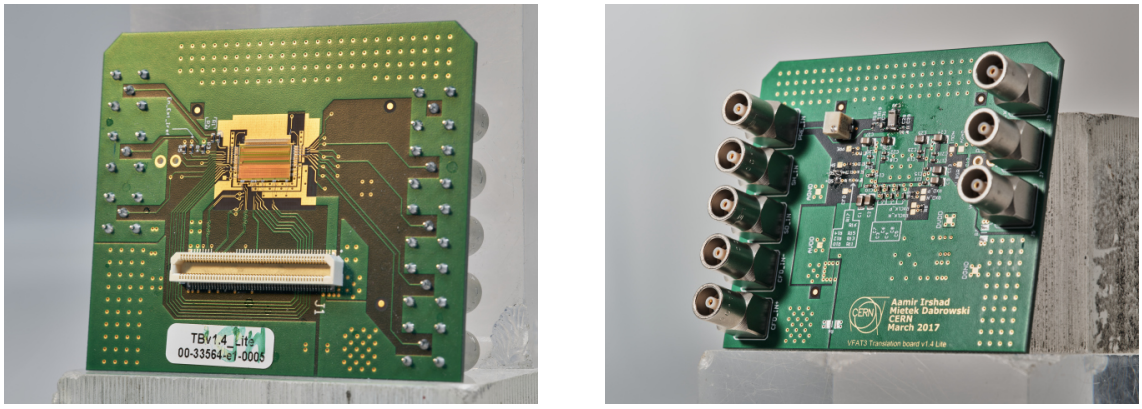
The hardware architecture consists of a translation board, a verification board, and an off-the-shelf Kintex-7 development board. The translation board was designed to host the bare VFAT3 die. The verification board provides power to the chip as well as a link to the FPGA interface. The verification board also provides three different powering options for the VFAT3, including the radiation-tolerant Feast DC-DC powering scheme [66], which is intended to power the VFAT3 during the phase-2 upgrade operation.

4.2.1.1 Translation board

A translation board was designed to host the VFAT3 die. VFAT3 is a complex mixed-signal analog & digital chip with low noise requirements, and any excessive PCB couplings and cross-talk could lead to noise increase. The front-end channels are susceptible to noise and can pick noise from nearby routed power planes. Therefore a careful routing strategy was needed to route the front-end channels, keeping away any large power strips. On the other hand, VFAT3 digital transceivers operate with the differential SLVS standard, requiring 100 Ω impedance control routing. A split planes strategy was adopted to avoid analog and digital onboard cross-talk. Both the top and bottom views of the translation board are shown in Figure 4.2

This board was designed with 4-layers stack to provide 100Ω differential impedance, required for high-speed comm-port and trigger lines routing. Small landing pads of few tens of micrometer dimensions were designed to bond the VFAT3 die pads through wire bonding. The board was designed with a fine-pitch clearance of 80 μm, and surface leveling was achieved through Electroless nickel immersion gold (ENIG) plating.

In addition to 128 analog channels, VFAT3 also provides a test channel for visualizing pulse shape and detailed characterization. The input and output of each sub-stage of the test channel are connected to VFAT3 pads. It enables the injection and monitoring of preamp, shaper, SD, and CFD signals through external equipment. The test channel was fully routed with minimal trace lengths on



(a) Translation board top view

(b) Translation board bottom view

Figure 4.2: VFAT3 translation board as a carrier PCB for wire bonded bare ASIC

the translation board to minimize external noise injection into the device. The VFAT3 Comm-port (V3CP) (explained in chapter 3 section 3.8.1) was also routed on-board to configure and characterize internal modules. The on-chip CBM module is accessible through V3CP, Imon, and Vmon pads on the chip routed to an external connector.

4.2.1.2 Verification Board

VFAT3 translation board was mounted on another large support board, named as the verification board. It provides VFAT3 power, monitoring of internal DAC, and fast e-links connectivity to the Kintex-7 FPGA. Three different power domains were generated on the verification board, namely 1.2V analog, 1.2V digital for core logic, and 2.5V digital IO power. Furthermore, three different powering schemes are also implemented on the verification board to monitor the noise effect of the power supply on the device performance. These schemes include external power supply, FEAST DC-DC modules powering, and LDO-based low noise supply schemes. A picture of the verification board is shown in Figure 4.3.

The verification board also provides impedance-controlled routing of digital signals for better noise immunity and error-free data transmission at 320 MHz clock speed.

4.2.1.3 KC705 Kintex-7 FPGA board

A Xilinx KC705 Kintex-7 evaluation board [67] was used as the main processing engine for VFAT3 test system. It consists of an XC7k325T FPGA device with plenty of logic and memory elements. VFAT3 communicates with the LVDS transceivers of the FPGA via passive level translators provided on the verification board. The FPGA on-die termination was enabled for input data lines. The development board has 1 GB DDR3 memory, which was the main working memory for the embedded MicroBlaze processor program and data during the execution. Two flash memories are also provided in the Kintex-7 board for the permanent storage of program and configuration images. The VITA 57.1 standard pinout is supported via two connectors of high pin count (HPC) and low pin count (LPC).

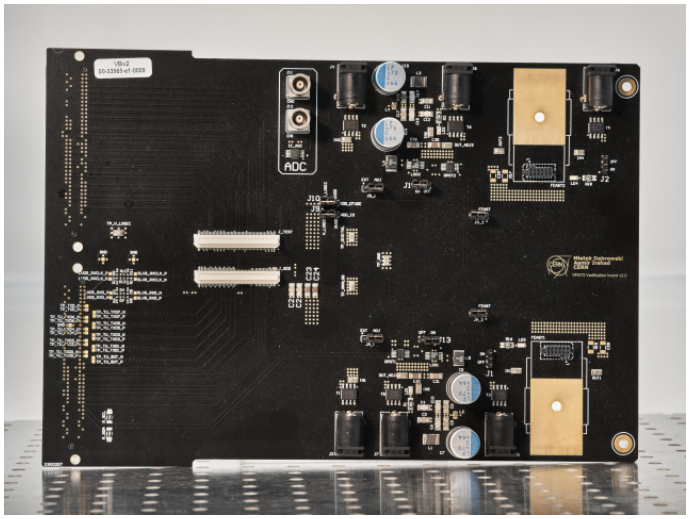


Figure 4.3: VFAT3 verification board. This board has two FMC connectors, and it can be connected to any compatible off the shelf FPGA module supporting VITA 57.1 standard

4.2.2 Firmware architecture

The block diagram of the firmware design is shown in Figure 4.4. It is based on the System on Chip (SoC) design methodology which was also successfully used by [68] for data accquisition design in the initial development stages of the GE1/1 DAQ system, before the first prototype of the OptoHybrid was designed. A 32-bit MicroBlaze processor is instantiated in the FPGA, working as the heart of the firmware blocks. MicroBlaze controls the VFAT3 and communicates to an external computer running either Matlab [69] or Python scripts through a 1 Gbps TCP/IP link. A lightweight IP stack is used on the MicroBlaze itself to establish the communication link.

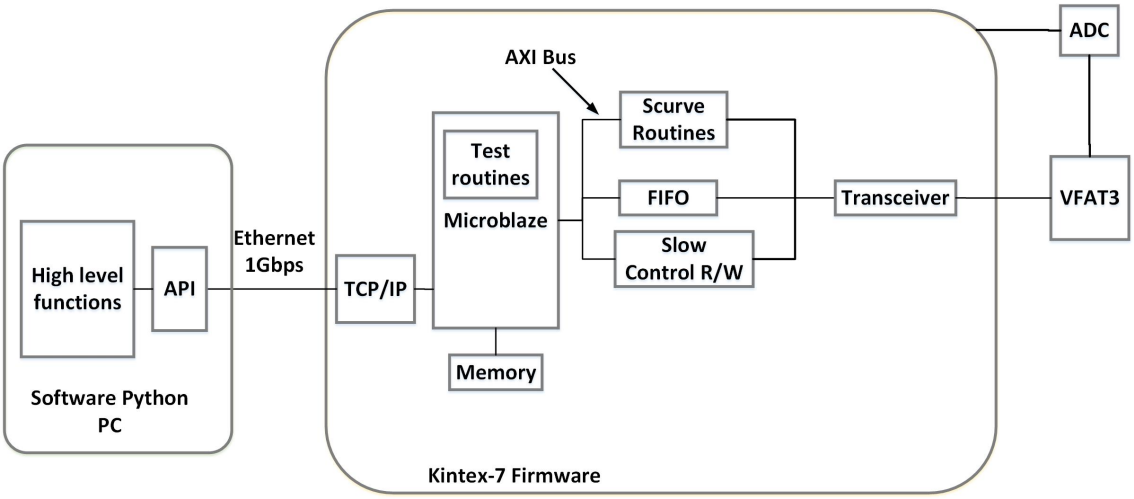


Figure 4.4: Block diagram of VFAT3 MicroBlaze based firmware

An AXI bus [70] was used for MicroBlaze and the rest of the system connectivity in the firmware design. The firmware generates two system clocks of 320 MHz and 40 MHz by using an internal PLL. The fast 320 MHz clock serves as a

master clock for the device. The VFAT3 data was de-serialized in the transceiver blocks and converted to a 40 MHz internal clock domain for post-processing. A Xilinx interconnect IP connected all the hardware IP blocks with MicroBlaze for configuration and control purposes.

4.2.2.1 AXI bus interface

Advanced eXtensible Interface (AXI) is a part of the famous ARM AMBA, a family of micro-controller buses first introduced in 1996. Xilinx has wholly adopted the AXI protocol for its Intellectual property (IP) cores beginning in 2009. The current version of AXI is AXI4, and it supports three types of interfaces. The first is the AXI4 (full) interface used for high-performance burst-supported memory-mapped data transfers. The second interface is AXI4-Lite, which is mainly used for simple, low throughput memory-mapped interfaces. In modern Xilinx-based embedded applications, IP control and configuration are done by this AXI4-Lite interface. The AXI4-Lite interface only supports the transaction of burst length 1. The data accesses only support the full width of the data bus (32/64-bits). The interface accesses are non-modifiable and non-bufferable. These restrictions make this interface extraordinarily lightweight and straightforward to use. The AXI specifications describe an interface between AXI master and slave cores that communicate with each other. The data between the cores can move in both directions simultaneously, and data transfer sizes can vary. This feature is achieved by having separate address and data buses for both read and write channels. Figure 4.5 shows how an AXI4 read transaction uses the read address and read data channels.

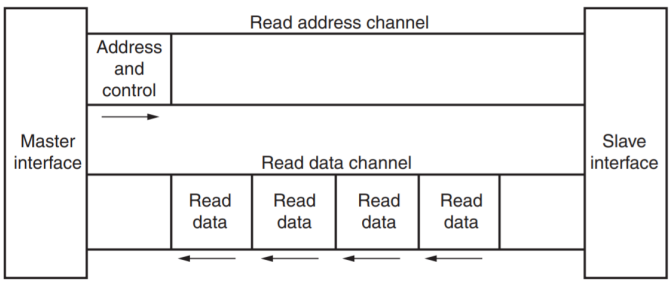


Figure 4.5: Channel architecture of reads [71]

Figure 4.6 shows how a write transaction uses the write address, write data, and write response channels.

AXI4 provides separate addresses and data lines, which allows simultaneous and bidirectional data transfer. AXI4 (full) only requires a single address and then a maximum burst of up to 256-words of data, enabling AXI4-compliant systems to achieve high throughput. The AXI4-Stream protocol defines a unidirectional channel for the transmission of data. In contrast to the first two AXI4 interfaces, the AXI4-Stream interface transmits unlimited data, a handy feature to transmit data streams in high-energy applications.

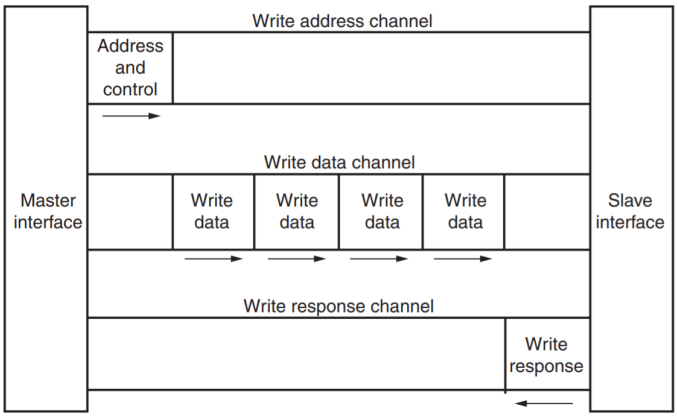


Figure 4.6: Channel architecture of write transactions [71]

4.2.2.2 MicroBlaze overview

The MicroBlaze embedded processor softcore is a reduced instruction set computer (RISC) optimized for implementation in Xilinx FPGAs [72]. A simplified block diagram of the MicroBlaze core is shown in Figure 4.7.

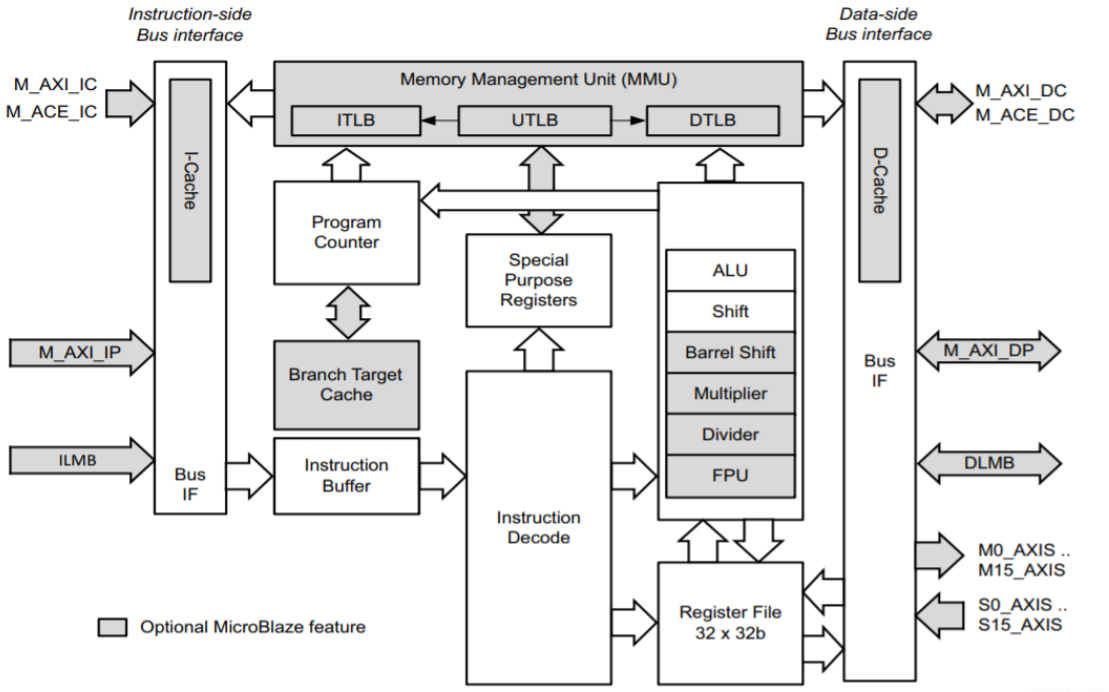


Figure 4.7: MicroBlaze core block diagram [72]

The MicroBlaze softcore processor consists of a minimal fixed feature set block and several configurable feature blocks. The minimal fixed feature set includes thirty-two 32-bit general-purpose registers, a 32-bit instruction word, and a default 32-bit address bus, extensible to 64 bits. The MicroBlaze processor is parameterized and configured to allow selective enabling of additional functionality not limited to the addition of general-purpose input-output ports (Gpio), floating-point multiplier unit, and configurable on-chip ram. The MicroBlaze AXI4 memory-mapped interfaces are only implemented as full 32-bit masters;

even 8-bit accesses are allowed. In the VFAT3 test system, all the hardware IPs were configured and controlled by the AXI4-Lite interfaces connected to MicroBlaze address and data buses through a Xilinx interconnect cross-connect switch IP.

4.2.2.3 Lightweight IP stack

A lightweight IP (lwIP) is an open-source TCP/IP networking stack provided under an open-source license. The Xilinx software environment fully supports lwIP software customized to run on MicroBlaze or PowerPC processor-based embedded systems [73].

In the VFAT3 test system, this lwIP stack is configured in echo server mode. The connected PC initiates master transactions and sends the command to slave MicroBlaze that decodes them and initiates the corresponding slave hardware functions. Upon completing the underlying task, MicroBlaze collects the data from the hardware IPs and sends back the processed packets to the computer over the TCP/IP secure link. The TCP/IP is inherently a complex stack, and MicroBlaze requires Linux or a real-time operating system (RTOS) to make it run properly. In VFAT3 test firmware, a Xilinx multi-threaded FreeRTOS is ported on MicroBlaze to run the lightweight IP stack. Its distribution is accessible under the MIT open source license. It includes a kernel and a broad set of libraries accessible through a standard "gcc" environment.

4.2.2.4 Custom AXI4-Lite IPs

Several custom-designed IPs have been integrated into the VFAT3 test system firmware. These IPs conform to the AXI4-Lite protocol. The advantage of using the AXI protocol is that MicroBlaze is connected easily with IPs for configuration purposes. Most timing-intensive functions were implemented through RTL programming blocks such as counters, multiplexers, decoders, and finite state machines (FSMs). One of the nested and time-consuming routines is the S-curve analysis (see section 4.7. An HDL implementation of data parsing block, which is an integral part of the s-curve routine, is shown in Figure 4.8. This data parsing block constitutes the innermost loop of the s-curve routine.

This IP parses incoming VFAT3 tracking data packets with a fixed latency. A total of 16 bytes contain information of 128 channels, one bit per channel. Two multiplexer stages are used to parse these bytes into single bits. Finally, these bits representing channel hits are used as enable signals for the next Hit-counter stage. If a channel got hit, then the counter is incremented. An outer software loop running on the MicroBlaze controls data flow through the AXI4-Lite interface. Finally, "hit" information is sent to the external computer for data interpretation and error function fitting algorithms.

The hardware implementation of the data parsing algorithm accelerated data acquisition rates by 25X compared to the pure software approach. The data rate at input serializers is 320 MHz, which is reduced to 40 MHz at the parser IP level. This data rate is further reduced to [40 MHz/(No.of LV1As)] per point after the parser block. For example, if we use 100 LV1A triggers per point, MicroBlaze only needs to process a 400 kHz data rate. Microblaze can easily handle such low data rates (kHz).

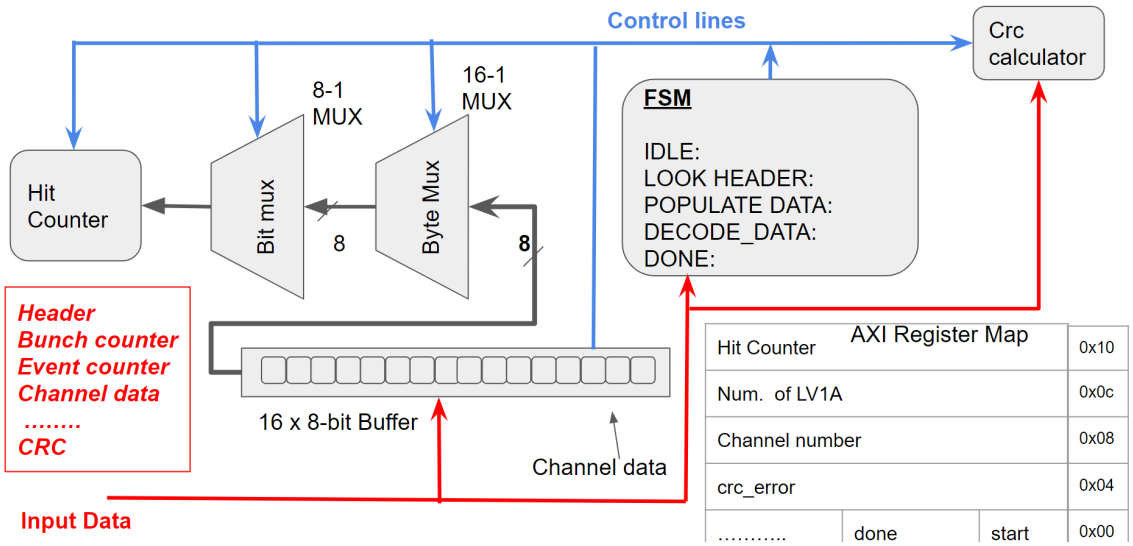


Figure 4.8: VFAT3 data parser block diagram, showing channel hit counting on real-time data stream.

4.2.3 Software design

Two different software platforms were designed to interface with VFAT3 test firmware. The first platform is intended for future VFAT3 hybrid production and is designed with Python open-source software. A graphical interface was also built using the TkInter GUI package for Python. In its first version, most of the VFAT3 basic test routines were implemented in the software only to validate the VFAT3 design functionality quickly [74]. These also included the implementation of low-level functions such as HDLC and IP-Bus-based slow control transactions. This resulted in inefficient use of available bandwidth and limited the further implementation of the complex functional testing of the device.

After major firmware upgrades, the software only sends minimal commands to initiate the corresponding hardware functions into the FPGA controlled by MicroBlaze. The processor returns the final decoded data packets, efficiently using the available bandwidth and improving the total test time.

The other test software was designed for detailed characterization with a proprietary Matlab software package. Another focus of this software was also to facilitate the debugging and validation of firmware routines. A GUI was integrated with Matlab to monitor and configure the VFAT3 register map, and characterization data was plotted to visualize device performance more intuitively. A snapshot of the Matlab GUI is shown in Figure 4.9 below.

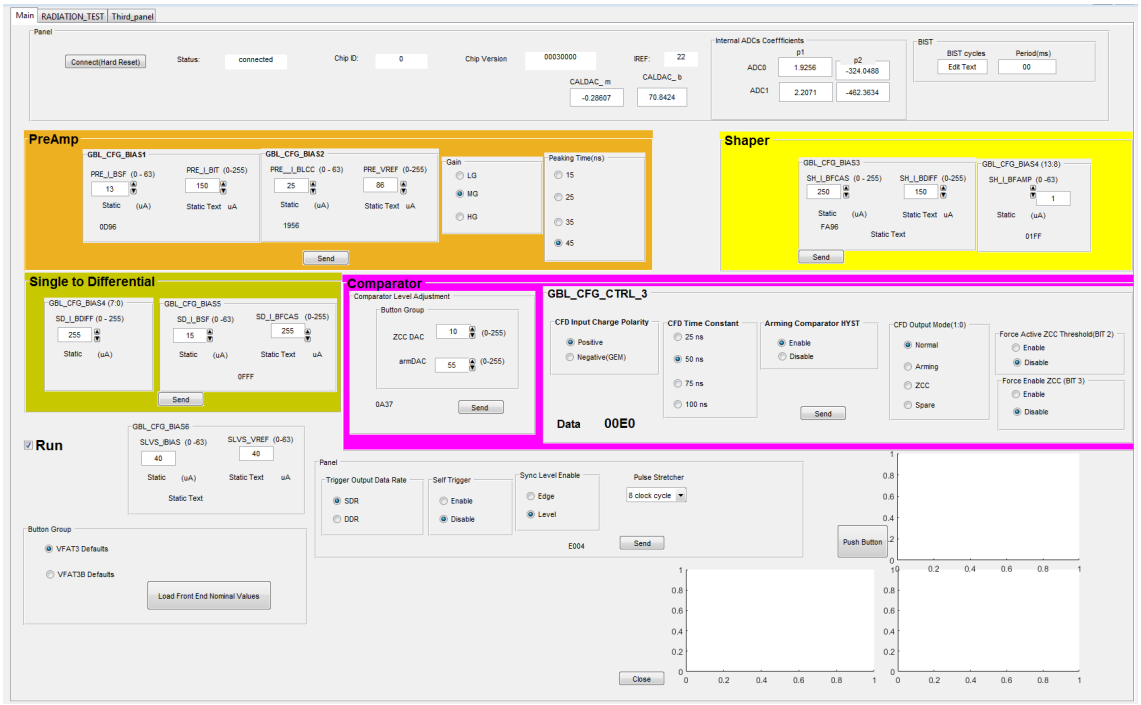


Figure 4.9: Matlab GUI VFAT3 front-end registers settings view.

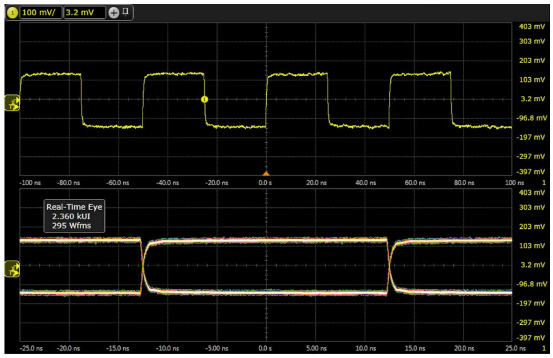
4.3 SLVS characterization

A scalable Low Voltage Signaling (SLVS) standard is adopted for the VFAT3 communication links [75]. All of the VFAT3 trigger and tracking links conform to this standard. It is a differential current-driven protocol similar to industry-standard Low Voltage Differential Signaling (LVDS). The major differences between the two standards are that SLVS has a voltage swing of 200 mV while the LVDS swing is 400 mV. Furthermore, SLVS has a common-mode voltage of 200 mV while LVDS has a common-mode voltage of 1.2 Volts. The interfacing between two standards is possible by the use of either active or passive level translators.

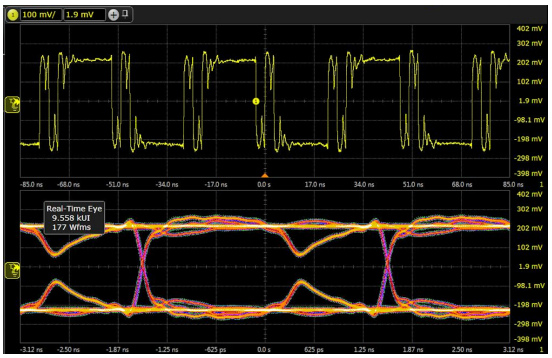
VFAT3 is designed as low power and high-speed front-end ASIC to read 128 GEM readout strips in the experiment. The VFAT3 also aims to achieve high levels of performance in terms of timing resolution and accuracy. This performance could be limited by digital noise and crosstalk within the device. The use of the SLVS standard for VFAT3 provides a low power low-voltage swing signaling, boosting signal switching capabilities without a significant increase in the resulting crosstalk in the analog blocks of the VFAT3 ASIC.

Figure 4.10 shows real time eye diagrams captures of VFAT3 RXD and TXD differential signals. The RXD plot (left) is showing idle bit patterns of 0xFF00 and TXD plot (right) is showing alternate idle bit pattern stream of of 0x7E and 0x81. These idle patterns help synchronization process on both ends of the communication channel.

In VFAT3, two reference DACs (slvs_ibias and slvs_vref) can be scanned to adjust the pk-pk amplitude of the TXD lines. The output amplitude can be adjusted by varying either of slvs_vref and slvs_ibias DACs. The SLVS output amplitude slvs_ibias dependency can be written in a linear equation, provided slvs_vref =



(a) RXD eye-pattern showing idle pattern of 0XFF00 continuously sent to VFAT3 through SLVS lines.



(b) TXD eye-pattern showing idle pattern of 0X7e and 0x81 continuously transmitted by VFAT3 through SLVS lines.

Figure 4.10: VFAT3 RXD and TXD differential signal waveforms. The upper half of each plot is showing time domain waveforms while real time eye-diagram is obtained in the lower half.

40 (default), as shown in Equation 4.1.

$$V_{out} = 8.05 * DAC_{ibias} + 104 \tag{4.1}$$

V_{out} here is the pk-pk amplitude V) with a 100 Ω termination resistor. The DAC_{ibias} word can be varied from 20 to 63 to adjust the desired output swing. It is important to note that the low values of slvs_ibias (< 20) lead to minimal pk-pk amplitude, causing communication errors and eventually losing connection with the chip. The only solution to re-establish the communication with the chip is either a hard reset or a power cycle. The default word of slvs_ibias is 40, which indicates that we have almost twenty steps on each side to adjust the output amplitude of the TXD line if required.

4.4 Front-end Transient response

VFAT3 is designed with a lot of built-in testability options. The analog front-end is a vital component of the chip, which requires a thorough characterization. In addition to 128 channels, an extra test channel with buffered outputs, directed to I/O pads of the ASIC, is provided to test and debug the channel response. The test channel with internal buffers (Fig. 4.11) is routed on "translation board" as well (Fig. 4.2).

Each substage of the test channel is routed on the translation board. Several 0Ω resistors are used on-board to connect the previous stage's output to the input of the next stage. By removing a particular 0Ω resistor, an external signal can be injected into any preamplifier, shaper, and single-to-differential stages for debugging or characterization. The analog front-end transient response is shown in Figure 4.12 at High Gain (HG) and four different peaking time settings of 15, 25, 35, and 45 ns.

The shaper and single-to-differential responses suffer from a slight undershoot due to the inter-stage AC coupling effect. The presence of this undershoot

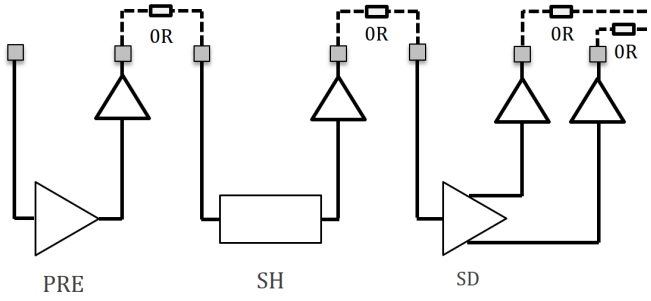


Figure 4.11: VFAT3 test channel routed on translation board [51].

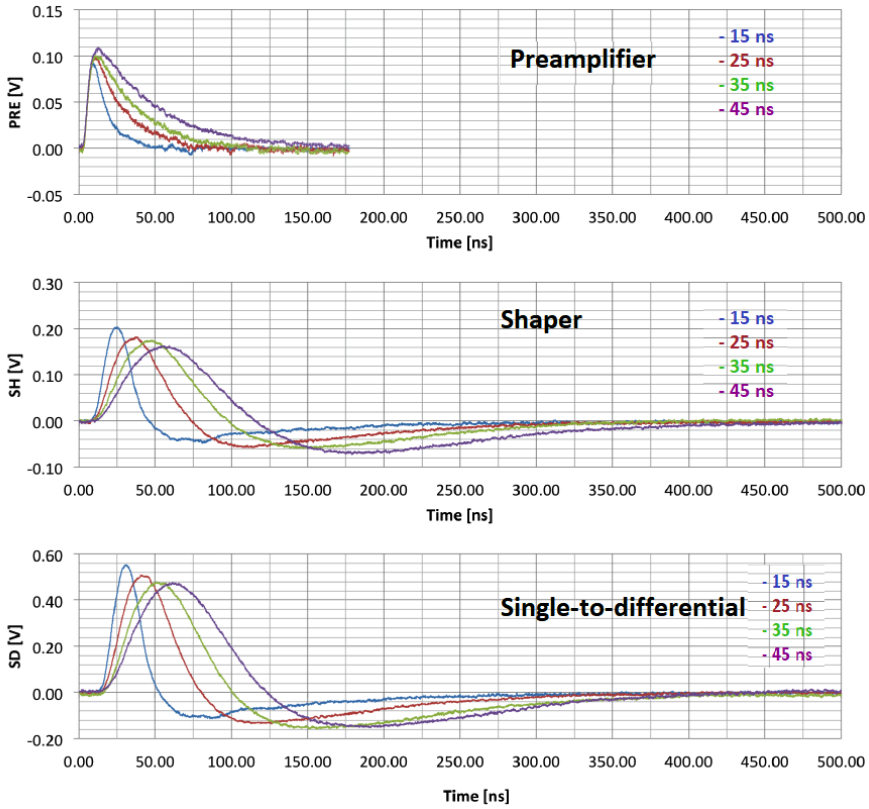


Figure 4.12: VFAT3 front-end transient response at "HG" and 15, 25, 35, 45 ns shaping time settings. The plots were obtained by using high bandwidth (12 GHz oscilloscope with TB_1.4 lite test board (translation board)) [55].

limits the maximum input particle hit rate by introducing a baseline distortion. The restoration of baseline takes 500 ns at a maximum shaping time of 45 ns. This restoration shows that the front-end can work up to a 2 MHz particle rate while CMS's maximum desired particle hit rate is 1 MHz, far less than VFAT3 supported limits.

4.5 Characterisation of CBM Module

Calibration, bias, and monitoring (CBM) modules are responsible for optimum front-end biasing and adjusting current and voltage DACs inside the chip. The

calibration of the global reference current is the first step of the CBM characterization.

4.5.1 Global Reference Current Adjustment

Iref is the reference current generated by DAC "Iref" immediately after the bandgap. This current is used as a reference current for all the other biasing DACs. In order to monitor bias currents generated in the chip, an external high precision 20 kΩ resistor (R_{ext}) is used (Figure 4.13).

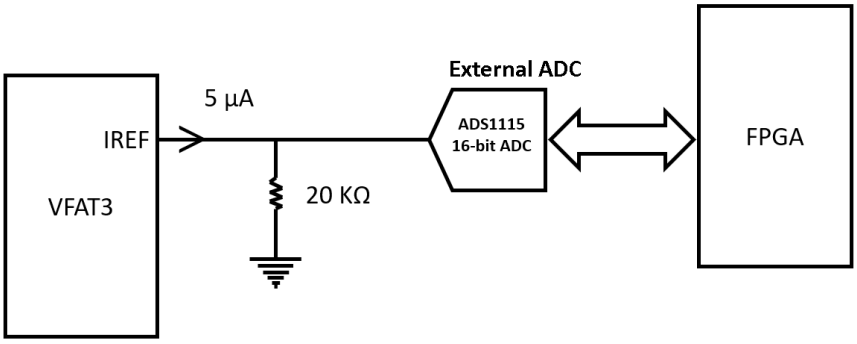


Figure 4.13: Iref adjustment through external ADC and I^2C readout routine in the FPGA

The voltage across R_{ext} is internally multiplexed. It can be read using the internal calibrated ADCs or an external ADC connected to the Imon and Vmon pins of the device. To measure and adjust the reference current, we set the Monitor_Sel bits of the GBL_CFG_CTR_4 register equal to 0. This connects the Iref DAC to the Imon monitoring pin. We then measure the voltage across the R_{ext} resistor to evaluate the current ($5\mu A \rightarrow 100$ mV across the resistor). If the measured current is different from the nominal $5\mu A$, we change the Iref bits in the GBL_CFG_CTR_5 register until the set point of 100mV is reached.

After the scanning of Iref, the value of 100mV at the Imon pin is adapted. The calibration and adjustments of all other DACs are strongly dependent on the tuned value of the Iref register(corresponds to 100 mV at Imon).

4.5.2 Calibration DAC to Charge Conversion

Each VFAT3 has 128 analog channels, and one GE1/1 GEM chamber has 24 VFAT3 ASICs mounted over the detector; thus, a total of 3072 strips need to be read out per detector. An on-chip charge injection circuit is provided in each device to test the uniformity and response of the VFAT3 analog channels. This injection circuit plays a vital role in the proper operation of GEM detectors. The principle of internal charge injection operation via a voltage step is shown in Figure 4.14.

A step is produced between two dc voltages, namely V_{high} and V_{low}. V_{low} is a constant while V_{high} is programmable via an 8-bit Calibration DAC. The step is achieved by pre-charging with one dc value and switching to the other. The polarity setting determines the precharge voltage and switching value. A 16 bit external ADC is used to read V_{high} and V_{low} voltages. Upon reception of the

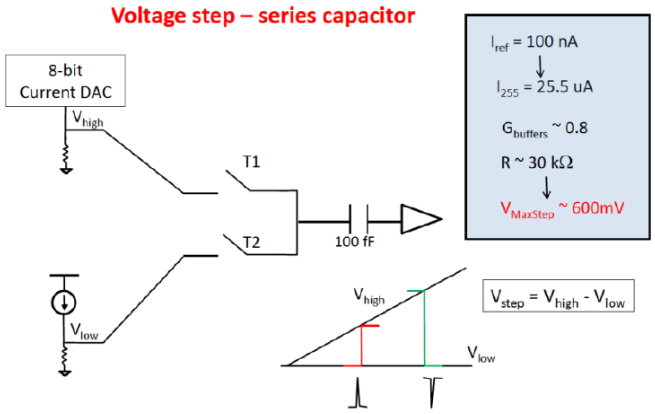


Figure 4.14: Voltage step generation - Principle of operation [51].

"Calpulse" fast command code through comm-port (V3CP), the circuit in Figure 4.14 generates a voltage pulse of V_{high} amplitude with a low latency fixed response. Using the internal monitoring system and external ADC, the Calibration DAC is scanned to measure Vhigh and Vlow. The difference between the two values multiplied by the $100fF$ injection capacitor gives the injected charge $Q = C * V_{step}$. This can then be used to generate a lookup table between the DAC word and injected charge values. Figure 4.15 plots the charge injected as a function of the Calibration DAC word for positive polarity signal pulses.

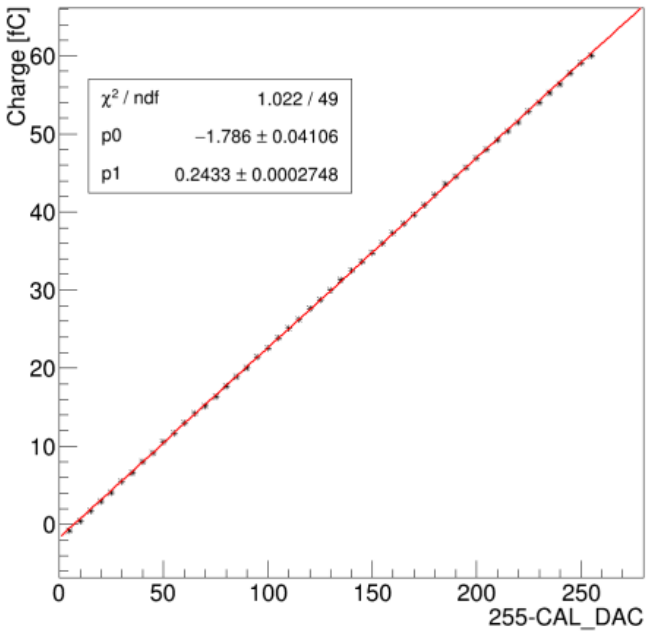


Figure 4.15: CAL DAC calibration plot

Calibration DAC scan can produce calibration pulses from $0fC$ to $60fC$ with a minimum $0.25fC$ LSB step. This is a wide range of pulse amplitudes covering the most probable GEM charge of $4fC$ and covering the amplitude range for most energetic particle strikes.

4.5.3 Internal ADC Characterization

Several currents and voltages need to be monitored for the tuning of front-end biasing circuits during device operation. Two redundant ADCs are incorporated in the VFAT3 monitoring block to achieve in-situ calibration capability. The main difference between the two ADCs is only how their reference voltage is applied. One converter (ADC0) uses an internal bandgap reference for its reference, and another converter (ADC1) uses an external reference of 1.2 Volts (AVDD) (see section 3.7.3).

The internal voltage reference circuit needs to be calibrated first before ADC0 calibration. The calibration of the internal voltage reference is made by monitoring the ADC0 reference voltage (ADC_Vref) value through the Vmon pin. A 2-bits fine adjustment (Adj) is used to tune the reference with 50 mV steps. We measure ADC_Vref for all (Adj) values (0 to 3) and choose the word to have the value closest to 1V.

After the internal voltage reference adjustment, the calibration of ADC0 is done by monitoring and scanning an internal voltage DAC (Preamp_Inp_Tran), which generates a ramp voltage with a 4mV resolution. The resulting voltages are measured both with the internal and external ADC. Finally, we use the linear fit function to obtain the gain and offset coefficients for ADC0. The gain and offset coefficients are used for the correction of measured voltages by internal ADCs. The plot for ADC0 calibration and linear fit function coefficients are shown in Figure 4.16.

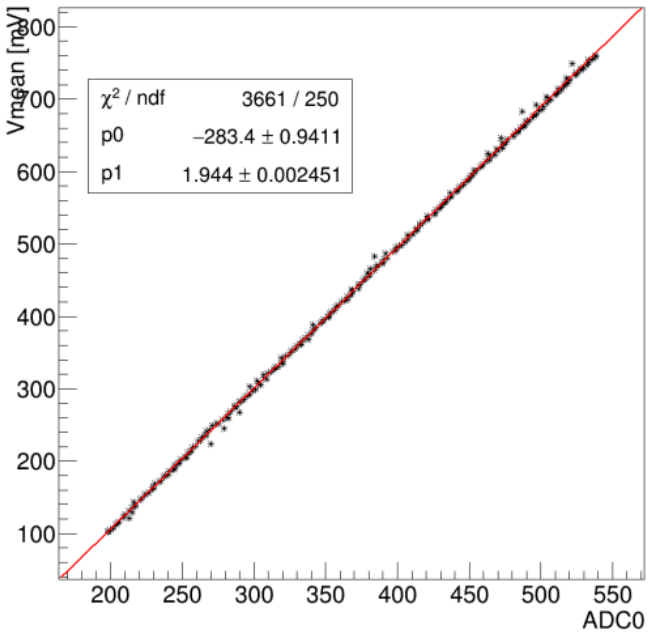


Figure 4.16: ADC0 calibration plot

The LSB of 1.94 mV is obtained from the fitting coefficients which is close to simulated LSB of 2mV. The key properties of both ADCs are tabulated in the Table 4.1.

Both converters have LSB of ∼2mV, but ADC0 showed slightly improved noise immunity and measurement accuracy compared to ADC1. This difference is the internal reference used for ADC0, which is less sensitive to supply noise.

Measured Value	ADC0 (1 V Int. reference)	ADC1 (1.2 V Ext. reference)
LSB (mean)	1.9 mV	2.2 mV
error (max)(INL)	3 mV (1.58 LSB)	3.1 mV (1.41 LSB)
error (σ)	0.9 mV (0.47 LSB)	1 mV
operational ENOB	~9	~9

Table 4.1: Key parameters coparison for both the internal ADCs,showing that ADC0 has slightly better response than ADC1

4.6 Front-end biasing: DAC Scans

VFAT3 has nine 6-bit DACs and eight 8-bit DACs to configure the front-end and communication interfaces. In addition to these global DACs, each channel has 6-bit threshold trimming and ZCC timing optimization DACs per channel (in total, 129 x 2 = 258 trimming DACs). Precise current and voltage biasing are required in the analog circuits to achieve a nominal front-end performance. All the front-end DACs need to be calibrated, scaled and converted to required current or voltage units to precisely bias the chip.

In the calibration procedure, an external ADC is used to monitor the internal DACs voltages. The procedure to calibrate all these DACs is similar and begins by switching the desired DAC to the monitoring pad connected to an external ADC. The whole DAC range 0 to 63 for 6-bit DAC and 0 to 255 for 8-bit DAC is scanned and measured by Imon/Vmon pins by external ADC.

The individual DACs were internally scaled inside the chip to generate the desired current/voltage range for proper circuit biasing. The external 16-bit ADC has an LSB of 625 μV. If the "n_{ADC}" represents measured digital word then V_{ADC} in mV can be written as

$$V_{ADC} = n_{ADC} * 0.0625 \quad (mV) \tag{4.2}$$

The DAC current without scaling correction is represented by

$$I_{raw} = (\frac{V_{ADC}}{R_{ext}} - 5) \quad (\mu A) \tag{4.3}$$

The 5μA is the global reference current, which needs to be subtracted from all other current DACs. The recommended value of R_{ext} is 20kΩ. I_{raw} further needs to be corrected by the scale factor "SF," which is applied internally to achieve the optimum range of the desired current. The desired current "I_{DAC}" can be represented as

$$I_{DAC} = \frac{I_{raw}}{SF} \quad (\mu A) \tag{4.4}$$

The required VFAT3 front-end DACs nominal currents and corresponding scale factors are shown in Table 4.2.

A combined DAC scan plot is shown in Figure 4.17, representing relative linearity and scaling differences for various VFAT3 currents and voltages. All the DACs show excellent linearity, and there are no missing codes over the entire scanning range. The DACs designing is perfectly matched with the biasing cur-

DAC	Current LSB	Full Scale	Nominal Current	Default word	Scale Factor
Preamp_BiasInputTransistor	1 μA	180 μA	150 μA	150	0.2
Preamp Bias Source follower	2 μA	126 μA	26 μA	13	0.25
Preamp_BiasLeakage	1 nA	63 nA	25 nA	25	100
Shaper_BiasInputPair	200 nA	51 μA	16 μA	80	1
Shaper_BiasFoldedCasc	200 nA	51 μA	26 μA	130	1
SD_BiasInputPair	200 nA	51 μA	28 μA	140	1
SD_BiasFoldedCasc	200 nA	51 μA	27μA	135	1
SD_BiasSource follower	500 nA	126 μA	30μA	15	0.25

Table 4.2: Front-end DACs nominal current values and scale factors.

rents and voltages such that default DAC words always correspond to the mid-point of linear ranges for GEM detector operation. This provides the maximum possible margin for parameter tuning during the experiment. It can also be seen

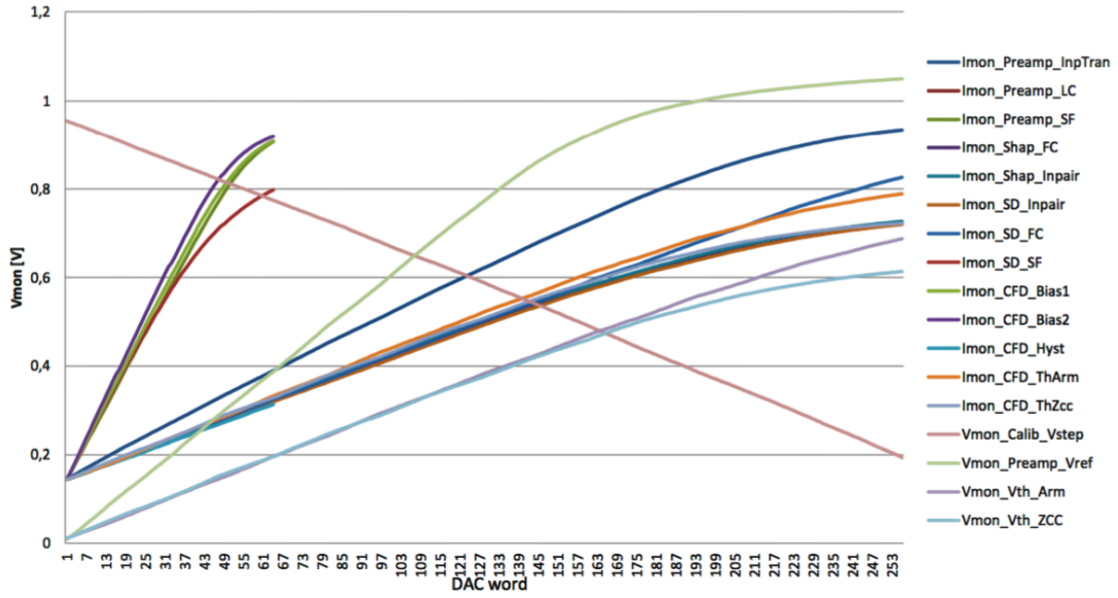


Figure 4.17: DAC scan of various VFAT3 internal currents and voltages showing different scale factors and linearities over wide useful ranges

that Calib_Vstep DAC has a negative slope and excellent linearity over the whole range, which is highly desirable for its application as a pulse generation DAC. A linear fit function is sufficient for this DAC fitting, and other DACs are calibrated through higher-order polynomials to reduce differential non-linearities. The Calib_Vstep DAC is the most frequent scanning DAC used in pulse injection circuits to calibrate the front-end channels.

4.7 S-curve analysis

The S-curve algorithm is extensively used in particle physics applications to characterize the front-end noise in readout chips. In VFAT3, known internal calibration pulses are injected into all channels one by one, and the resultant response of the channels is measured, as shown in Figure 4.18.

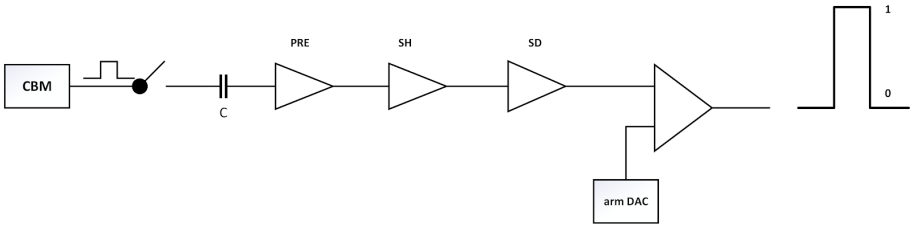


Figure 4.18: S-Curve Functional diagram

For a certain constant fraction discriminator (CFD) threshold, an s-curve is obtained by scanning calibration DAC to inject known charge pulses to input channels, and record channel hit occupancy at the CFD output. An s-curve plot is shown in Figure 4.19. Ideally, the curve should be a step function because once the pulse amplitude (V_Cal) is above the threshold, the CFD should always fire to produce a hit pulse at the output. However, the noise degrades the shape of the curve leading to an s-curve like function. The shape of the s-plot is thus directly related to the channel noise, so an error function can be fitted to compute noise and effective threshold, as shown in equation 4.5.

$$f(x) = \frac{1}{2}(1 + erf(\frac{x-\mu}{\sigma\sqrt{2}}) \tag{4.5}$$

In the equation 4.5, μ represents the mean threshold of the respected channel and σ represents the equivalent noise charge (ENC). It is defined in section 4.8 and normally represented in units of femto-Coulomb and equivalent electrons (e^-).

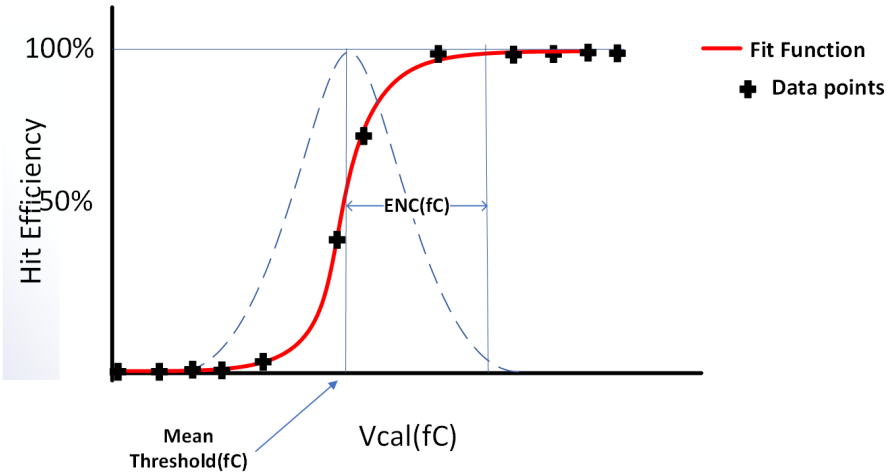
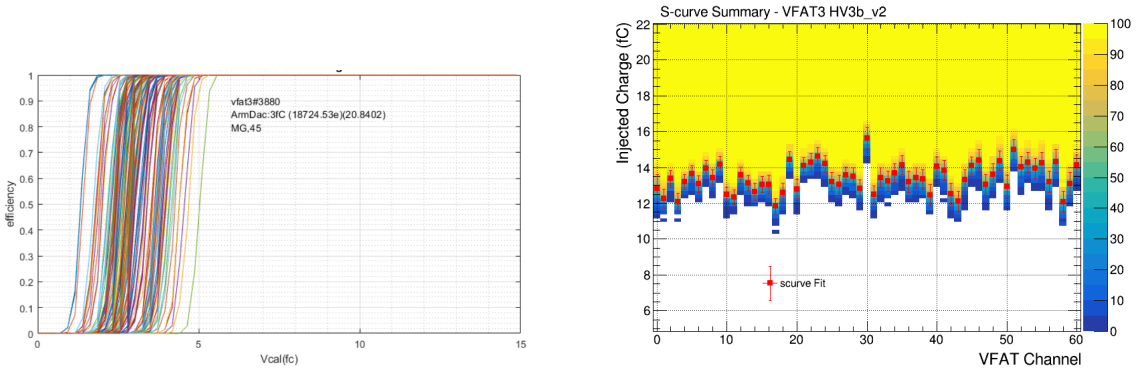


Figure 4.19: S-Curve plot formation

A 2-D representation of the s-curve plot is also adopted to visualize channel by channel thresholds and noise. Although the CFD threshold is globally applied

to all the channels, not all channels are fired at the same threshold. The possible reasons are analog transistor mismatches, and in practice, we get a distribution of channel thresholds around the setpoint threshold. S-curve from 1-VFAT3 chip are shown in Figure 4.20 with 1-D and 2-D representations.



(a) 1-D S-curve plot

(b) 2-D S-curve plot

Figure 4.20: VFAT3 S-curve plots showing channel hits

In a 1-D classic s-curve view, calibration pulse amplitude is plotted on the x-axis and hit occupancy is plotted on the vertical axis. This representation is unable to distinguish between individual channels due to overlaps of their response curves. A threshold spread and channel noise can be visually interpreted well in this representation. In the 2-D representation in Figure 4.20b, the firing of individual channels can be observed clearly, and it helps identify noisy or dead channels even with the naked eye. In the s-curve analysis, we usually use one thousand pulses per (V_cal) step to get a precise noise estimate. This makes the algorithm slow due to the processing of 1000 data packets for each input pulse amplitude. The initial implementation of the algorithm was based on the buffering of data packets and iterative data parsing to extract the channel "hit" information. The new hardware implementation of sub-modules accelerated the algorithm by unrolling iterative sub-modules and avoiding unnecessary data buffering (see section 4.2.2.4).

4.8 ENC measurement results

The amount of charge injected in the preamplifier for which $S/N = 1$ is known as equivalent noise charge (ENC). Any charge equal to or less than this value is not detectable by the channel. So this parameter defines the sensitivity of the analog channel. An accurate estimate of ENC is a critical parameter to compare the efficiency of the front-end channel response in the context of the conformity of the VFAT3 in the GEM detector system. To compute the VFAT3 channel dependence on detector capacitance, a VB_RAD board is designed having every 10^{th} channel bonded to an external LEMO connector and empty pads for capacitor insertion. An ENC measurement plot with VB_RAD measurement is shown in Figure 4.21

In the VB_RAD measurements, the front-end is configured in "High gain" and a maximum shaping time of 45 ns. The mean noise of the un-bonded channels is 600 e^- while bonded channels showed an ENC up to 900 e^-.

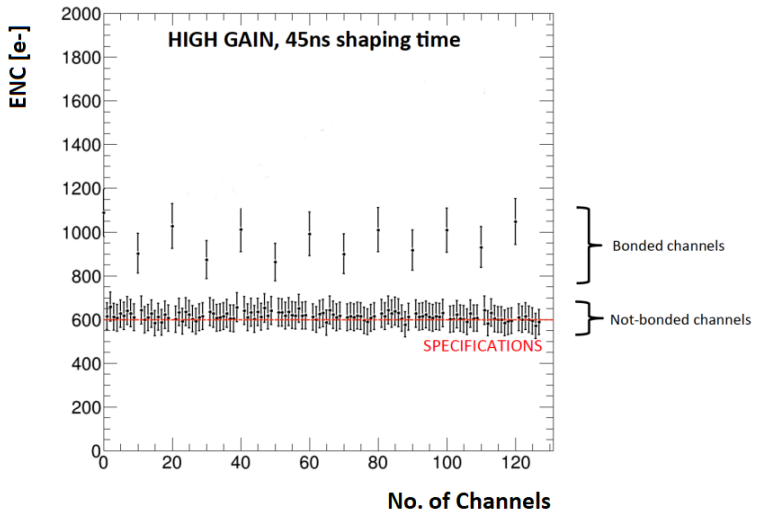


Figure 4.21: ENC measurement with Test board with every 10th channel bonded.

These measurements showed that ENC is highly sensitive to input capacitance and preamplifier gain settings. The input channel response with various detector capacitances must be computed and well understood.

Two set of measurements at high and medium gains were also performed by monitoring ENC variation versus input capacitance are shown in Figures 4.22 and 4.23.

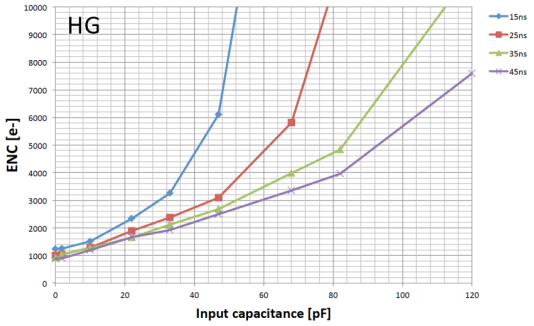


Figure 4.22: ENC measurement versus input capacitance at 4 different shaping times for High Gain (HG).

T_p[ns]	Noise Slope [e^-/pF]
15	75
25	47
35	36
45	33

Table 4.3: Noise Slope extracted from the plot @ 4 different shaping time settings

The noise slope is extracted from the plots in Figure 4.22 and tabulated in Table 4.3. The system noise increases by reducing shaping time. A minimum noise slope of 33 e^-/pF is achieved at 45 ns shaping time and "high gain" settings. On the other hand, a noise slope of 75 e^-/pF is observed at 15 ns shaping time. The exponential growth of noise slopes at all shaping times was observed, limiting the maximum allowed capacitance of 80 pF at 45 ns of shaping time. This capacitance is more than the nominal GEM readout strips capacitance of 20 pF, confirming the compatibility of VFAT3 front-end with detectors of large capacitance. At "high gain" (HG) settings, the system noise also amplifies with the signal and limits the

use of the input channels at low shaping times. The shaping times of 35 and 45 ns are the only possible choices with reasonable low noise at "HG".

The ENC variation at "medium gain" (MG) showed a mostly a linear relationship with input capacitance as shown in the Figure 4.23 and results are also tabulated in the Table 4.4.

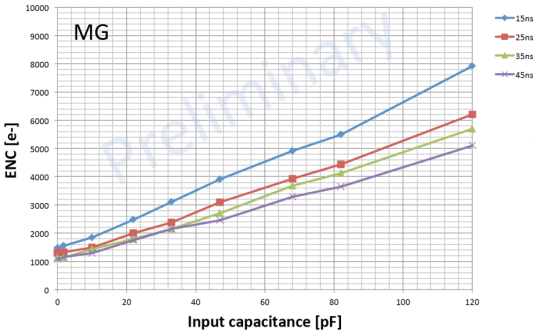


Figure 4.23: ENC measurement versus input capacitance at 4 different shaping times for Medium Gain (MG).

T_p[ns]	Noise Slope [e^-/pF]
15	57
25	40
35	31
45	28

Table 4.4: Noise Slope extracted from the left plot @ 4 different shaping time settings

A minimum noise slope of 28 e^-/pF is achieved at 45 ns shaping time and MG settings. On the other hand, a noise slope of 57 e^-/pF is observed at 15 ns shaping time. A linear response of noise slopes at all shaping times is measured, enabling the maximum allowed capacitance up to 120 pF at all shaping times. In the "medium gain" (MG) configuration, the front-end showed the lowest noise of around 1500 e^- ($C_d = 20pF$) and the maximum allowed detector capacitance of 120 pF. The MG is suitable for detectors with larger capacitance with no restriction on front-end shaping times.

4.9 Arming DAC equivalent charge conversion

An 8-bit Arming threshold DAC (armDAC) is used to set the global threshold for all input channels. The armDAC to equivalent charge conversion is computed by scanning the armDAC linear range. An s-curve is obtained for each threshold to obtain the armDAC versus extracted charge lookup table. The armDAC to fC computation also incorporates front-end gains. VFAT3 has three different gain settings and four shaping times. Hence, different armDAC calibrations are required for each of these 12 possible configurations. The armDAC plots at 45 ns shaping time and three possible gain settings LG, MG, and HG are shown in Figure 4.24.

The armDAC equivalent charge full-scale range varies inversely with the channel gain. The same armDAC word corresponds to different equivalent charge values (fC) at different gain settings. In comparison, $armDAC = 100$ corresponds to 4.75 fC at HG, 14.3 fC at MG, and 27.6 fC of equivalent charge at LG settings of the front-end channel. Around 70% of the armDAC range exhibits a linear response, which is sufficient for discriminating most of the GEM signal charges. The most probable GEM charge (MPV) is 4 fC, and the mean charge per strip for

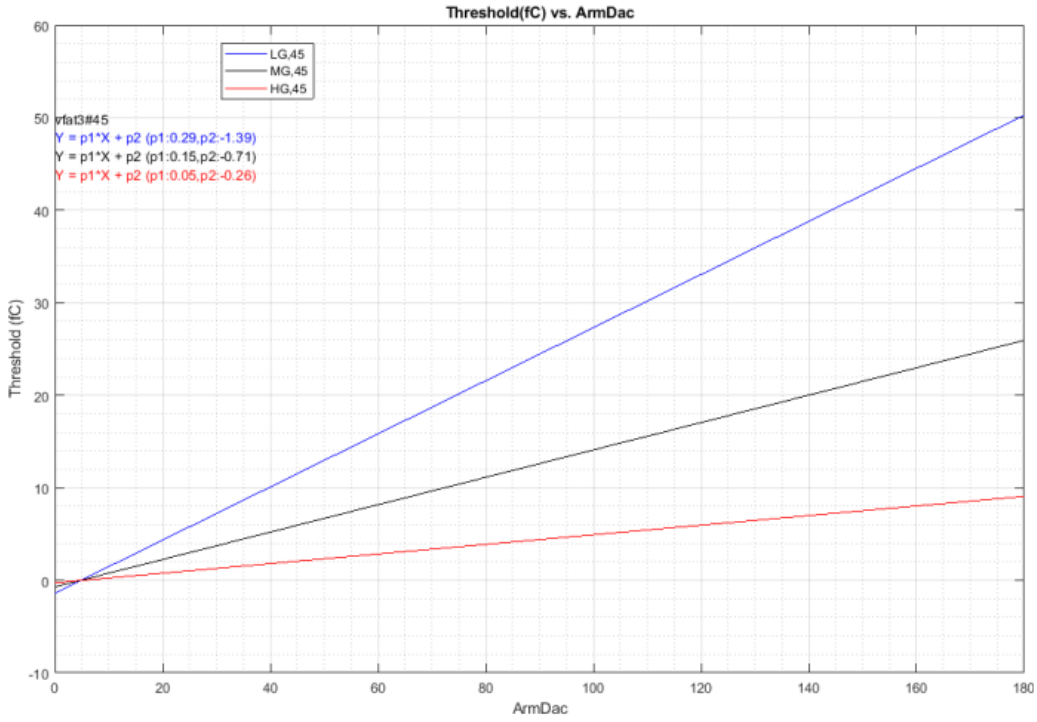


Figure 4.24: armDAC at three different gains and with 45ns shaping time. The coefficients, "p1" represent LSB in fC

GE1/1 and GE2/1 detectors is $\sim 11\ fC$ [76]. It can be seen from the plots that the front-end can discriminate a wide range of input particle energies by switching different armDAC thresholds and gain configurations. This fact made the VFAT3 a versatile front-end ASIC [55].

The global armDAC threshold can be fine-tuned locally for each channel by adjusting its 6-bit bi-directional trimming DAC. The trimming DAC plots at 45 ns shaping time and different gain settings are also plotted here in Figure 4.25.

The armDAC and trimDAC resolutions and their full-scale ranges are also tabulated in the Table 4.5 below.

Gain Settings	**armDAC range**	**armDAC LSB**	**TrimDAC Range**	**trimDAC LSB**
High Gain	**0 - 9 fC**	**0.05 fC/bit**	**±1 fC**	**0.01 fC/bit**
Medium Gain	**0 - 26 fC**	**0.15 fC/bit**	**±2 fC**	**0.04 fC/bit**
Low Gain	**0 - 50 fC**	**0.29 fC/bit**	**±5 fC**	**0.08 fC/bit**

Table 4.5: Arming DAC to Charge Equivalent Representation

In high gain, the linear armDAC range is ($0 - 9\ fC$) with an LSB of $0.05\ fC$. The trimDAC range is $\pm\ 1 fC$ with an LSB of $0.01 fC$. The maximum threshold range can be extended to $26\ fC$ and $50\ fC$ at medium and low gains, respectively.

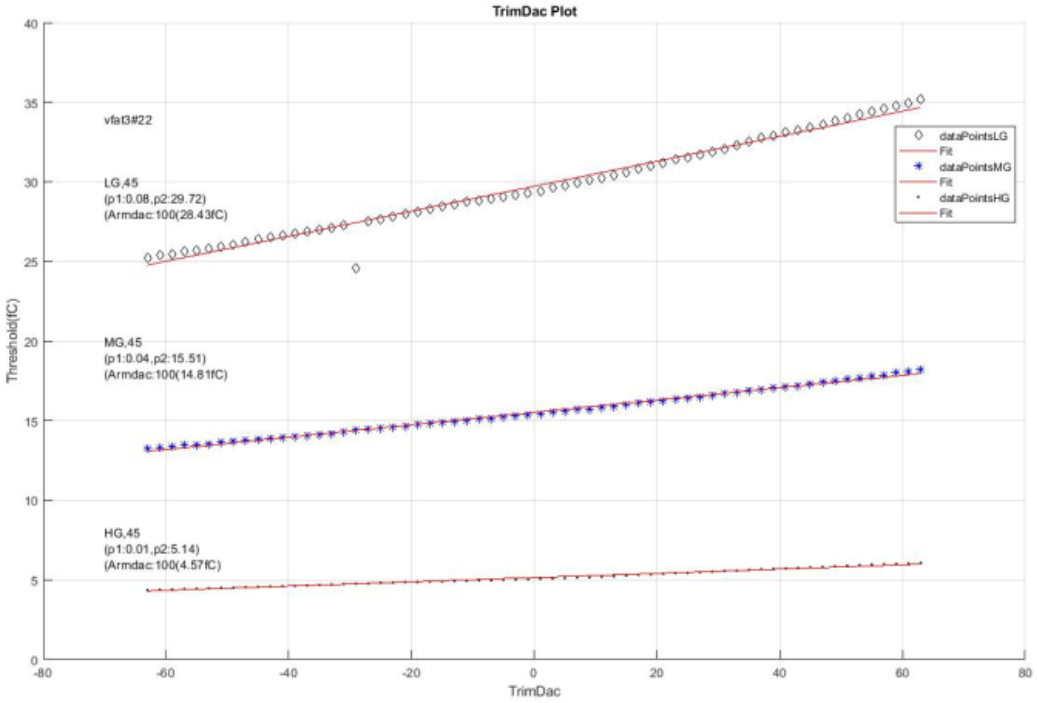


Figure 4.25: armDAC at three different gains and with 45ns shaping time. The coefficients, "p1" represent LSB in femto-coulomb

4.10 Threshold Trimming Algorithm

The s-curve plots in Figure 4.20 show a wide spread of threshold distribution for all-channels "extracted thresholds." It is necessary to narrow down the threshold spread for all the channels to detect the arrival of incoming particles correctly. In VFAT3, a global threshold (armDAC) is applied at CFD input for all analog channels. It is observed that the actual firing of individual channels is not the same for all the channels due to transistors mismatch. Each channel is designed with a 6-bit trimming DAC (trimDAC) to compensate for this mismatch. These trimDACs need to be adjusted to equalize the full chip response. We use a modified linear interpolation method using the s-curve and armDAC equivalent charge calibration coefficients to perform the threshold trimming.

The threshold trimming algorithm is based on the linear response of the trimDAC scan. The linearity of trimDAC at two different armDAC words of 50 and 100 is shown in Figure 4.26.

We start with the conversion of armDAC in femto-Coulomb (fC) units. The channel trimming needs to be done by using a nominal fixed armDAC value such as 4 fC. This value is taken as the 'set point' threshold for all the channels denoted by Th_{sp}. The s-curve for all channels is obtained at Th_{sp} with all trimDACs set to "0". The mean thresholds (fC) for all the channels are extracted by using error function fit (Eq. 4.5), named as Th_0. Ideally, these thresholds should be equal to Th_{sp}, target threshold, but in practice a wide distribution of thresholds around Th_{sp} is obtained. Next, the trimDACs of all the channels are tuned to a larger value, such as $trimDAC = +30$, s-curve for all the channels provide positive side

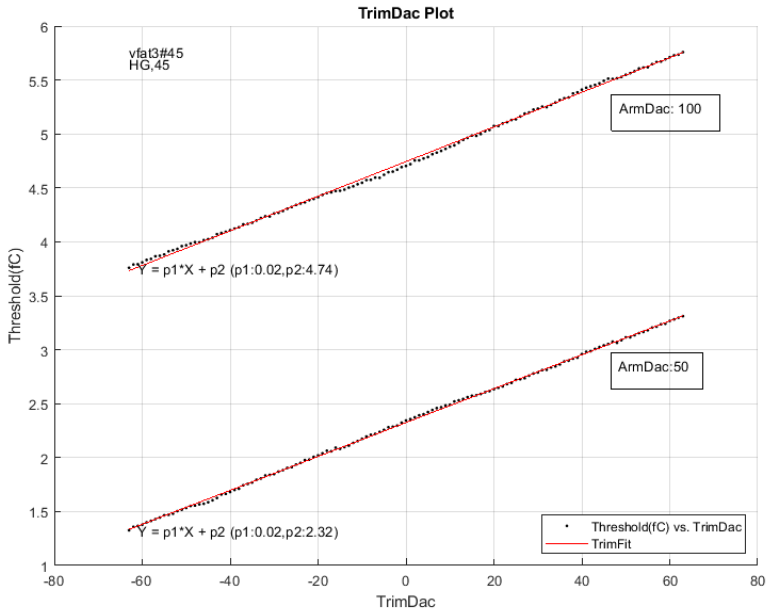


Figure 4.26: Two plots of single channel threshold (fC) vs. trimDAC at two different armDAC settings, showing linearity of trimDAC.

thresholds Th_+. Similarly, the s-curve for $trimDAC = -30$ provides Th_- for all the channels.

A plot between $trimDAC = [-30, 0, +30]$ and, $Thr_{ext}(fC) = [Th_-, Th_0, Th_+]$ for each channel is obtained. The linear fit function of data provides Gain "m" and offset "c" for each of the channel and form a linear function for evaluation of trimDAC for every channel at desired threshold of Th_{sp}.

$$TrimDAC_n = m_n * Thr_n + c_n \tag{4.6}$$

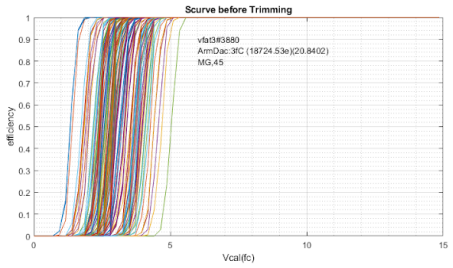
where m_n and c_n represent fit parameters obtained from linear fitting of the data for n^{th} channel and Th_n represent desired threshold for n^{th} channel. Next, we set $Thr_n = Th_{sp}$ for all channels as our set point. Finally, we compute the following equation

$$TrimDAC_n = m_n * Thr_{sp} + c_n \tag{4.7}$$

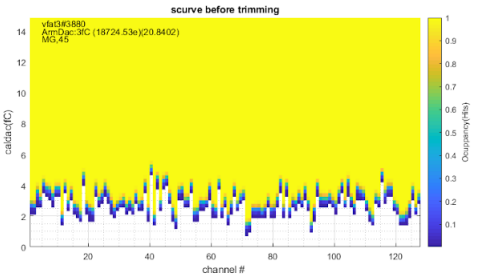
and using the equation 4.7 for all of 128 channels, we get desired trimDAC values which must be loaded in the registers to fine tune the channels.

A trimming response is shown in Figure 4.27.

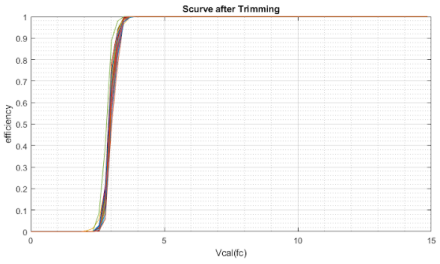
A significant level of trimming is achieved by applying this interpolation algorithm. We now define a dimensionless quantity named "trimming gain," representing a ratio between mean channel noise before trimming (σ_b) and noise after trimming (σ_a). The trimming gain of up to 29 is achieved by trimming the channels with this linear interpolation method. This method is fast, and it requires only three s-curves per channel to extract the trimDAC values. The traditional convergence-based methods suffer here due to the measurement error in successive ENC measurements. It is likely to produce less effective trimming values, which provided only a trimming gain of up to 10. This fact can also be verified by observing differential non-linearities in the trimDAC plots of Figure 4.26.



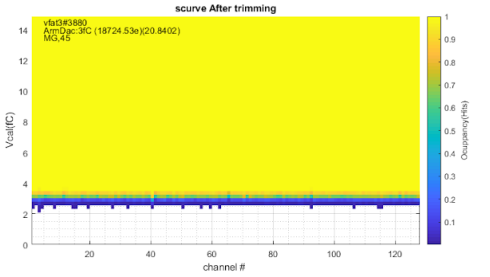
(a) 1-D s-curve before trimming



(b) 2-D s-curve before trimming



(c) 1-D s-curve after trimming



(d) 2-D s-curve after trimming

Figure 4.27: Plots showing threshold trimming results. Top two plots show s-curves before trimming and bottom 2 plots show s-curve after trimming

4.11 Internal Temperature Calibration

VFAT3 has a built-in temperature sensor, helpful in obtaining a full GEM system temperature map during CMS operation. The architecture of the VFAT3 temperature sensor is shown in Figure 4.28. It consists of two blocks: the temperature-sensitive device (sensor) and the output stage.

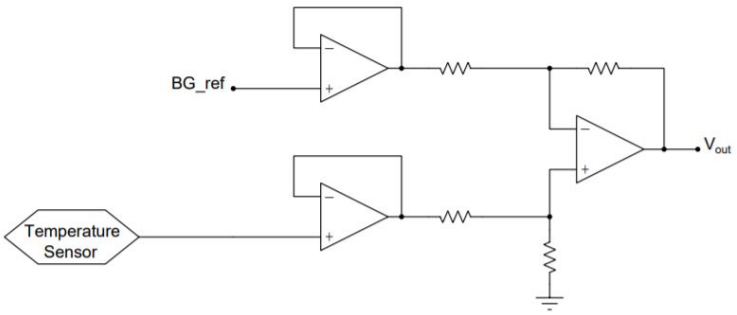


Figure 4.28: VFAT3 Internal temperature sensor block diagram.

The sensor is based on the standard PTAT architecture (Positive To Absolute Temperature). The output stage amplifies and shifts the output voltage of the PTAT stage to increase the sensitivity and keep the output swing in the power supply range. The reference voltage BG_ref used to shift the output characteristic is provided by the internal bandgap circuit (about 350 mV). The critical sensor specifications are listed in table 4.6.

Sensitivity	3.78mV/C°
Temperature Range	±100C°
Output Dynamic Range	140mV - 900mV

Table 4.6: Temperature Sensor Specifications [77].

A one-point calibration method (OPC) is implemented to compensate for the offset variation from the sensor to sensor, assuming the validity of simulated sensitivity of 3.78 mV/C° for all the sensors. We only need one temperature measurement sample to compute the offset coefficient, so the method is called a one-point correction (OPC). This method has been extensively used in infrared image processing to correct the real-time sensor offsets, assuming a unity gain for all sensor matrices.

The main benefit of this method is that there is no need to keep the VFAT3 inside a dedicated temperature chamber, and it is fast enough to be adopted for mass production at faster production rates.

This method is based on a linear extrapolation method. We use a linear relationship equation between sensor temperature and measured sensor voltage, assuming a constant sensitivity of the sensor. We computed the offset coefficient from the equation and used it in the second phase of the procedure to measure the actual temperature of the device during operation. The linear relationship can be defined as

$$V_{Tint} = m * T_{extc} + c, \tag{4.8}$$

where T_{extc} is the temperature of the chip measured by a pointed infrared gun at the time of calibration. "m" is the simulated sensitivity of the sensor ($3.78\, mV/C°$). The offset coefficient "c" can be computed as

$$c = V_{Tint} - m * T_{extc}, \tag{4.9}$$

Once offset "c" is computed, we can solve the equation 4.8 to measure the actual working temperature of the chip during experimental runs as:

$$V_{Tint} = m * T_{corr} + c, \tag{4.10}$$

$$T_{corr} = (1/m) * V_{Tint} - c/m, \tag{4.11}$$

Where T_{corr} is temperature computed by the OPC method using an offset coefficient "c" obtained during the first phase of the calibration procedure. A comparison of achieved measurement accuracy by OPC method versus standard infrared gun measurement is shown in Figure 4.29.

The operating temperature of the hybrids in CMS is around 20 °C. The internal temperature sensor has a linear response around this point, making this correction method more reliable. This fast OPC calibration achieves an accuracy of ± 2°C.

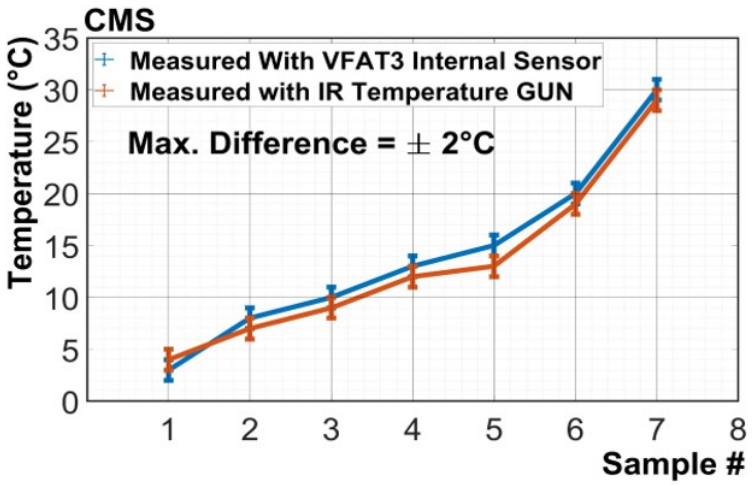


Figure 4.29: A comparison of VFAT3 temperature measured with One point method vs. Reference infrared gun.

4.12 VFAT3 CMS Phase-2 compatibility

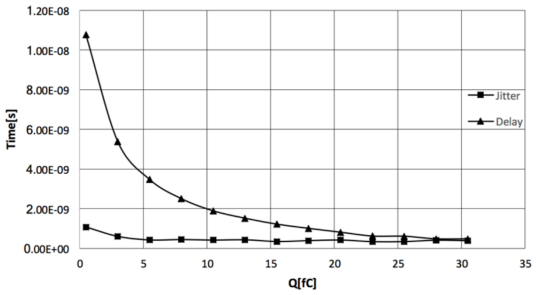
After the second long shutdown (LS2) of 2019-20, the LHC luminosity will be increased to 2-3 $\times 10^{34}$ cm^{-2}s^{-1}, exceeding the design value of 1 $\times 10^{34}$ cm^{-2}s^{-1} enabling the CMS experiment to collect approximately 100 fb^{-1} per year. A subsequent upgrade in 2022-23 will increase the luminosity up to 5 $\times 10^{34}$cm^{-2}s^{-1}. The CMS GEM system must cope with the corresponding increase in background rates and trigger requirements for this upgrade. VFAT3 is a common ASIC for three GEM stations, GE1/1, GE2/1, and ME0. More details about the last two detector stations and their design requirements are discussed in chapter 8. VFAT3 also needs to cope with this increased luminosity and its effects. The desired and achieved timing requirements, particle hit rates, trigger capability, and radiation hardness of the VFAT3 ASIC are discussed in the following sections.

4.12.1 Timing Resolution

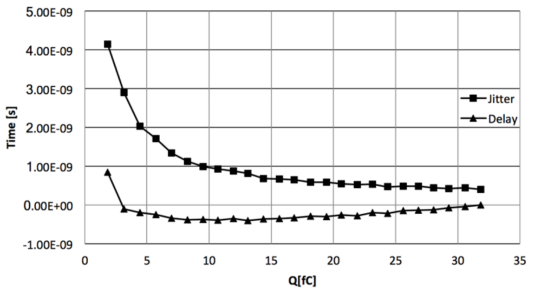
The signal from GEM detectors can have a current pulse up to 60 ns wide (see section 3.2). Time walk refers to the difference in the time delay observed at comparator output if a large and small-signal pulse is applied for the same threshold. At LHC, the proton collisions happen every 25 ns, called a bunch crossing interval. In GEMs, hits on the readout strips are detected in a series of these bunch crossing clock intervals. Therefore, VFAT3 needs precise timing so that the hits may be associated with the correct bunch crossings. This is why the time walk effect must be minimized in the VFAT3 like modern chips.

When using the CFD technique for full charge integration, the effectiveness of time walk compensation is compared to the traditional arming comparator in leading-edge detection mode.

Figure 4.30a shows the discriminator performance in Leading Edge mode and Figure 4.30b in Full Integration mode. The two plots illustrate the time walk improvement when using the CFD compared to the arming comparator. With just the arming comparator, the time walk is considerably worst ∼8.5 ns for input



(a) Discriminator performance in Leading Edge mode. The arming comparator is used with $T_p = 15ns$. Response to a current pulse of 25 ns with increasing charge.



(b) Discriminator performance in Full Charge Integration mode. The CFD comparator is used with $T_p = 45ns$. Response to a current pulse of 25 ns with increasing charge.

Figure 4.30: Time Walk comparison between arming and CFD mode comparator [51]

charge between 3 fC and 30 fC. The CFD technique reduces this to approximately 400 ps for the same input charge range, allowing optimization of the signal to noise ratio by integrating the full signal charge while maintaining optimal timing resolution.

4.12.2 High rate: Analog & Digital performance

The CMS trigger currently comprises two levels (see section 1.8) [10]. The L1 trigger consists of custom hardware processors that receive data from calorimeter and muon systems, respectively, generating a trigger signal within 3μs, with a maximum rate of 100 kHz. The entire detector is read out on receiving a Level-1 Accept (L1A) signal, and events are built. The High-Level Trigger (HLT) is implemented in software and reduces the rate to $\sim$1 kHz. This two-level strategy will not change for Phase-2, although the entire trigger and DAQ system will be replaced [78]. The GEM detector readout electronics and DAQ are required to allow a maximum L1A rate of 750 kHz and latency of 12.5 μs (or 500 LHC bunch crossings). A burst of 200 analog current pulses having 12 fC of charge @ 25 ns shaping time is injected into the VFAT3 test channel to verify VFAT3 front-end pulse processing capabilities, shown in Figure 4.31.

The preamplifier is configured to have "Medium Gain," and the comparator threshold is set to $\sim$ 8 fC. The test channel response on the oscilloscope shows that the baseline restores before 500 ns, providing a stable 2 MHz hit rate at the CFD output. This is well beyond the CMS phase-2 requirement of 750 kHz.

The VFAT3 can provide 64 trigger bits every bunch crossing single data rate (SDR) resulting from fast OR operations or 128 trigger bits double data rate (DDR), instead of 8 bits for its predecessor (VFAT2) [79]. It implies an improvement in spatial resolution of a factor of at least eight at the Level-1 trigger.

The VFAT3 tracking data packets are also highly programmable [51]. The data packets can be configured lossless or data-dependent (zero suppressed) formats to achieve high rates beyond 2MHz. Different data packets options can be seen in the Figure 4.32.

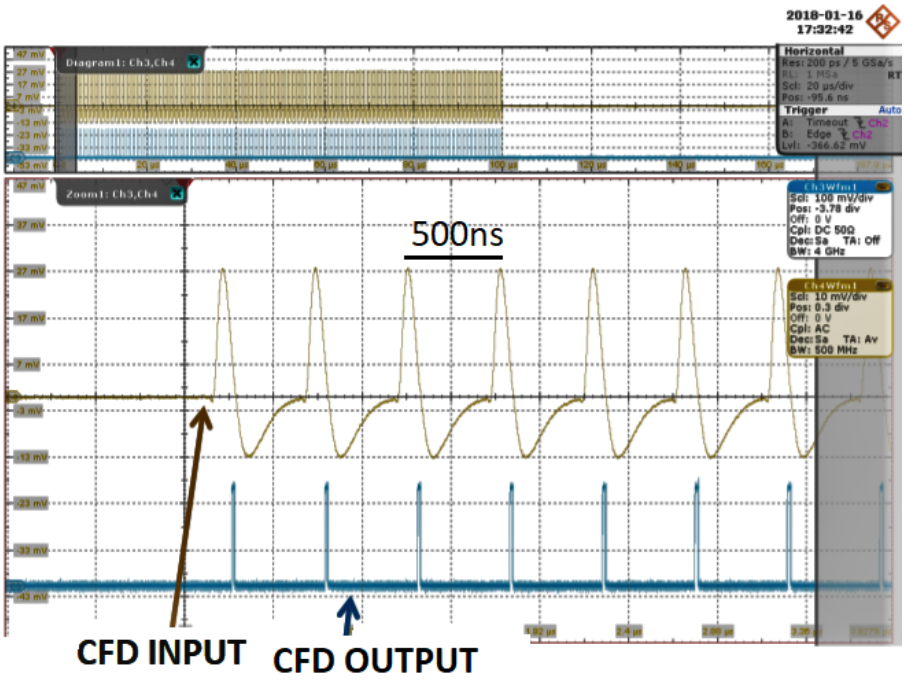


Figure 4.31: Front-end CFD firing at 2MHz showing that baseline restores up to 500ns, providing 2MHz stable pulse processing rate

Data Packet	No. Bits	Comment
Header I / Header IW	8	**Basic data packet**
EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
Data	128	
CRC	16	
Header II / Header IIW	8	**Zero Suppressed**
EC+BC / EC / BC	8 - 48	Size depends on Ecb
CRC	16	
Header II / Header IIW	8	**Zero Suppressed**

Header	8-bit representation
Header I	00011110
Header IW	01011110
Header II	00011010
Header IIW	01010110

Figure 4.32: Different lossless data packet formats can be adopted. Header is used to identify the current selected format

A variety of options can reduce the data packet size. As an example, it can be reduced to merely a header-only if no channels are hit. As a worst-case scenario, in the default "LossLess" data packet format, the packet size is 184 bits (23 bunch crossings = 575 ns). Hence, the maximum continuous Level-1 rate is 1.7 MHz without any zero suppression, beyond the CMS requirement of 750 kHz.

4.12.3 Radiation hardness requirement

All muon system detectors, including GEMs with their electronics, are presumed to last through 10 HL-LHC years (3000 fb^{-1}). As part of the muon upgrade program, the longevity of all new detectors and electronics systems must be certified for ten years of operation at the High Luminosity LHC.

The VFAT3 is a radiation-hardened design using ELT transistors, and most of its digital logic is also triplicated to mitigate total ionizing dose (TID) and single

event effects (SEE). A thorough radiation characterization is presented in Chapter 5. VFAT3 is tested up to 35 Mrad of TID in the CERN X-ray facility as acceptance criteria for HL-LHC radiation requirements. A single event effect (SEE) test was also performed at Louvain La Neuve, Belgium, verifying the configuration register radiation tolerance. CMS simulations predicted that the GEMs would receive up to 1 Mrad of total dose while VFAT3 can sustain up to 35 Mrad, which is well beyond the limits.

4.13 VFAT3 design non-conformities

Although VFAT3 is a thriving design produced in volumes, few VFAT3 functionalities did not meet design specifications. These non-conformities have no significant impact on the phase-2 performance, and thus there is no need to re-design the chip.

We discuss here briefly non-conforming parameters, beginning from the power-on-reset (POR) functionality. A POR function is implemented to reset the chip during power on its default state and initialize internal Finite state machines (FSMs). During the POR state, all the registers are reset to their default words. This circuit is not functioning as expected, and the chip needs to be reset at each power cycle externally. VFAT3 has two external pins to disable the POR functionality and others to reset the chip from some external device such as an FPGA system. So it is thus mandatory to assert the external reset signal for few cycles to reset the chip manually.

The front-end shaping times are designed to be programmable, targeting values of 25, 50, 75, and 100 ns. Measurements showed that achieved shaping times are only 15, 25, 35, and 45 ns. The impact of this non-conformity is not crucial since VFAT3 CFD can work both in edge or level mode to integrate most of the GEM signal charge at 45 ns shaping time.

A built-in self-test (BIST) testability feature is added to the chip to test the internal memory blocks. A BIST_Done signal indicates the completion of the test, and a BIST_Ok signal indicates test status. Due to a bug in the RTL code, this BIST_Ok signal cannot indicate the test result, but the BIST_Done signal indicates the end time of the test. On finding an issue, the test terminates before the nominal time of $\sim$27 ms. A solution is provided by adding a counter logic in the test bench firmware to count the time difference between BIST_start and BIST_end signal to evaluate the actual test time.

4.14 Summary

A high-performance VFAT3 functional test bench was designed comprising highly challenging hardware designs. A classical SoC-based firmware was designed in which a soft processor (MicroBlaze) was used as the main processing unit. High-speed FPGA transceiver builtin macros were instantiated to interface with the VFAT3 SLVS transceivers.

The VFAT3 functional characterization is completed successfully in conformance with the operational requirement of the CMS experiment. The measured response showed conformity with the simulated parameters up to a large extent.

The front-end noise performance was evaluated, and ENC of 650 e^- + 33e/pF was achieved, which is almost close to simulated noise of 600 e^-. It was also demonstrated that the front-end is highly sensitive to input capacitance, and both medium or high gain settings can be used for GEM charge read with 45 ns of shaping time. CFD ensures minimum time walk even at the highest possible peaking time of 45 ns. Several characterization algorithms were evaluated for arming DAC calibration, threshold trimming, and one-point correction temperature calibration. The threshold trimming allowed us to set the lowest possible thresholds at specific gain settings. The phase-2 compatibility was evaluated in detail, and it was demonstrated that VFAT3 could handle GEM charge with a longer shaping time of 45 ns and constant fraction discriminator mode. Various data packet options of the chip enable us to handle fast level-1 trigger rates up to 2 MHz.

Chapter 5

VFAT3 radiation characterization

5.1 Introduction

In CMS, the GEM detectors will be operated during more than 10 years in a radiation environment. In the CMS muon endcap the main sources of background which may affect the electronics operation are the neutrons produced within the hadronic showers and the photons produced in de-excitation of nuclei. The radiation interacts with the on-detector electronics generally in two ways. The first interactions are known as the cumulative effects, and the second is Single Event Effects (SEE). Cumulative effects are gradual anomalies developing in the electronic devices during the whole lifetime of exposure in a radiation environment. A sensitive device will exhibit failure in a radiation environment when the accumulated Total Ionizing Dose (TID) reaches its tolerance limits. On the contrary, SEE happens due to the energy deposition by a single high-energy particle to sensitive nodes in electronic devices. Therefore, these effects can happen instantaneously during device operation, and their probability is expressed as cross-sections. Characterizing the VFAT3 behavior for both effects is therefore an important step of the validation of the VFAT3 for its use with the CMS GEM detectors.

This chapter starts with a summary of the radiation environment in the CMS muon system and a reminder of the relevant radiation effects on the matter. Then the irradiation tests performed with the VFAT3 front-end hybrid are discussed. Finally, the detailed post-analysis of radiation results are discussed, mentioning the suitability of VFAT3 for the long-term operation in the CMS environment.

5.2 Background radiation in CMS muon system

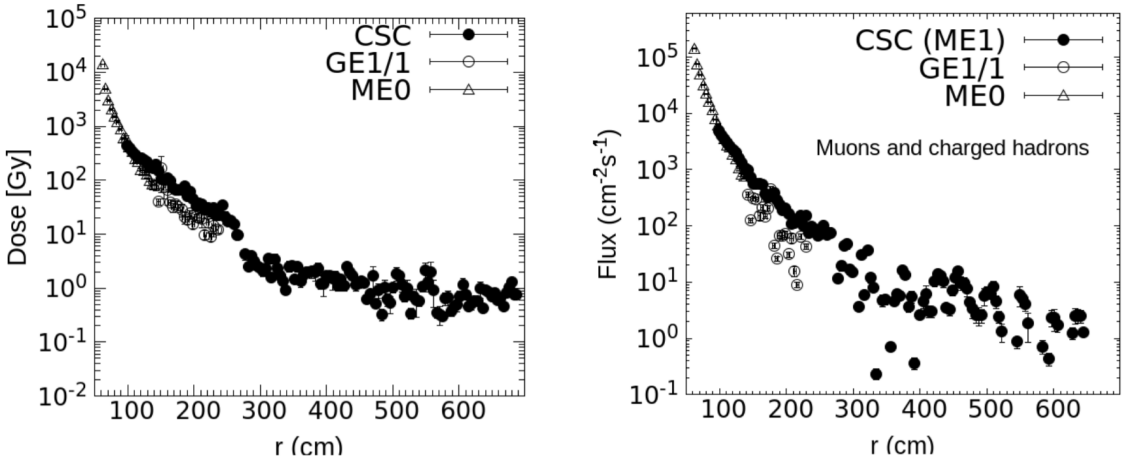
The high rates expected at the HL-LHC pose a challenge for muon detectors. Different types of detectors will receive varying particle fluxes in the CMS muon endcap. GEMs are being instrumented in the very forward region where background rates will be high. The HL-LHC background in the muon system is simulated with PYTHIA and FLUKA tools. Simulation incorporated detector materials, cavern walls modeled with an ellipsoidal shape, cavern floor, and simplified models for the electronics. The primary sources of background in the muon system are:

1. low-rate punchthrough **hadrons** from the inner region and **muons** from solenoid background, mainly a concern for segment reconstruction

2. **neutrons** from hadronic showers or the leaks in the forward shielding. These neurons primarily influence the gaseous detector longevity.

3. **photons** produced in de-excitation of nuclei through the capture of low energy neutrons. These photons are considered to be the primary source of background hits in the muon endcap region.

The simulated radiation dose levels and flux in the CMS muon endcap region for 3000 fb^{-1} are shown in Figure 5.1.



(a) Simulated total ionization dose (TID) in the muon system for 3000 fb^{-1} at HL-LHC for the endcaps.

(b) Simulated muon and charged hadrons flux in the muon system at HL-LHC for the endcaps.

Figure 5.1: Simulated total ionization dose (TID) and flux in the muon system at HL-LHC for the endcaps. [2].

The GE1/1 and GE2/1 will receive up to 10 krad (100 Gy) and ME0 will receive 1 Mrad (10 kGy) of dose in 10 HL-LHC years. The on-detector electronics need to sustain radiation for the whole HL-LHC lifetime of CMS GEM operation. The background radiation can interact with semiconductor devices and can cause temporary failures and permanent device degradation. In the section 5.3, some dominant radiation interactions with solid targets will be discussed.

5.3 Interaction of Radiation with matter

The surrounding environment strongly influences the interaction of radiation with matter. The mass, charge, and kinetic energy of particles present in the environment, play a vital role in the interaction. It also depends on the atomic number and density of the target material. Strictly discussing the CMS muon endcap region, the dominant interactions between radiation and solid targets are listed below:

1. Photons

- Photoelectric effect
- Compton scattering
- Pair production

2. Charged particles
   - Rutherford (coulombic) scattering
   - Nuclear interactions (heavy particles)
3. Neutrons
   - Nuclear interactions

The thorough details of these interactions are covered in several textbooks and other available references [80, 81]. A brief overview of underlying interactions is presented in the following sections.

5.3.1 Photon interactions

Photons interact with target atoms primarily through the photoelectric effect, Compton scattering, and pair production. In all three cases, the interaction produces energetic free electrons. Figure 5.2 shows that photon interaction is strongly dependent on the incoming photon energy and the atomic number of absorber material.

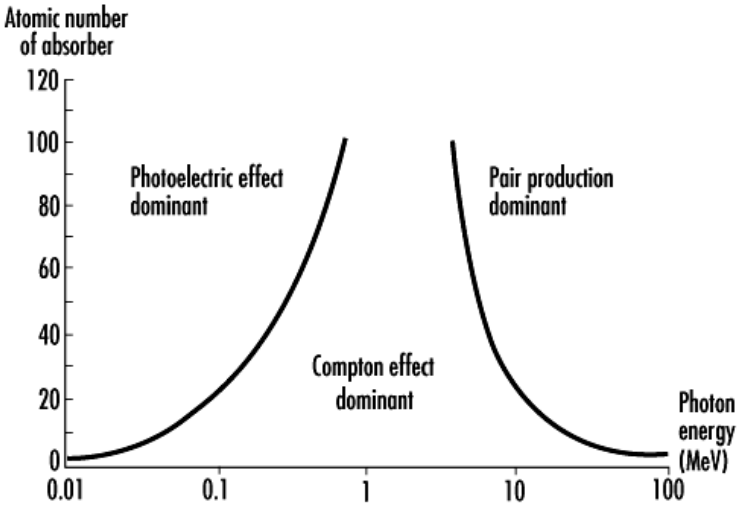


Figure 5.2: Illustration of three photon interactions as function of atomic number and photon energy

At low energies below 0.1 MeV, the photoelectric effect is dominant while Compton scattering dominates up to 10 MeV, after which pair production dominates all the interactions. The three dominant photon interactions with matter are shown in Figure 5.3. For silicon (Z = 14), the photoelectric effect dominates at energies below 50 keV, while pair production dominates for broad energy ranges up to 20 MeV photons.

In the photoelectric process, the target emitted electron entirely absorbs the incident photon energy. In Compton scattering, the incident photon with much

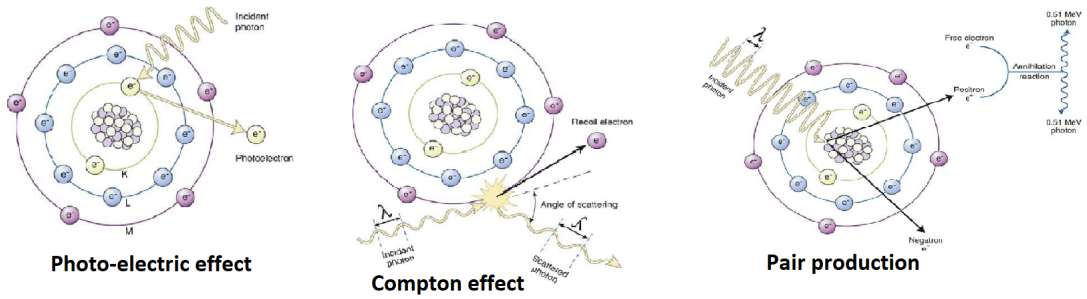


Figure 5.3: different Photon scattering interactions

higher energy gives up a fraction of its energy to the emitting electron. The scattered electron then travels in a different direction with less remaining energy. At high energies beyond 1 MeV, the pair production dominates for high-Z targets in which an incident photon is completely absorbed and releases an electron-positron pair. All discussed photon interactions ended up producing energetic secondary electrons, which then underwent subsequent charged particle Interactions. Hence, the primary energy transfer from the incident photons to the target occurs via the secondary electron interactions.

5.3.2 Charged particle interactions

The charged particle interaction with matter concerns the forces of attraction and repulsion between the charged particle and surrounding electrons and nuclei of the matter. The significant interactions involve ionization, excitation, Cerenkov and Bremsstrahlung radiation. The charged particles continuously transfer their energy to the material and slow down. We are concerned with stopping power or linear energy transfer (LET), the average energy loss by the charged particles per unit distance traveled. The primary mode of interaction is "ionization" in most cases. It occurs if the incident particle has sufficient energy to overcome the binding energy of the electron with its nucleus. The ionization creates positive and negative charges along the trajectory of the incident particle.

5.3.3 Neutron interactions

The neutrons have no charge, and their interaction with matter primarily involves a collision with the nuclei of the target atoms. The primary modes of interactions are either neutron scattering or absorption of incident neutrons. The energy of neutrons and the atomic number of the target atoms are two main factors that affect the interaction to a large extent. The neutrons are classified according to their kinetic energy. Although neutron categorization has no sharp boundaries, neutron energy plays a key role in the underlying interaction. The widely accepted neutron categories are thermal, slow, intermediate, and fast neutrons. These have typical energies of 0.025 eV, 10 eV, 100 keV, and 20 MeV respectively. Normally, neutrons are produced as fast neutrons, gradually slowed down to intermediate and slow neutrons, and ultimately absorbed by the target nucleus. Predominantly incident neutrons undergo three types of interactions, namely elastic scattering, inelastic scattering, and transmutation. In an elastic scattering of neu-

trons, the neutron recoils the target nucleus from its position and slows down. The high-energy recoiled nucleus further travels in the material and initiates ionization and excitation of its surrounding atoms. The total energy of the system remains conserved, and the recoil nucleus remains in the non-excited state. The elastic scattering occurs when the target nucleus has a low atomic number, such as hydrogen, deuterium, and paraffin.

In contrast, the recoiling nucleus absorbs some neutron energy in an inelastic scattering, which remains excited. Thus the only momentum remains conserved in this scattering, and kinetic energy is not conserved. The excited target nucleus emits gamma rays to release this energy to reach to ground state. In inelastic scattering, the incoming neutron is absorbed by the target nucleus, which later emits a slow neutron and gamma radiation. In neutron-induced nuclear transmutation reactions, the neutron is absorbed in the target material. The resulting new element is activated and emits nuclear radiation such as alpha, beta, and gamma rays. This activation poses a potential hazard for humans, particle detectors, and surrounding electronics.

5.4 Radiation effects

The interaction of radiation with matter involves several complex atomic and nuclear interactions, as briefly discussed in the preceding section 5.3. The nature of these interactions is strongly influenced by the energy, mass, and charge of incident particles. The atomic number of the target material also strongly influences the resultant mode of interaction. Concerning the effects of radiation on solid-state targets in particle physics applications, we converge to two essential consequences of these interactions: "Ionization" and "displacement damage" of the material. In the ionization process, the electron-hole pairs produced in the silicon cause the performance degradation of the underlying circuits due to transistor characteristic drift. In the displacement damage, the atoms of the target dislodge from their lattice positions. Only the most probable modes of failure in detector applications in the CMS environment are considered for this discussion. Even though a small amount of atomic displacement damage can generally occur for charged particle irradiation, the primary modes of electronic devices degradation occur due to ionization. On the contrary, for high-energy neutron irradiation, the primary modes of device degradation are associated with displacement damage, even though some ionization can occur with neutron interactions. The most common radiation-induced damages are shown in Figure 5.4.

The electronics devices operating in the CMS environment must operate for the whole HL-LHC run time of 10 years. The devices must be tested for robustness against TID radiation damage for the whole life cycle to guarantee their proper function. In practice, it is impractical to irradiate the devices for years to observe radiation impact on their operation due to the time and money involved in such rigorous testing. The standard practices are to use X-ray, heavy ions, and neutron facilities to irradiate the devices relatively quickly and then extrapolate these results for the accelerator environment. The experience of LHC phase-1 operation also demonstrated that TID testing proved to be extremely helpful in estimating the long-term damage to the silicon devices currently operating in

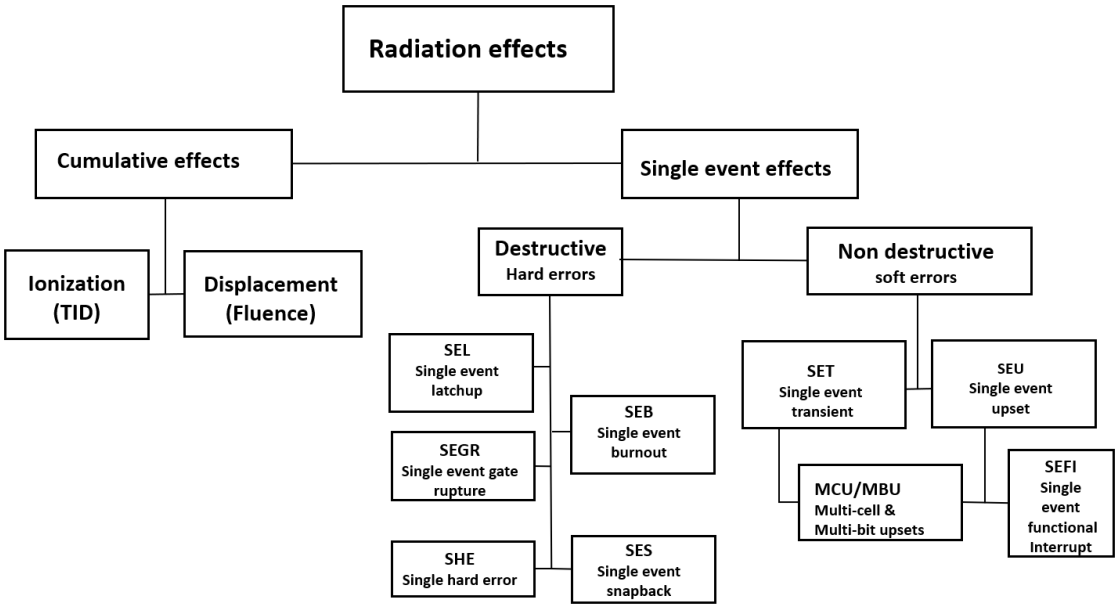


Figure 5.4: Classifcation of Radiation induced effects

LHC [82, 83]. In contrast, SEU testing proved to be helpful in the estimation of upset cross-sections by single high-energy particles in the experiment. The study of VFAT3 TID and SEE effects and implications in performing these experiments are presented in the following sections.

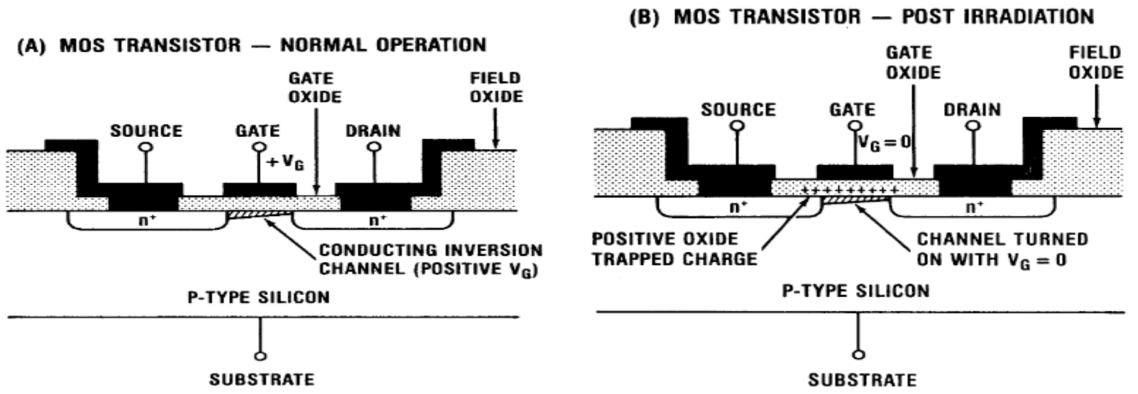
5.4.1 TID effects

During the lifetime of electronic devices operating in the radiation environment, TID is deposited in the atoms of the devices. TID is the measurement of the dose, that is, the energy, deposited in the target material by the incident radiation in the form of ionization energy [84]. In the CMS muon endcap region, ionization effects are produced mainly by the electrons, charged hadrons, gamma rays, and neutrons. A good point regarding TID effects is the gradual and predictable degradation occurring to the devices exposed for extended periods. A device sensitive to TID will fail only when the threshold TID is reached. So it is possible to precisely predict when the failure will happen for a given well-characterized component.

The basic building blocks of modern custom readout electronic integrated circuits are the Metal Oxide Semiconductor (MOS) transistors. The threshold voltage and leakage current of a MOS transistor are two intrinsic parameters affected by radiation. The threshold voltage commonly denoted by V_{gs} is defined as the minimum voltage at the gate required to turn on the device for operation. It depends on the oxide capacitance, the fixed charge due to the silicon-oxide interface, and doping concentrations. The leakage current in a MOS transistor flows between two reversed biased pn-junctions. This current also depends on the junction area and doping concentrations. Mainly, two types of effects are induced due to TID in MOS devices, named "charge buildup" and "Interface states".

5.4.1.1 Charge builup

When the electron-hole pairs produced in the material do not completely recombine in a short time, then devices suffer performance degradation. The recombination of electron-hole pair slows down if the device operates under biasing potential. The electrons leave the oxide quickly compared to holes that got trapped in defect centers in the oxide. This leads to an unnecessary positive charge trapped throughout the gate oxide (SiO_2). This effect is shown in Figure 5.5.



(a) MOS transistor normal operation before TID damage.

(b) MOS transistor with the trapped holes after TID damage.

Figure 5.5: TID effect on standard MOS transistor. The left picture shows normal operation of the MOS transistor. The right picture shows trapped charge in the positive oxide channel.

Once enough charge is trapped in the channel, it turns on even with $V_{gs} = 0$, increasing the leakage current [85].

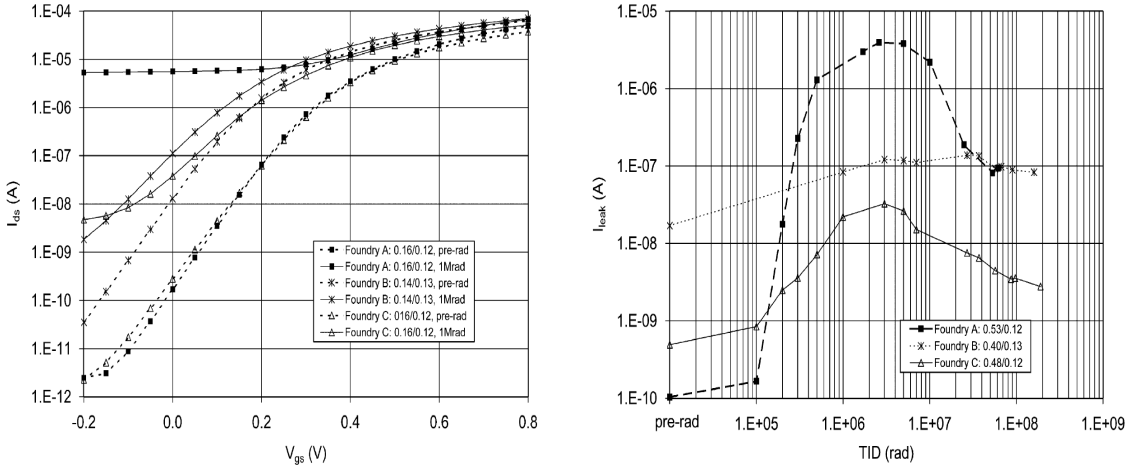
5.4.1.2 Interface states

The charge buildup also causes the creation of unnecessary conductive channels between silicon, and SiO_2 boundaries, which are known as interface states [86]. They trap channel charge leading to threshold voltage shift and also affect the carrier mobility in the channel. Holes are trapped quickly and can be recombined by annealing at higher temperatures. Increasing the temperature is an excellent method to anneal the trapped charge. Interface states instead exhibit a slow formation, and they anneal at temperatures higher than 400 $^{\circ}C$ [87].

5.4.1.3 TID implications

The hole trapping and "interface states" dynamics have a strong influence on testing methodology. The time dependence of production and recombination of holes must have a reliable damage estimate for the device in a real radiation environment. In addition, two vital aspects which may influence the TID test results are foundry-to-foundry variability and bias conditions during the tests. These are explained in [82] by F. Faccio et al. In his study, both n- and p-channel MOSFETs

manufactured in 130-nm commercial technology by three different manufacturers A, B, and C, were irradiated. The chosen core and I/O transistors were used having gate oxide thicknesses of 2.2 nm and 5.2 nm respectively. In Figure 5.6, the I_{ds} vs. V_{gs} curve of a minimum size NMOS transistor is shown before irradiation and after 1 Mrad for each foundry. The (width/length) W/L ratio is the most important parameter of the CMOS inverter affecting current flow and other parameters of CMOS transistor as well. In the plots (from Figure 5.6 to 5.8) the W/L ratio of transistors is also mentioned in the units of micrometer.



(a) I_{ds} vs V_{gs} curve in saturation of NMOS core transistor from each foundary before irradiation.

(b) Leakage current rise of a NMOS core transistor from each foundry after irradiation.

Figure 5.6: Leakage current increase with TID of a NMOS core transistor from each of three foundries [82].

TID also affected threshold voltage of transistors, as shown in Figure 5.7. A

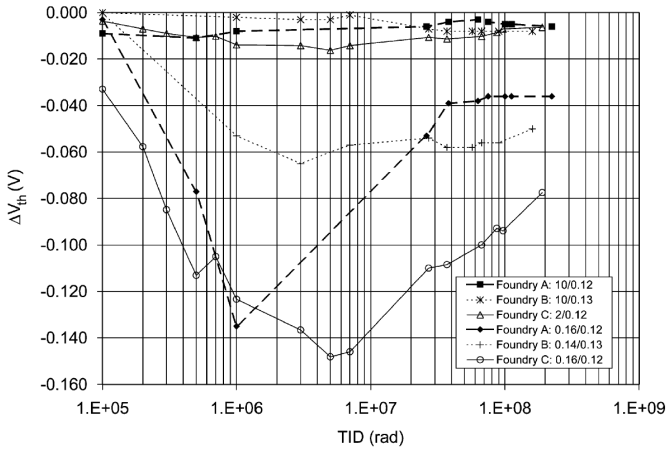


Figure 5.7: Threshold voltage shift variation with TID of both wide and narrow NMOS transistors from each foundry [82].

peak in the saturation current and threshold voltage degradation is observed between 1 and 10 Mrad. The small-size transistors showed degradation in leakage

current and threshold voltage, while large ones only showed considerable leakage current increase.

Another critical factor affecting TID results is the transistor bias conditions during the irradiation. Figure 5.8 shows threshold voltage degradation of transistors from foundry C when bias differently during irradiation.

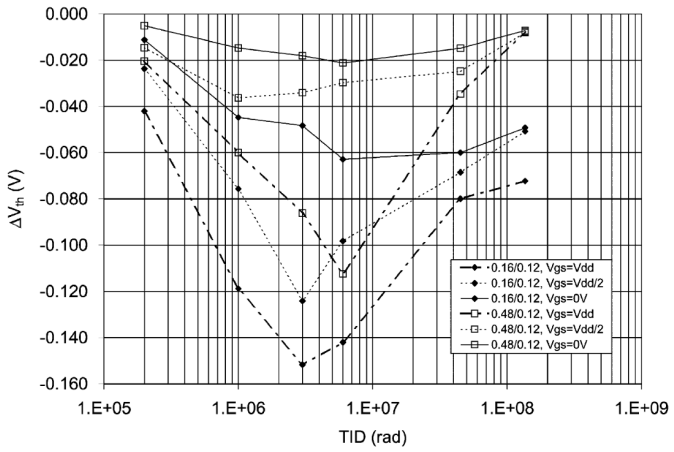


Figure 5.8: Bias impact on the threshold voltage shift of both NMOS transistors from foundry-C [82].

Due to the strong influence of foundry-to-foundry variations and bias dependence on TID results, it is recommended that the radiation tolerance of any ASIC manufactured in 130-nm technology has to be tested for every prototyping and engineering run.

5.4.2 Single Event Effects

In addition to gradual, cumulative effects, Single Event Effects (SEE) are also radiation damages that cause sudden interruption to the device operation or sometimes permanent damage to the devices in the worst scenarios. SEE happens when energy deposition by a single incoming particle is sufficient to change the radiation-sensitive node voltage levels in the underlying circuit. These effects can happen at any moment, and their probability is represented in terms of the cross-section. A device sensitive to SEE can exhibit failure at any moment since its operation in a radiation environment. The typical modes of failure include device memory and configuration corruption due to bit flips. A sensitive node in a memory cell struck by a high-energy particle is shown in Figure 5.9.

In MOS circuits, reverse-biased nodes are usually the most sensitive part of the devices. A typical sequence of single event upset in such a MOS transistor is shown in Figure 5.10. A long track of electron-hole pairs is formed with a sub-micron radius when an energetic particle passes through a sensitive region (Fig. 5.10 a). Due to reverse biasing, near the depletion region, the carriers are promptly collected in that region, and a fast current transient is produced at the node Fig. (5.10 b). The electrons with much higher mobility move faster, and a potential distortion creates a funnel in the substrate [88]. This funnel enhances the charge collection drastically and completes the collection in nanoseconds, depending on the doping concentration of the substrate. In Figure 5.10 c, the

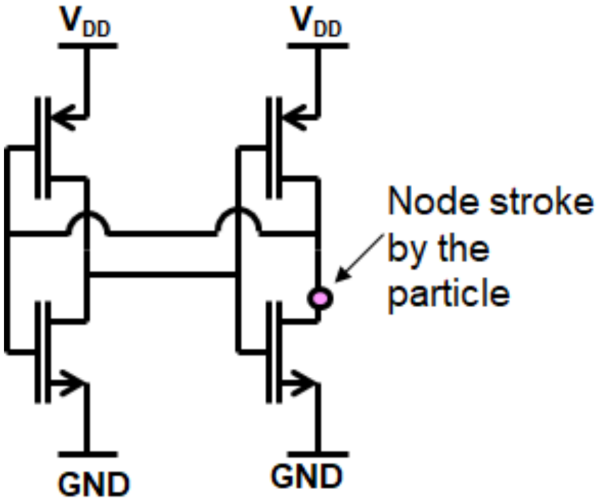


Figure 5.9: High energy particle struck a sensitive node changing voltage level at the output.

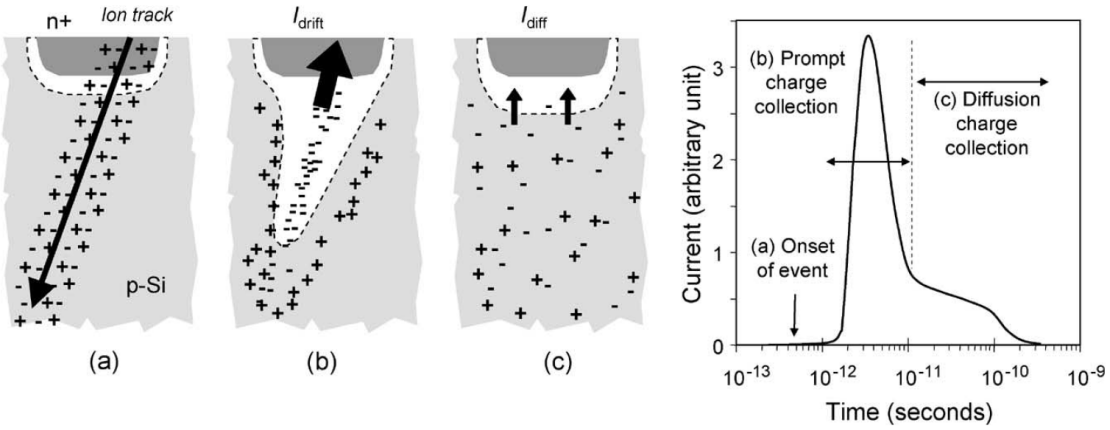


Figure 5.10: Charge generation and collection phases in reverse-biased MOS transistor. A sharp current pulse is generated with a relatively long tail region [89].

relatively slow diffusion starts to dominate, and a further charge is collected as electrons continue to be absorbed in the depletion region. It takes hundreds of nanoseconds to completely diffuse or recombine the excess charges in the substrate region. The right plot of Figure 5.10 explains all three phases of a typical charge generation in a reversed-biased MOS transistor. In general, the closer the funnel creation happens to the depletion region, the larger the produced charge, and more damage will be done and vice versa. Other factors also influence the SEU effect in actual circuits, such as the proximity of the sensitive nodes to other nodes. Closer the nodes, larger will be the charge sharing among them, and unwanted parasitic transistors will be created between junctions, influencing the transients produced in the circuit.

A simplified classification of different kinds of SEEs is also shown in Figure 5.4. The SEE is classified into two broad categories, hard errors and soft errors. The hard errors cause permanent damage to the microelectronic devices, and thus devices stop working. Single event latchup (SEL) is the most commonly

occurring hard error condition in the devices. An unwanted creation of a low-impedance path between the transistor power rails leads to a short circuit in the device, thus destroying the circuit. Single event gate rupture (SEGR) causes damaging the gate oxide and the formation of the oxide conducting path. An increase in gate leakage current follows, and degradation of the device or permanent malfunction occurs [90].

In contrast, single event soft errors are non-destructive and can be corrected by reloading the configuration or by making a hard-reset of the device. Nevertheless, soft errors become more critical due to their impact on device operation. It is necessary to measure the device cross-section for the SEEs to find the threshold energy beyond which the device is sensitive to energetic particles. The soft errors are generally of two kinds: Single event transients (SET) and Single Event Upsets (SEU) [91]. SET effects are difficult to probe in complex ASICs, and in most cases, these effects do not disturb the device operations. The SET effect is the production of combinational glitches in the digital circuit, disturbing device operation. If these glitches latched up in the device registers, we call them SEUs. In most cases, SEU may lead to malfunctioning of the device or unexpected device operation. In general, SEU cross-sections of the devices are measured by heavy-ions or protons beam irradiation in a vacuum environment in dedicated accelerator facilities.

5.5 VFAT3 irradiation campaign

VFAT3 is designed to operate in a harsh CMS radiation environment for at least ten years. The radiation characterization of the VFAT3 is necessary to ensure the reliable operation of the device for HL-LHC GEM operations. The device should sustain both the cumulative and single event effects during this life cycle. An extensive irradiation campaign was launched to evaluate the radiation hardness of the device. First, the device was irradiated with an X-ray beam to explore the TID response. An SEU test of the device is also done with multiple heavy-ion beams to find the event cross-section and ensure its safe operation.

5.6 VFAT3 TID Test

In CMS GEM detectors, the maximum background particle rate is 378 kHz cm^{-2} (see Figure 5.32b). Over the HL-LHC 10-years of operation, the GEMs will only receive a maximum of 1 Mrad dose at the innermost position (see Figure 2.7 in [92]). It was decided to test the performance of VFAT3 up to extended ranges to find its radiation tolerance limits. Two different TID irradiation were performed. The first test was conducted to evaluate the radiation effect on all internal modules of the device. The second test was conducted to investigate further some communication issues encountered during the first test. Dose rates of 1.84 and 5.5 Mrad/hr were used for the first and second tests. VAFT3 TID testing is performed with an X-ray facility at CERN, named ObeliX [93], as shown in Figure 5.11.

The ObeliX irradiation system consists of a Seifert RP149 X-ray machine, a base plate to mount device under test (DUT), a cooling system, and a humidity

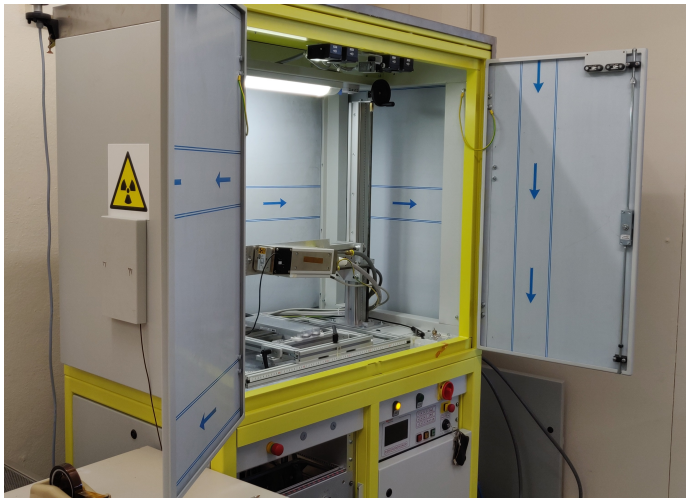


Figure 5.11: The ObeliX X-ray facility at CERN [93]

control system with a compressed air network. The thermal plate can be set to temperatures ranging from -50 to 200 °C to facilitate a wide range of irradiation configurations. The tube and thermal plate both are manually adjustable to align the DUT properly. The X-ray tube shown in Figure 5.12 provides a peak of 10 keV X-ray beam of radiation. A 150 µm Aluminium filter is also added in front of the Beryllium window to ensure a uniform dose rate of up to 9 Mrad/hr (SiO_2 equivalent for semiconductor chips).

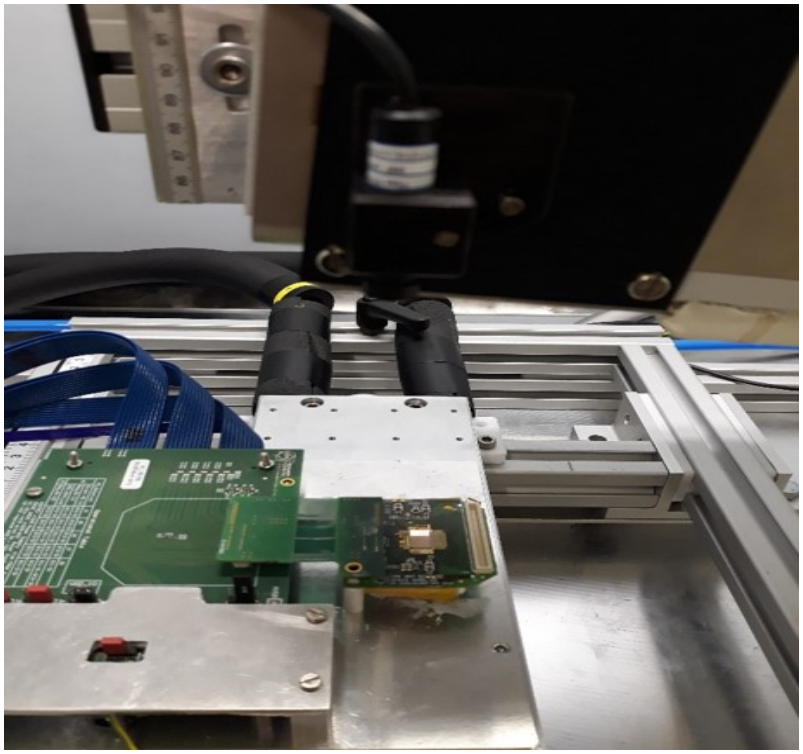


Figure 5.12: VFAT3 hybrid is mounted on a base plate during irradiation

The machine is calibrated with a PIN diode, with a sensitive depth of 25 µm. The tube can be operated up to a maximum tube voltage of 50 kV and a 60 mA current. A laser pointer is provided to align the DUT with the X-ray beam center.

Two samples of VFAT3 hybrids with wire-bonded VFAT3 were irradiated in the facility. The VFAT3 front-end noise, calibration circuit performance, and communication links were observed during the irradiation and compared with the pre-rad reference data. A custom radiation test bench, shown in Figure 5.13, has been designed to configure and monitor the chip during X-ray irradiation. A combination of two 90 cm long FMC cables connects the VFAT3 interface board to the external FPGA module. The cables are routed through narrow feedthrough, to communicate with the DUT safely. A Kintex-7 FPGA is used running 320 MHz clock to interface with VFAT3 SLVS lines. The tap delay in the Kintex-7 serializer provides a resolution of 78 ps to align the phase with the VFAT3. A PC running the Matlab script is used to capture live data during radiation.

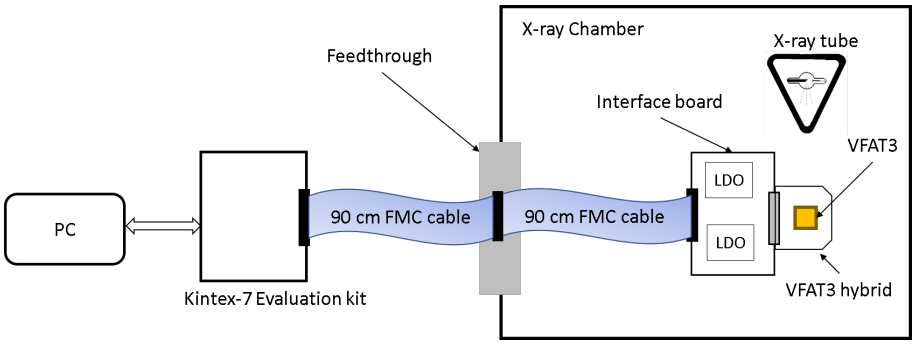
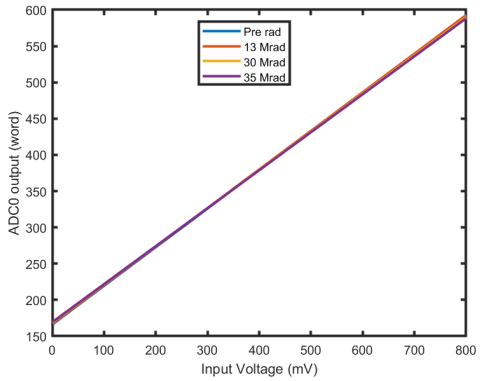


Figure 5.13: A simplified VFAT3 radiation test system block diagram.

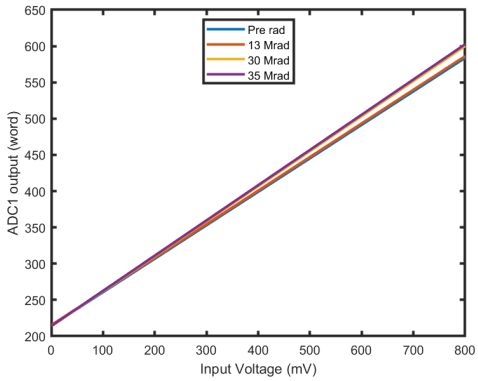
5.6.1 TID effect on internal ADCs

Both the internal ADCs were evaluated for performance deterioration due to TID effects. The linearity of the ADCs was monitored after each dose run. The linearity was evaluated before the radiation as a reference to monitor any integrated dose effect. The Figures 5.14a and 5.14b show the linearity plots of ADC0 and ADC1 respectively, before and after the irradiation. All the four checkpoint plots starting from pre-rad data, 13, 30, and 35 Mrad plots are superimposed on each other to show the variation in the linearity of the ADCs.

ADC1 has an LSB of 2.13 mV before irradiation, which decreased to 2.05 mV after TID of 35 Mrad. The offset coefficient increased from a pre-rad value of -459 to -440 for a maximum TID of 35 Mrad. This variation represents a 3.8% decrease and a 4.1% increase in the LSB and offset coefficients respectively. Similarly, ADC0 has an LSB of 1.88 mV before irradiation, which increased to 1.91 mV after a TID of 35 Mrad. The offset coefficient also decreased from a pre-rad value of -312 to -323 for a maximum TID of 35 Mrad. These variations represent only a 1.2% increase and a 2.8% decrease in the LSB and the offset coefficients, respectively, over the entire TID up to 35 Mrad. These deviations translated to a maximum of 1.3% error in the voltage measurement over the entire input voltage range of 1.0 Volt. Considering the maximum TID of 1 Mrad for GEMs, we can conclude that this variation would not be influential during the whole life cycle of GEMs.



(a) TID effect on ADC0 showing almost similar response curves, least affected by radiation.



(b) TID effect on ADC1 showing a slight response variation with increasing radiation dose

Figure 5.14: TID plots for ADC0 and ADC1 showing response variation after increasing doses

5.6.2 Front-end biasing TID effects

The VFAT3 front-end biasing DACs are part of the CBM module discussed in section 3.7 and 4.6. VFAT3 has nine 6-bit DACs and eight 8-bit DACs to configure the front-end and communication interfaces. The effects of TID on the front-end biasing have been monitored by looking at output current stability as a function of the DAC input word. All the front-end biasing DACs showed good stability and linearity during the TID test. The linear fit analysis of two of the front-end DACs is discussed in detail. The first is the preamplifier InputTrans DAC which has a current LSB of 0.7 μA with an offset coefficient of 4.3 μA during pre-radiation measurements. After a maximum dose of 35 Mrad, the current LSB decreased to 0.68 μA with the dc offset of 4.12 μA. This change translates to a 2.6 % decrease in the current LSB and a 4.4 % decrease in the offset coefficient.

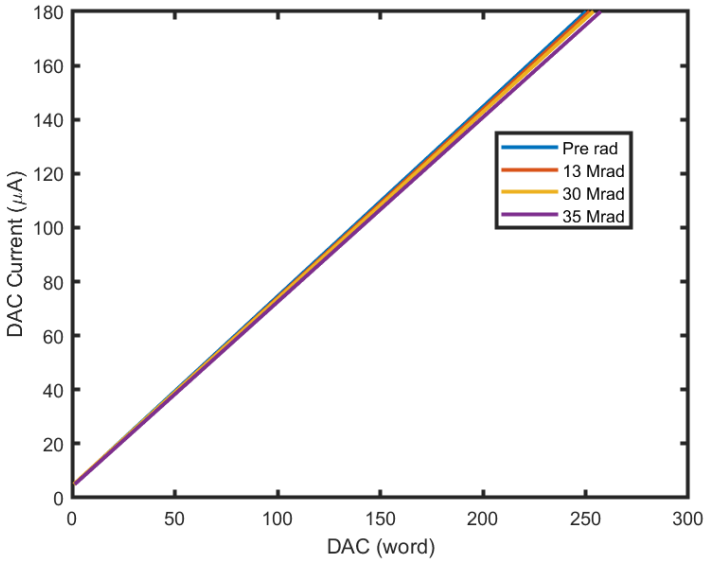


Figure 5.15: TID effect on preamplifier inputBiasTrans DAC

These coefficient variations also slightly impacted DAC conversion efficiency. Considering the full range of this 8-bit DAC, a DAC value of "255" corresponds to 183 μA with pre-radiation measurement, which decreased to 178 μA after 35 Mrad of TID, shows a decrease of 2.8% in the resultant current provided by the same DAC word at its input. It indicates that an increase of 2.8% to the DAC word is required to achieve the same desired current of 180μA.

A similar linear fit analysis of shaperBiasinputPair 8-bit DAC showed a current LSB of 168 nA with an offset coefficient of 3.3 μA during pre-radiation measurements. After a maximum dose of 35 Mrad, the current LSB decreased to 165 nA, and the dc offset decreased to 3.2 μA. This decrease translates to 1.7 % in the current LSB and a 4.5 % decrease in the offset coefficient.

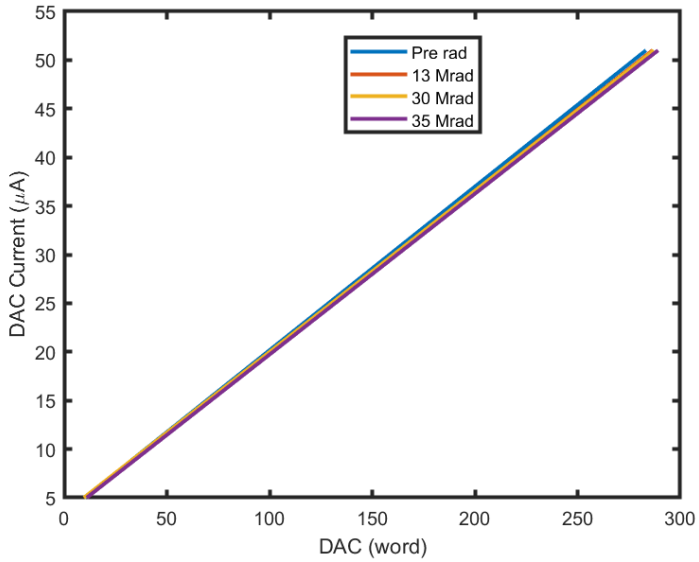


Figure 5.16: TID effect on shaperBiasInputPair DAC

The change of LSB and offset coefficients also slightly impact DAC conversion efficiency. Considering the full range of this 8-bit DAC, a DAC word of "255" corresponds to 46 μA with pre-radiation measurement and decreases to 45 μA after 35 Mrad of TID. This decrease translates to a maximum reduction of 2% in the resultant current provided by the same DAC word at its input. It also indicates that an increase of 2% to the DAC word is required to achieve the same desired biasing current output to the front-end.

5.6.3 Front-end channels TID effect

The VFAT3 front-end channels are injected with internal charge pulses and are configured in Medium Gain (MG) and 45 ns of peaking time. The TID effect is recorded by monitoring the mean threshold of all channels in charge units, as shown in Figure 5.17.

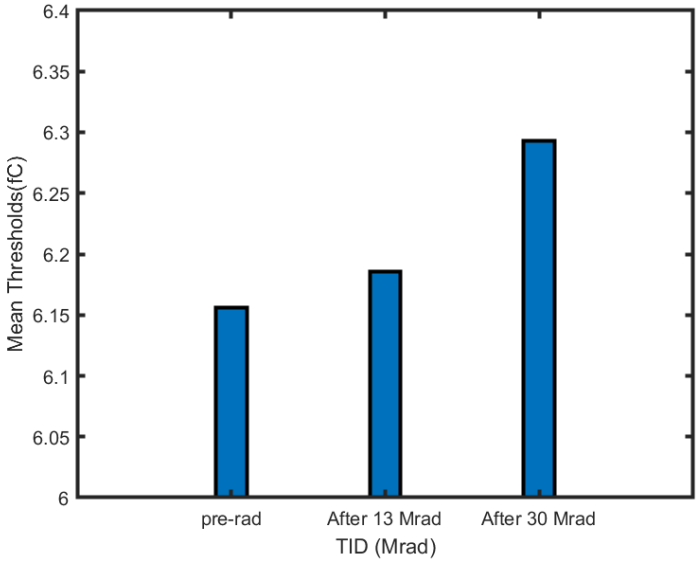


Figure 5.17: TID effect on mean thresholds of all channels

The threshold of a channel is obtained by making an s-curve fitted by an error function. The underlying algorithm is described in section 4.7. The mean threshold shows a slight increase with the TID. The pre-rad threshold is set at a mean of 6.15 fC for all VFAT3 channels, which increased to 2.2% after 30 Mrad TID. VFAT3 will receive a maximum of 1 Mrad TID over the ten years of LHC run; it means that the threshold variation would only be 0.07%, which is negligible. Besides, frequent in-situ calibration of front-end channel thresholds would be performed during the CMS operation to adjust and calibrate channel thresholds. It may be concluded that this threshold increase is so slight that it will not be observable during the VFAT3 operational lifetime in CMS.

The front-end channels also showed a similar trend in the Equivalent Noise Charge (ENC) measurements. An increase in the channel noise was observed after a total of 30 Mrad TID, as shown in Figure 5.18.

A pre-rad measurement with the same configuration showed an ENC of 0.14 fC, which increased to 0.2 fC after 30 Mrad TID. Interpolated to CMS GEM environment, the increase would be at the level of 1.3%. These measurements showed a slight variation in the applied biasing of the front-end DACS (<3%), which is insignificant compared to permissible operational biasing tolerances of 5%.

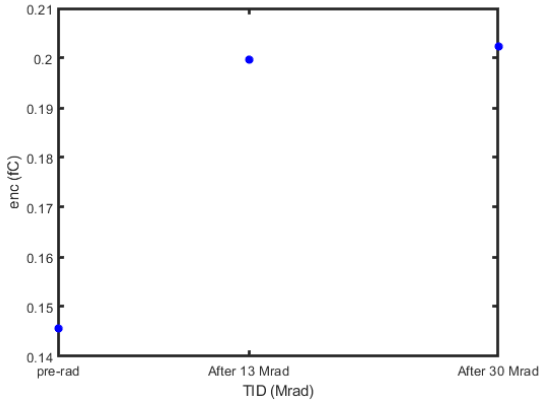


Figure 5.18: TID effect on mean ENC (fC) of all channels

5.6.4 VFAT3 communication failure and recovery

All along the irradiation, the communication with the VFAT3 has been monitored. Two VFATs have been irradiated up to 35 Mrad without showing any communication errors. Beyond 35 Mrad, the first device showed CRC errors and stopped transmitting data soon after. The second device also stopped communicating after 35 Mrad. Neither hard reset nor power cycle was succeeded in recovering the communication. After long room temperature annealing, one of the devices showed no recovery, and no improvement could be achieved even after weeks of wait. The second device showed slow recovery, and the communication was re-established after 60 hours of annealing. This post-rad annealing can be observed in Figure 5.19.

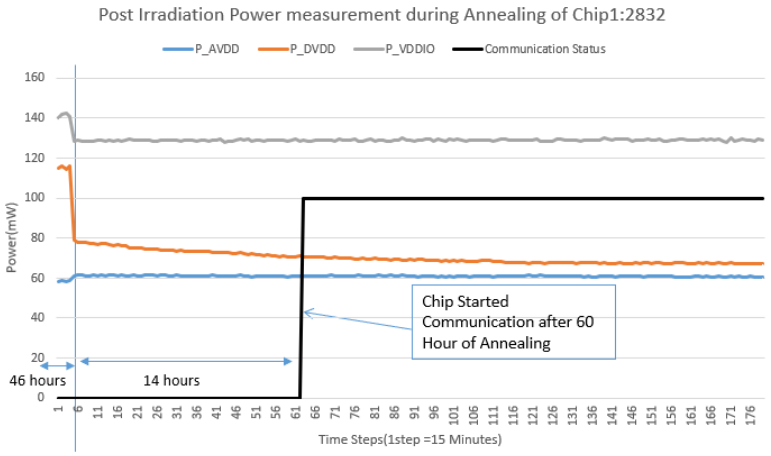


Figure 5.19: VFAT3 Post Irradiation Annealing Phase. This plot starts with excessive currents for DVDD and VDDIO just after the communication loss event. These measurements were taken after the completion of 35 Mrad of TID. The device was re-powered in the laboratory with onboard power monitoring enabled. Measurements show a slow recovery in the power domains of VFAT3. After 61 hours of post-rad annealing, the power consumption turned to the pre-rad normal state, and VFAT3 started to synchronize with the FPGA normally.

The TID results obtained for the analog submodules follow the results dis-

cussed in [94] with minor variations developed in the device characteristics. A fast dose rate of 1.84 Mrad/hr is used, which accelerated the e-h pair creation rate significantly, causing a sharp rise in the digital power of the chip just before the communication break.

During the first TID test, the power monitoring was unavailable due to the power configuration used to power the chip (All VFAT3 power domains set to 1.2 V). A 2.5V VDDIO (I/O power domain) is required to turn on on-board power monitoring circuitry. So later, a second TID campaign was launched (with VDDIO = 2.5 V) to irradiate the VFAT3 at 5.5 Mrad/hr. The idea was to irradiate the device to monitor both device power and communication until the device stops working. All three VFAT3 power domains (analog, digital, and I/O) were monitored to detect possible latch-up in the chip. The phase variation is also monitored with the help of FPGA serializers tap delay correction offsets. The data lines were monitored continuously for phase variation, and sampling was adjusted to sample the data at the mid-point of the eye diagram. The initial value of the tap delay corresponding to the mid-point of the data eye was recorded. Any variation in the tap-value corresponding to the mid-point of the data-eye is considered as phase variation.

The device was irradiated at a relatively higher rate of 5.5 Mrad/hr, reaching up to a total dose of 150 Mrad. It is observed that the phase margin of data eye for the TXD line varied linearly with TID up to 35 Mrad, and then a permanent communication loss was happened. The phase margin reduction is shown in Figure 5.20.

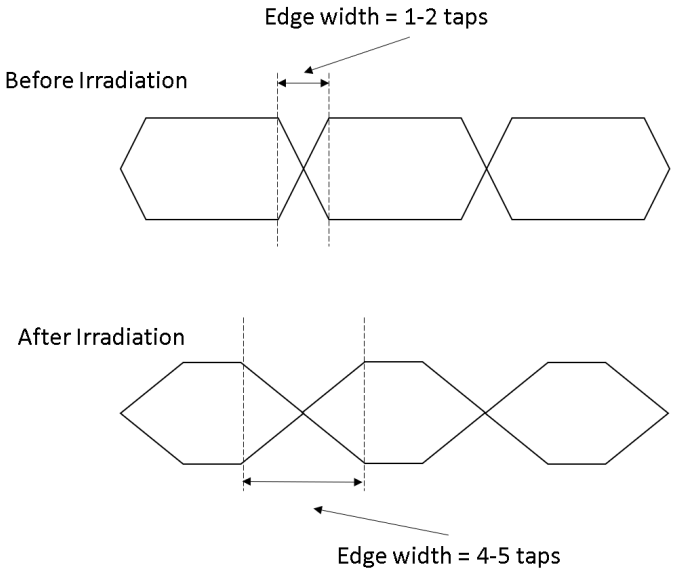


Figure 5.20: VFAT3 data-line phase margin reduction before and after TID. One tap delay is 78 ps in the chosen Kintex-7 FPGA serializers. The observed edge width was 156 ps before irradiation which was increased to 390 ps after irradiation. The figure is exaggerated to show the spread of edge width.

The reduction in phase margin may be related to an increase in threshold voltage mismatch and a rise of leakage current of I/O transistors in the VFAT3 device. The power monitoring for all three domains during the TID also showed an

abrupt rise of leakage current within different digital and I/O blocks of VFAT3 as shown in Figure 7.1.

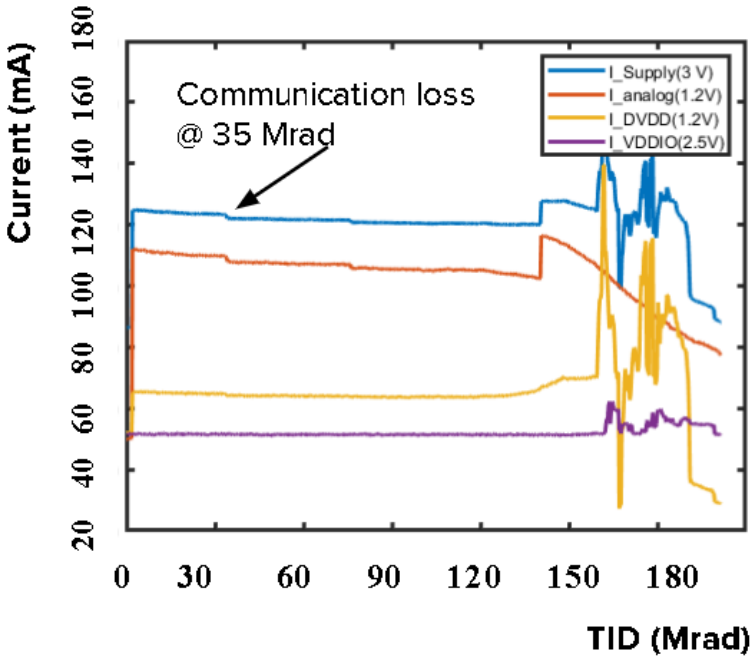


Figure 5.21: VFAT3 Current variation versus TID (Mrad)

This rise occurred way beyond the 35 Mrad device working limit. After 145 Mrad of TID, VFAT3 started to sink excessive currents, and internal damage happened. It is important to mention that this test was devised to obtain the absolute maximum limits of the device and should not be considered a critical problem in the device operation, which is working perfectly up to 35 Mrad of TID.

About the failure after 35 Mrad, two possible causes of failure could be SLVS transceiver and CMOS pads. The most probable reason could be related to CMOS pads instead of the SLVS. In fact those pads make use of thick oxide devices, which degrade much faster than thin oxide transistors that were used to build the SLVS and also the chip core [84].

5.7 VFAT3 single event effect test

In the previous section, we have shown that VFAT3 can operate up to a TID of 35 Mrad, far beyond the expected dose in the CMS muon system. We still need to check the single event effects on the device in the heavy-ion environment. If the heavy ion beam results in a higher cross-section than expected CMS hadrons cross-section, we might need to mitigate these effects during the device operations. The single event upset (SEU) test has become essential for electronics devices for the accelerator environment.

5.7.1 SEU test setup

The test has been conducted at the Cyclotron Resource Centre (CRC) of Louvain-La-Neuve (LLN), Belgium. CRC is a multi-beam electronic devices testing facility providing a Heavy Ion Facility (HIF), Light Ion facility (LIF), Neutron Ion Facility (NIF), and Gamma Irradiation Facility (GIF) all under the same premises. We opted for HIF irradiation which provides variable beam flux up to 1.5 $\times 10^4$ particles /s.cm^2. The beam homogeneity is $\pm$ 10 % on a 25 mm diameter, which is large enough to cover most of the larger micro-electronic devices. The available ions inside the cocktail are tabulated in the Table 5.1. A standard 24.2 $\times$ 24.2 cm

M/Q	Ion	DUT energy (MeV)	Range (μm Si)	LET $(MeV/(mg/cm^2))$
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

Table 5.1: Particle cocktail available at HIF LLN cyclotron [95]

test fixture is provided to mount the custom electronics and device under test. The test fixture can be tilted up to a wide angle of 60°, which helps get to different effective LETs avoiding the time-consuming step of frequent ion change. Different sealed flanges are provided to route the cables out of the chamber without vacuum loss. A custom-designed FMC flange is also used to route the FPGA FMC cables. An inside view of a test setup with VFAT3 custom hardware and long FMC cables is shown in Figure 5.22. The inner 90 cm FMC cable is mounted from the test board to a CERN custom vacuum flange. A second 90 cm of FMC cable is also used for outside connections from the vacuum flange to the FPGA board. The power is provided to the chip through BNC connectors mounted on

other flange provided by the facility. Water circulation is used to keep the device at 20°.

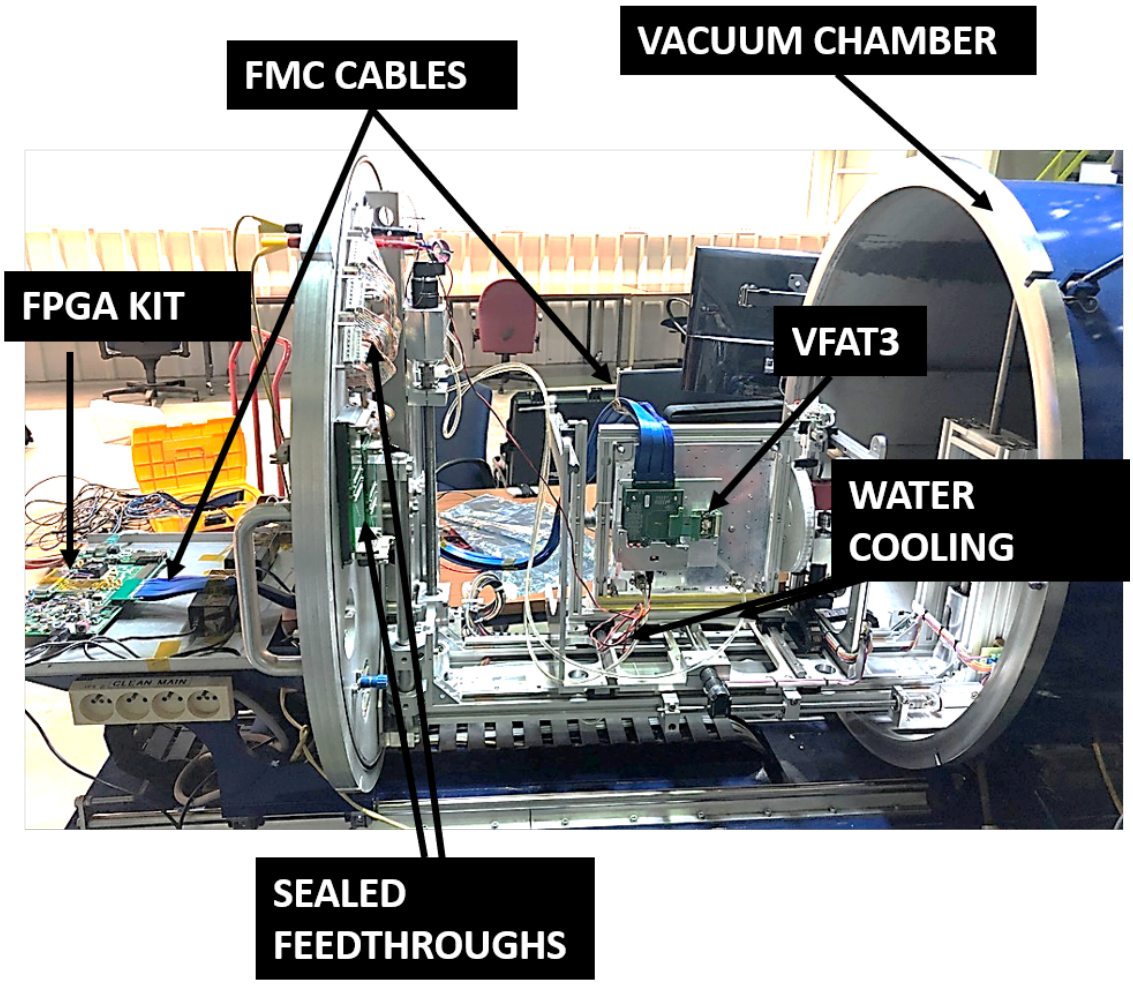


Figure 5.22: VFAT3 SEU test system installed at LLN Ion Beam Test facility. The VFAT3 hybrid with support board was mounted on a water-cooled metal plate. Two 90 cm FMC cables were used to establish VFAT3 and the external Kintex-7 FPGA link. A sealed FMC feedthrough was used for FMC cable connections, and a BNC feedthrough was used for power supply connections.

The beam alignment is done through a laser cross-hair, which aligns the device at the ion beam center precisely. VFAT3 beam alignment and laser cross-hair are shown in Figure 5.23.

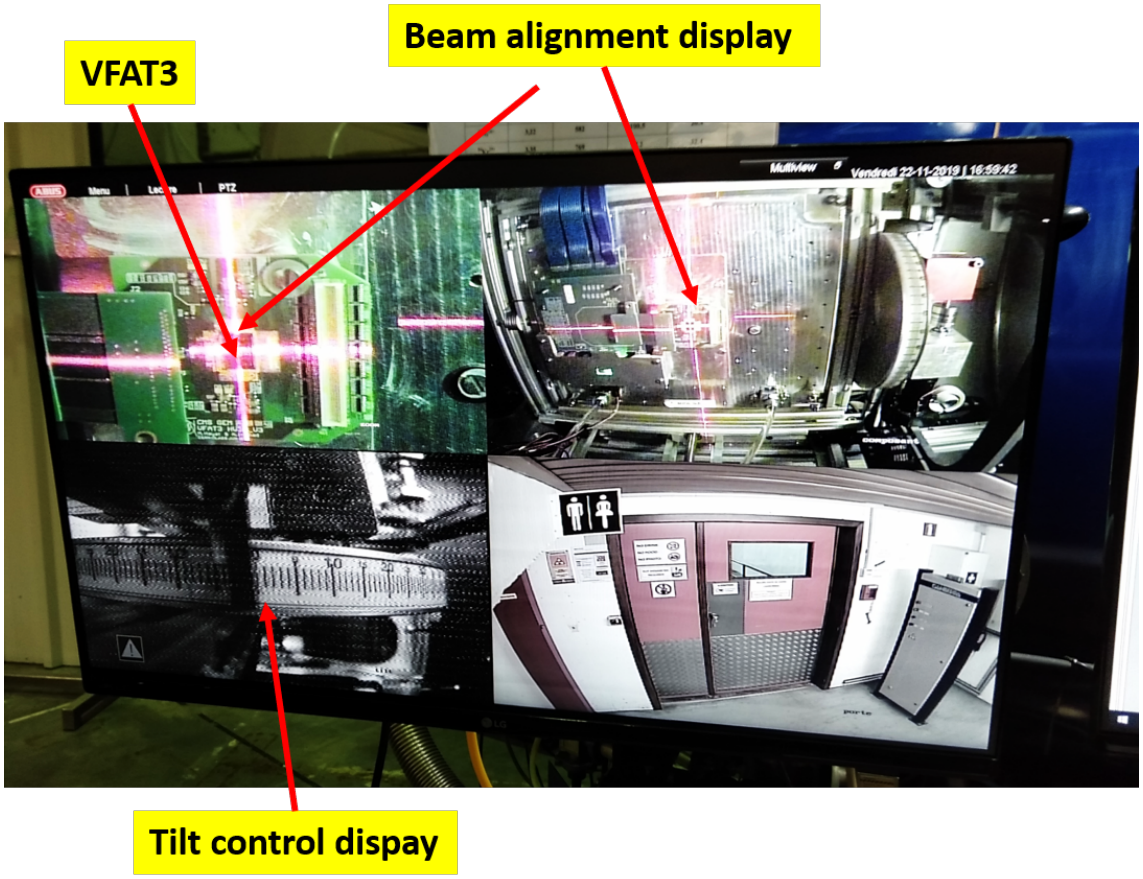


Figure 5.23: VFAT3 beam alignment through a laser cross-hair. A horizontal dial also indicates a tilt angle of the device support plate.

5.7.2 SEU test principle

Two types of SEU tests are normally performed on large devices. The first is the SEU test for the memory block, and the second is the SEU test for configuration registers. In the start, an appropriate ion species such as $^{58}Ni^{18+}$ with LET of 20.4 $MeV/(mg/cm^2)$) was selected, which could provide a sufficient number of upset events while keeping the functional interrupts and CRC errors at a minimum. In VFAT3, the memory test is not possible due to the continuous write of internal memories at LHC bunch crossing frequency. Although the register SEU test was performed, and saturation cross-section and threshold LETs were calculated. The test started with the writing of a known bit pattern to the registers before the beam. The device is then irradiated for a certain time to achieve defined fluence and collect sufficient bit-flip statistics. After stopping the beam, the registers were read back, and any bit flips were recorded. This procedure is repeated for all the desired ion species (LETs) until the threshold LET, and saturation cross-section for the device under test are obtained. The exposition time can be increased to enhance bit-flips statistics. Indeed the test should reflect sufficient recorded events to be statistically representative of the chip functionality.

5.7.3 VFAT3 configuration registers SEU cross-section

When a mono-energetic beam of particles irradiates the device under test, some particles may deposit enough charge in the sensitive regions to initiate an event (upset, latchup, or transient). The number of events N can be written as

$$N = \rho * n \tag{5.1}$$

where ρ is the event probability multiplied by the total number of particles n passing through the device. The above equation can be written in terms of event cross-section and the beam fluence. If A is the area of the device, then we can write the equation 5.1 as

$$N = (\rho * A) * (n/A) \tag{5.2}$$

$$N = \sigma * \Phi \tag{5.3}$$

Here, σ is the event cross-section with the area units, and Φ is the particle fluence expressed in units of particles per unit area. The cross-section depicts all the necessary information about a device to estimate the event rate in any environment. The event cross-section also relies on several parameters, such as:

- angle of incidence of the incoming particle
- the type and energy of the incoming particle
- the device temperature
- electric fields present near the sensitive nodes of the device.

A total of seven ion species were available at the facility on the test day, and all of them were used to obtain the VFAT3 registers bit-flip data. The 8^{th} measurement was also added by using the effective LET. For this 8^{th} measurement, the device was tilted at an angle of 60° to achieve LET_{eff} of 40.8 $MeV/(mg/cm^2)$) by using $^{58}Ni^{18+}$ with LET of 20.4 $MeV/(mg/cm^2)$). The effective LET is calculated by using the following formula:

$$LET_{eff} = \frac{LET}{cos\theta} \tag{5.4}$$

The irradiation with each ion species was repeated several times to increase the reliability of bit-flip statistics. Table 5.2 summarizes VFAT3 SEU test at LLN cyclotron. For each ion type, the table provides the tilt angle between the ion beam and the VFAT3. The device flux and the respected fluence, exposition time, and the number of bit-flips observed were recorded for each run.

From the table, accumulating the statistics over the several runs for each ion type, we can compute the event cross-section by using equation 5.3 as follows:

$$\sigma_3 = \frac{N_{events}}{N_T\,\Phi} \tag{5.5}$$

where,
Φ $= Total\ fluence$,

Ion	Tilt θ°	LET_{eff} $(MeV/(mg/cm^2))$	Flux $i/cm^2.s$	Reached Fluence (i/cm^2)				Elapsed Time (sec)				Flips			
				1	2	3	4	1	2	3	4	1	2	3	4
$^{13}C^{4+}$	0	1.3	1.5e7	3.37e7	—	—	—	2191	—	—	—	0	–	–	–
$^{27}Al^{8+}$	0	5.7	1.5e7	2.7e7	2.7e7	—	—	1766	1768	—	—	0	0	–	–
$^{36}Ar^{11+}$	0	9.9	1.5e4	1.5e7	1.5e7	—	—	970	973	966	—	1	0	1	–
$^{53}Cr^{16+}$	0	16.1	1.5e4	9e6	1.5e7	—	—	575	963	—	—	2	3	–	–
$^{58}Ni^{18+}$	0	20.4	1.5e4	5e6	5e6	9e6	5e6	316	327	583	326	2	1	6	1
$^{84}Kr^{25+}$	0	32.4	1e4* 1.5e4	5e6	5e6	5e6	—	495	329	330	—	3*	3	2	–
$^{58}Ni^{18+}$	60	40.8	7.75e3	5e6	5e6	5e6	—	647	647	641	—	3	4	6	–
$^{124}Xe^{35+}$	0	62.5	1.5e4	5e6	5e6	5e6	—	325	331	327	—	10	5	9	–

Table 5.2: VFAT3 configuration registers SEU data

$N_{events} = Number\ of\ flips\ recorded\ per\ ion\ species,$
$N_T \quad = Total\ count\ of\ triplicated\ registers,\ and$
$\sigma_3 \quad = Triplicated\ bits\ cross\_section$

The SEU cross-section as function of LET is expected to follow a Weibull function [84]. A typical Weibull curve for heavy ions SEU cross-section is shown in Figure 5.24. The cross-section as a function of the LET should exhibit a turn-on

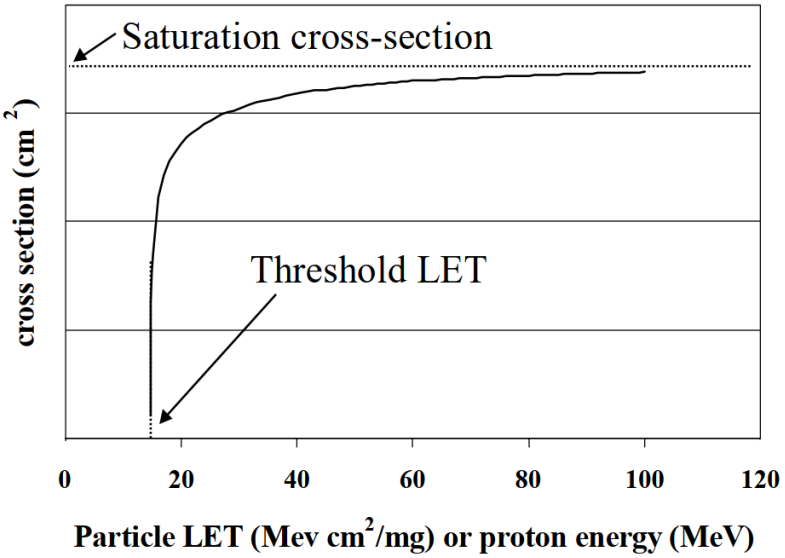


Figure 5.24: Typical Weibull fit showing Threshold LET and saturation cross-section [84].

rise defining a "Threshold LET" below which the circuit is not upset by the ion energy. Above this threshold energy, the upset rate first rises sharply and then converges to a saturation cross-section. This saturation indicates that all the sensitive nodes of the device are upset at this LET, and there is no new effect even if we are at higher ion energy. We can find the Threshold LET and saturation cross-section by using a cumulative Weibull function with four parameters.

$$\sigma = \sigma_0 \left(1 - exp\left\{-\left[\frac{E_{dep} - E_0}{W}\right]^s\right\}\right) \tag{5.6}$$

Here σ_0 is the saturation cross-section, E_0, and E_{dep} are the SEU threshold and

deposited energies, respectively. W and s are the scale and shape parameters of the distribution.

During the SEU test, the data is obtained as a function of LET. We need to convert these LET values into the deposited energy E_{dep} to use the Weibull fit function. As we know that at saturation cross-section, all sensitive regions of the device get upset, we can estimate the cross-sectional area of the sensitive region per node by dividing this saturation cross-section by the number of radiation-sensitive nodes of the device. This area multiplied by the device effective thickness provides the sensitive volume (SV) [96]. The VFAT3 cross-section is calculated at all the LETs, and Weibull distribution is fitted to calculate the saturation cross-section and threshold LET.

A cross-section plot for VFAT3, taking into account all the bit-flips transitions, is shown in Figure 5.25.

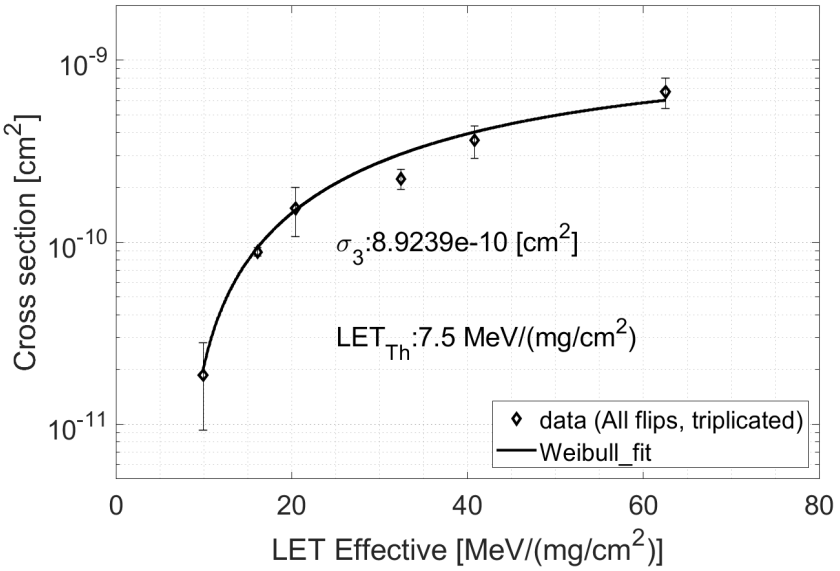
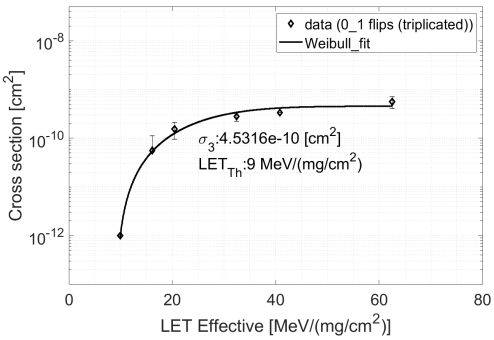
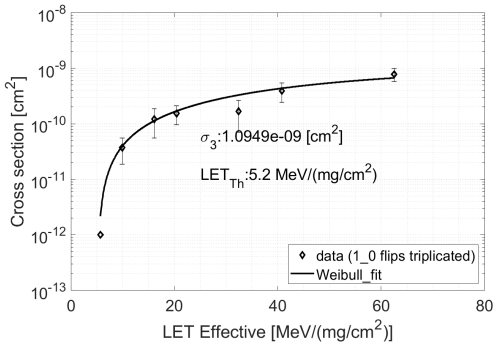


Figure 5.25: VFAT3 triplicated registers cross-section (per-bit) plot with Weibull fit, showing saturation cross-section and threshold LET

In total, 2385 triplicated bits were monitored during the test. Most of the VFAT3 configuration registers have a 16-bit width. To calculate the $0 \rightarrow 1$ and $1 \rightarrow 0$ transition cross-sections, a pattern of 0xFF00 was loaded to simultaneously calculate the cross-sections. The Figure 5.26 shows both cross-section plots for triplicated VFAT3 registers.



(a) VFAT3 configuration registers $0 \rightarrow 1$ flips cross-section plot.



(b) VFAT3 configuration registers $1 \rightarrow 0$ flips cross-section plot.

Figure 5.26: VFAT3 configuration registers $0 \rightarrow 1$ and $1 \rightarrow 0$ plots comparison.

VFAT3 is designed in 130-nm TSMC foundry and uses standard library blocks. VFAT3 cross-section results for all-bits, $0 \rightarrow 1$, and $1 \rightarrow 0$ are consistent with most of the SEU tests around the community [97, 98] . The table 5.3 lists all the cross-sections for VFAT3 triplicated registers for a comparison purpose. The $0 \rightarrow 1$

Transition monitored	Cross-section $[cm^2]$/bit	Comparison Factor
$0 \rightarrow 1$	4.5×10^{-10}	1
All transitions	8.9×10^{-10}	1.8 X
$1 \rightarrow 0$	1.09×10^{-9}	2.4 X

Table 5.3: VFAT3 triplicated register cross-section comparison

cross-section is smallest of all three, and $1 \rightarrow 0$ cross-section is largest among all cross-sections.

A comparison of $1 \rightarrow 0$ and $0 \rightarrow 1$ cross-sections is shown in Figure 5.27. The $1 \rightarrow 0$ cross-section is almost twice as compared to $0 \rightarrow 1$.

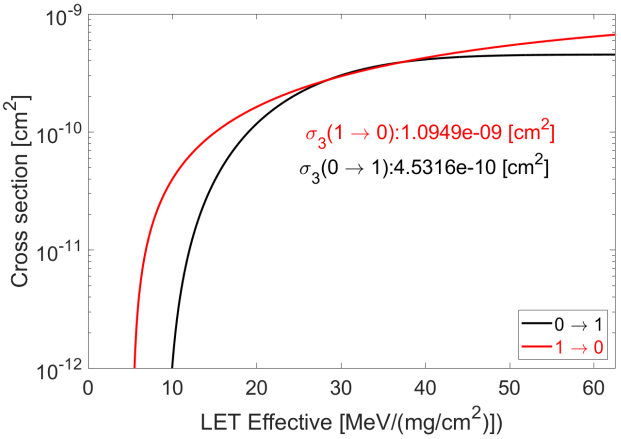


Figure 5.27: cross-section comparison between $0 \rightarrow 1$ and $1 \rightarrow 0$. The $0 \rightarrow 1$ cross-section is twice as low as compared to $1 \rightarrow 0$

Next, we discuss possible reasons why VFAT3 showed bit-flips in registers. VFAT3 registers are triplicated, so a single bit flip observed in the registers implies

that two out of three FFs have been flipped. Simultaneous corruption of two FFs of the triplicated register can happen if the two FFs are very close in the layout ($\leq$ 5.6μm), and the particle releases a large amount of charge. There was no control over the register placement tool when VFAT3 was designed. The average minimum distance between triplicated register cells, namely A, B, and C, was extracted to be around 5.6μm for *BC* cells, as shown in Figure 5.28.

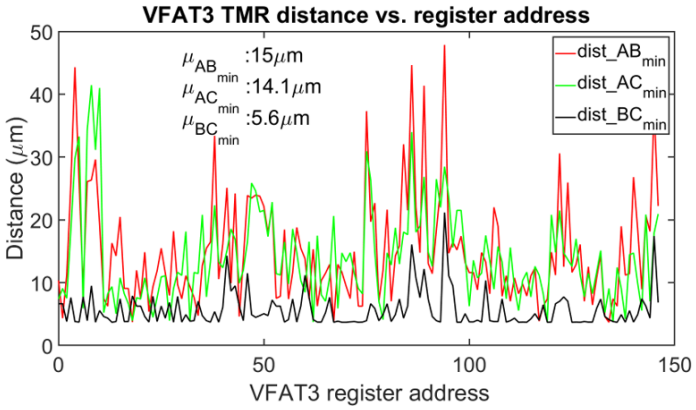


Figure 5.28: VFAT3 TMR minimum register distance versus register address. No controlled placement of triplicated registers was possible during VFAT3 design (2017) with Cadence Virtuoso placement. It reduced the effectiveness of TMR implementation.

In this case, the electron cloud is so large that multiple nodes can collect the charge. If we think that two particles corrupt the state of the two FFs of the same register within one clock cycle (3.25 ns or 25 ns), the probability of this event is extremely low.

5.8 VFAT3 SEFI effect (sync loss)

The Single Effect Functional Interrupt (SEFI) is defined as a soft error that causes the device to reset, freeze, or malfunction in a detectable way. However, it does not require the power cycling of the device to restore device operation. The SEFI is like an SEU in a critical part of the device, such as state machines, data paths, and clock trees that are not directly accessible through device control registers. The SEFI effect should be minimized to measure the desired SEU cross-section correctly.

During the VFAT3 heavy-ion beam test, a frequent synchronization loss phenomenon was observed, obstructing the data during SEU measurements. A synchronization loss was detected by continuously sending the "Sync_verify" fast command through comm-port to the chip. Each time, the chip replied with the "Sync_ack" character indicating that the link was good. The source of this synchronization loss was not obvious, and we categorized it as SEFI. The internal digital logic of the VFAT3 is triplicated to mitigate the SEU phenomenon, including the voter logic; the SLVS block itself is a current source-sink block that cannot be triplicated due to manufacturing limitations. A possible functional interrupt at a sensitive node of this block may lead to frequent synchronization loss with

the chip. Another possible explanation of the phenomenon is the noise glitch at sensitive clock tree nodes of the chip, causing to loss of the synchronization. The glitches on the reset line can also cause this effect. The asynchronous reset in the VFAT3 device is also triplicated, but the root of the signal is a single receiver. A particle passing across the transistors inside this block can potentially cause the flip of many flip flops (FFs). Moreover, it is not guaranteed that the buffers in the reset trees are sufficiently spaced in the layout to simultaneously avoid glitches inside the buffers. Since the width of the glitch is unknown, it can generate multiple effects: functional shift as a normal additional clock cycle or corruption of a flip flop (FF) value due to the short pulse on clock input.

5.9 VFAT3 synchronization loss cross-section

The SEU test system is designed to monitor both bit-flips and synchronization loss phenomenon during the beam. The firmware continuously verifies the synchronization with the chip by sending sync_verify fast commands continuously. The VFAT3 retains its configuration register settings unless a hard reset is asserted or we power cycle the chip. Both of these conditions are avoided during the test as these contribute to ruining the register SEU test. Once a synchronization loss is observed, the chip is re-synchronized by sending the three CCA characters, discussed in chapter 3, and the sync loss counter is also incremented.

The observed VFAT3 synchronization loss frequency during the HIF beam test is relatively high compared to the register bit-flip rate. The number of synchronization losses with different ion species is monitored, and exposition time is recorded to calculate the synchronization loss cross-section per device. The VFAT3 synchronization loss frequency variation is shown in the table 5.4.

Ion	Tilt	LET	Flux	Reached Fluence (i/cm^2)				Elapsed Time (sec)				Number of Sync loss			
	θ°	$(MeV/(mg/cm^2))$	$i/cm^2.s$	1	2	3	4	1	2	3	4	1	2	3	4
$^{13}C^{4+}$	0	1.3	1.5e7	3.37e7	—	—	—	2191	—	—	—	0	–	–	–
$^{27}Al^{8+}$	0	5.7	1.5e7	2.7e7	2.7e7	—	—	1766	1768	—	—	2	1	–	–
$^{36}Ar^{11+}$	0	9.9	1.5e4	1.5e7	1.5e7	—	—	970	973	966	—	0	2	0	–
$^{53}Cr^{16+}$	0	16.1	1.5e4	9e6	1.5e7	—	—	575	963	—	—	2	6	–	–
$^{58}Ni^{18+}$	0	20.4	1.5e4	5e6	5e6	9e6	5e6	316	327	583	326	6	3	5	3
$^{84}Kr^{25+}$	0	32.4	1e4* 1.5e4	5e6	5e6	5e6	—	495	329	330	—	5	2	6	–
$^{58}Ni^{18+}$	60	40.8	7.75e3	5e6	5e6	5e6	—	647	647	641	—	10	12	15	–
$^{124}Xe^{35+}$	0	62.5	1.5e4	5e6	5e6	5e6	—	325	331	327	—	11	13	12	–

Table 5.4: VFAT3 sync loss SEU data

Similar to the register bit-flip, by using equation 5.3, VFAT3 HIF sync loss cross-section is calculated and is plotted in the Figure 5.29.

The synchronization loss saturation cross-section is $2.44 \times 10^{-6} cm^2/device$, which is much higher than register cross-section. The exact volume of the sensitive nodes for synchronization loss is unknown, so the per device cross-section is chosen. Next, the extrapolation of synchronization loss cross-section to HL-LHC conditions is necessary. Suppose the extrapolation of results indicates more frequent VFAT3 synchronization loss rates in HL-LHC conditions. In that case, a dedicated GEM firmware adjustment might be required to recover the affected VFATs to reduce excessive CMS forced reset requests by the GEM detectors.

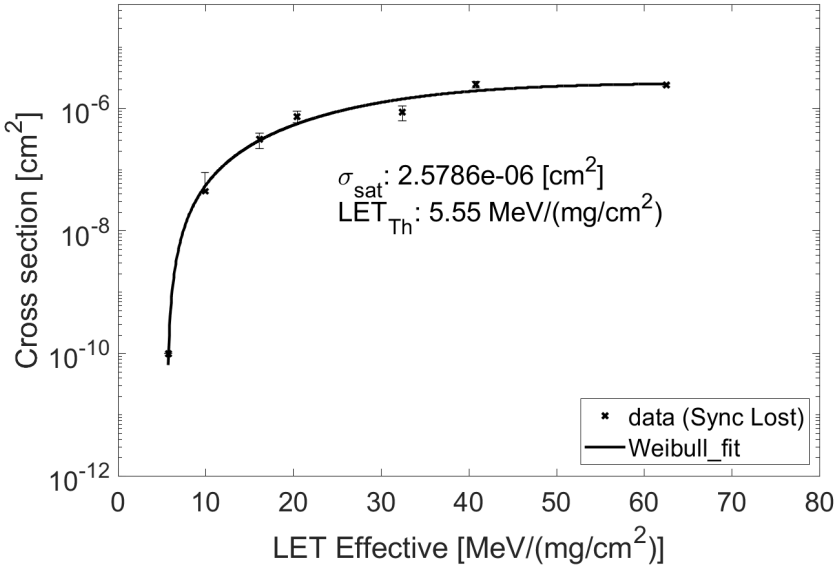


Figure 5.29: VFAT3 synchronization loss cross-section (per-device)

5.10 VFAT3 cross-section extrapolation to HL-LHC

It is essential to accurately estimate the HL-LHC upset cross-section for the VFAT3 device operation. We used a computational method to estimate SEU rates in the LHC environment first introduced by Federico et al. [96]. This method is based on the explicit generation and transport of nuclear fragments in silicon and explains their energy loss by ionization. To extrapolate the measured cross-section to the HL-LHC conditions, we do not need to simulate the underlying circuit, and only a reasonable guess of sensitive volume (SV) is required. The SV can be obtained by multiplying the cross-sectional area of the sensitive region per node obtained from Figure 5.24 with actual device SEU data. The simulation model begins with a simple step like critical energy and fixed SV. Later on the simplistic parameters are replaced with the actual heavy-ion Weibull fit parameters shown in Figure 5.25 and Figure 5.29. Assuming we have an SEU upset, a simplistic step-like model guarantees that ionization within SV exceeds critical energy.

We used Weibull fit to experimental data of heavy-ion SEU to quantify the SEU sensitivity of the device. We then convoluted the cross-section at threshold LET, extracted from Weibull fit with the simulated energy deposition probabilities for the proton of different energies, as shown in Figure 5.30.

The convolution of a cross-section from Weibull fit with the probability curve (Figure. 5.30) provides a fair estimate for the LHC SEU cross-section. The overlapping area between both curves provides the desired error rate projection. A graphical representation of this fact is shown in Figure 5.31.

Mathematically, SEU cross section in LHC environment can be computed as

$$\sigma_{LHC} = \sum_i P_i \Delta\sigma_i \frac{\sigma_0}{A} \tag{5.7}$$

where for each energy bin i we computed P_i, the simulated energy deposition probability from Figure 5.30 and the increase of sensitive area form the Weibull

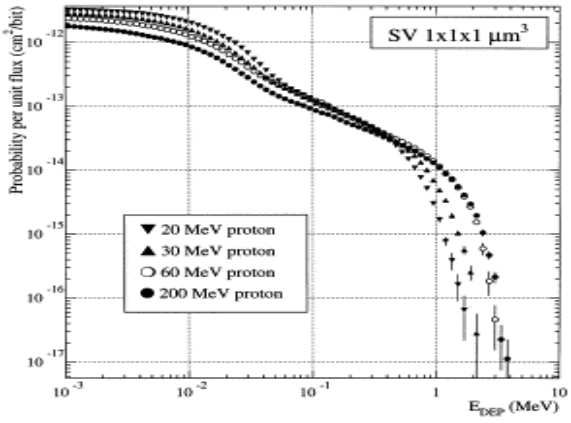


Figure 5.30: simulated energy deposition probabilities for protons of different energies in LHC environment [96].

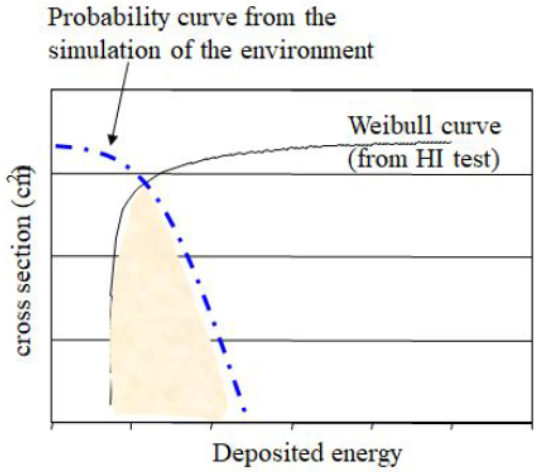


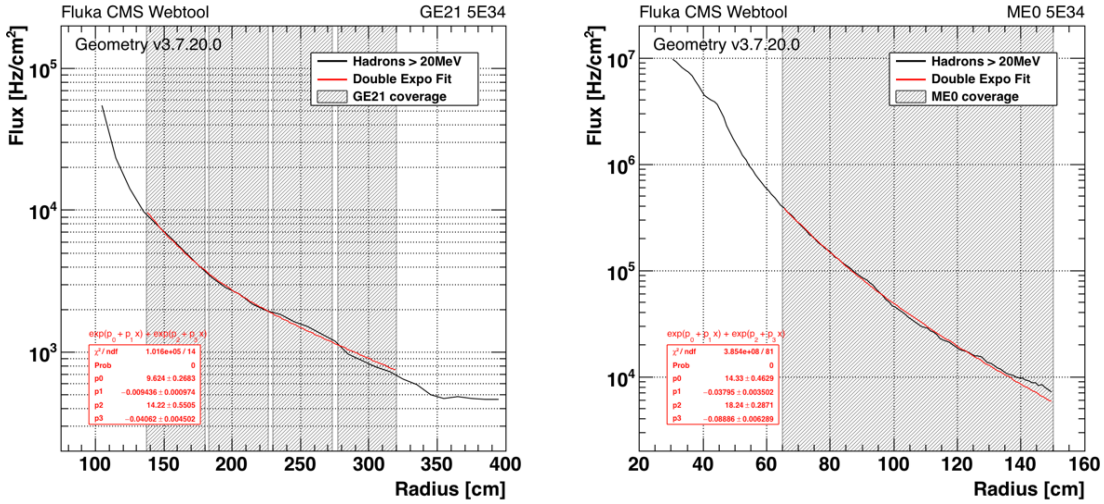
Figure 5.31: The convolution between the two plots, showing shaded area provides HL-LHC cross-section estimates.

distribution in the same energy bin, $\Delta\sigma_i = (\sigma_{i+1} - \sigma_i)/\sigma_0$. Using the sync loss cross-section Weibull parameters from Figure 5.29 , the equivalent 20 MeV proton cross-section (from computational method) is:

$$\sigma_{LHC} = 6 \times 10^{-14}[cm^2/Device] \tag{5.8}$$

The hadron fluxes for all three GEM stations, GE1/1, GE2/1, and ME0, are plotted using the FLUKA CMS web tool. The figure 5.32 shows hadron flux plots for two GEM stations.

The gray bands on all the plots indicate respected geometries chosen in FLUKA for GEM detector locations. The region $120 < R < 250$ cm corresponds to GE1/1, $137 < R < 320$ cm corresponds to GE2/1, and $65 < R < 150$ cm corresponds to ME0 geometry in CMS. The peak fluxes for GE1/1, GE2/1 and ME0 extracted from FLUKA plot data are $2.04 \times 10^4[Hz/cm^2]$, $9.7 \times 10^3[Hz/cm^2]$, and $3.87 \times 10^5[Hz/cm^2]$ respectively. The sync-loss rate per device in three GEM stations are calculated by multiplying the equivalent hadron flux mentioned in



(a) GE2/1 FLUKA simulation for Hadron (> 20 MeV) Flux

(b) ME0 FLUKA simulation for Hadron (> 20 MeV) Flux

Figure 5.32: CMS GEM Phase-2 Fluka simulation Hadron flux for $p > 20\ MeV$. The upgraded geometries are used to calculate these fluxes with 5-fold Luminosity increase as compared to phase-1 design values.

equation 5.8 with these three flux values to get:

$$\begin{aligned} SyncLossRate_{(GE1/1)} &= 1.22 \times 10^{-9} Hz\,; \quad (per\ device) \\ SyncLossRate_{(GE2/1)} &= 5.82 \times 10^{-10} Hz\,; \quad (per\ device) \\ SyncLossRate_{(ME0)} &= 2.32 \times 10^{-8} Hz\,; \quad (per\ device) \end{aligned} \tag{5.9}$$

Both GE/1 and GE2/1 consists of 3456 VFAT3 devices, and ME0 consists of 5184 VFAT3 devices. The expected sync loss rate, taken in account both endcaps are as follows:

$$\begin{aligned} SyncLossRate_{(GE1/1)} &= 4.29 \times 10^{-6} Hz\,; \quad (whole\ GE1/1\ system) \\ SyncLossRate_{(GE2/1)} &= 2.01 \times 10^{-6} Hz\,; \quad (whole\ GE2/1\ system) \\ SyncLossRate_{(ME0)} &= 1.2 \times 10^{-4} Hz\,; \quad (whole\ ME0\ system) \end{aligned} \tag{5.10}$$

The VFAT3 sync loss rates in HL-LHC environment are tabulated in table 5.5.

Detector	Minimum Time between Consecutive sync losses in the whole system
GE1/1	**65.6 hrs**
GE2/1	**138 hrs**
ME0	**2.3 hrs**

Table 5.5: VFAT3 sync_loss extrapolation to HL-LHC environment

The HL-LHC extrapolation shows that the VFAT3 synchronization loss phenomenon has very low cross-sections for all three GEM stations. Only the ME0 region indicates a large cross-section, leading to VFAT3 synchronization loss after

every 2.3 hrs of CMS operation. A CMS-wide global reset request could be generated to recover the GEM system if no other CMS detector requested global reset within the last 2.3 hrs. This sync-loss period is long enough, and in general, CMS asserts global resets after half an hour, which is sufficient to mitigate the issue.

5.11 Summary

The radiation tolerance of VFAT3 is tested in detail to ensure device qualification for HL-LHC operations in CMS GEM detectors. Two kinds of significant radiation damages may occur in the electronics, namely TID and SEU effects. TID effects are related to damage or deterioration in the device performance due to long-term exposure to a radiation environment. In contrast, single event effects (SEE) are related to the permanent device damage or temporary malfunction in the digital parts of the device due to a single energetic particle depositing its energy to the sensitive device nodes.

VFAT3 is exposed to up to 70 Mrad of TID initially with a mono-energetic X-ray beam in the CERN facility. The device showed an excellent tolerance to the radiation, and no significant deterioration was observed during the test. The I/O block of the chip showed sensitivity during the TID test. A sudden communication loss and synchronization issues were observed at 35 Mrad of TID. The interpolation of TID results to HL-LHC conditions showed that VFAT3 would perform without any issues in the CMS experiment environment, which would only accumulate a maximum of 1 Mrad of TID to the device over HL-LHC runs.

The SEU test is performed at LLN heavy-ion facility (HIF). The stability of the device in the presence of high energetic particles is recorded, and the SEU cross-section is calculated. The extrapolation to the HL_LHC cross-section is established. The VFAT3 registers are triplicated and showed low statistics of bit-flips (saturation cross-section: 6.1×10^{-10} cm^2/bit), a good indication of the robustness of the device against SEU effects. A synchronization loss phenomenon is observed during the ion-beam test, similar to communication break after TID dose. A cross-section is also calculated for this process. The observed frequency of sync-loss is much greater than SEU cross-sections, so an HL-LHC extrapolation is performed, and the worst scenario for ME0 indicated one sync loss after every 2.3 hrs. This sync-loss is easily recoverable as CMS asserts many global reset requests for all the detectors frequently, which will mitigate the issue without any additional firmware changes.

Chapter 6

VFAT3 integration and operation with GE1/1 detectors

6.1 Introduction

Before starting the mass production of the VFAT3 hybrid, the performance of the VFAT3 with the GE1/1 detector had to be verified. Beyond noise and efficiency measurements, the integration with the rest of the GE1/1 detector electronics also had to be verified. In addition, following the observation of unexpected channel loss with the VFAT2 during the two-year (2017-2018) Slice Test, a dedicated "Sustained Operation" campaign was launched to assess the behavior of the VFAT3 chip in case of potential detector discharges. This investigation led to a redesign of the GE1/1 VFAT3 hybrid.

Secondly, during the with-detector operation testing of pre-production hybrids, VFAT3 chip_ID bit-flip issue was observed. The investigations pointed to an under-optimized powering scheme of the VFAT3 on the GEB which was finally mitigated by the implementation of a multi-bit encoding scheme.

This chapter presents first some observations made with the VFAT2 during the Slice Test and the subsequent investigations with the VFAT3 regarding the damages produced by discharges in the Triple-GEM detector. The performance of the final VFAT3 hybrid design in terms of noise and efficiency with production GE1/1 detector are then discussed. Finally the issue and the mitigation of the VFAT3 Chip-ID bit flip are described.

6.2 GEM Sustained Operation study

The GE1/1 will be operated in a harsh radiation environment for extended periods. It was mandatory to evaluate the long-term operation of the detector electronics in a real CMS environment. In 2017, a GE1/1 Slice Test was performed in the CMS [99]. In this test, a set of five GE1/1 super chambers were installed in the CMS to acquire installation and commissioning expertise, prove the system operational conditions, and demonstrate the integration into the CMS online system. The name 'Slice Test' was originated from the fact that only a tiny slice out of the entire disk was populated with new GE1/1 detectors. It is essential to mention that VFAT3 was not available at that time, so VFAT2, the predecessor of

VFAT3, was used in these GEMs for charge readout. The input channel protection in VFAT2 and VFAT3 is of the same strength.

6.2.1 GEM Slice Test results

The crucial observations were taken during the Slice Test regarding high voltage discharge production in GEM detectors. Discharge propagation to the front-end hybrids and damages caused to the VFAT2 input channels were observed. Later on, several mitigation techniques are devised to achieve a simplified and most robust configuration, along with the redesign of the VFAT3 hybrid with additional protection, which will be discussed in detail in the following sections. The exact location of five super chambers installed during the Slice Test is shown in Figure 6.1.

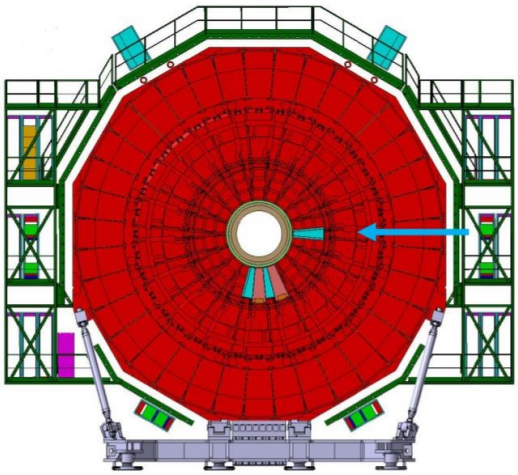
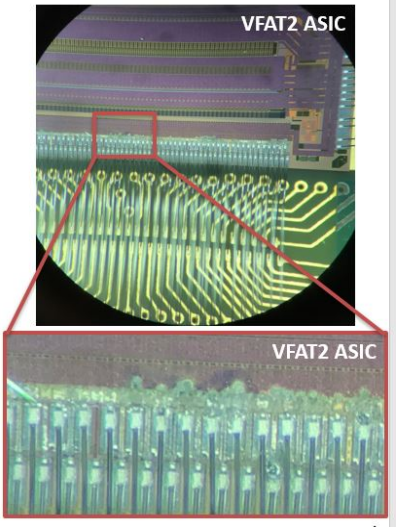


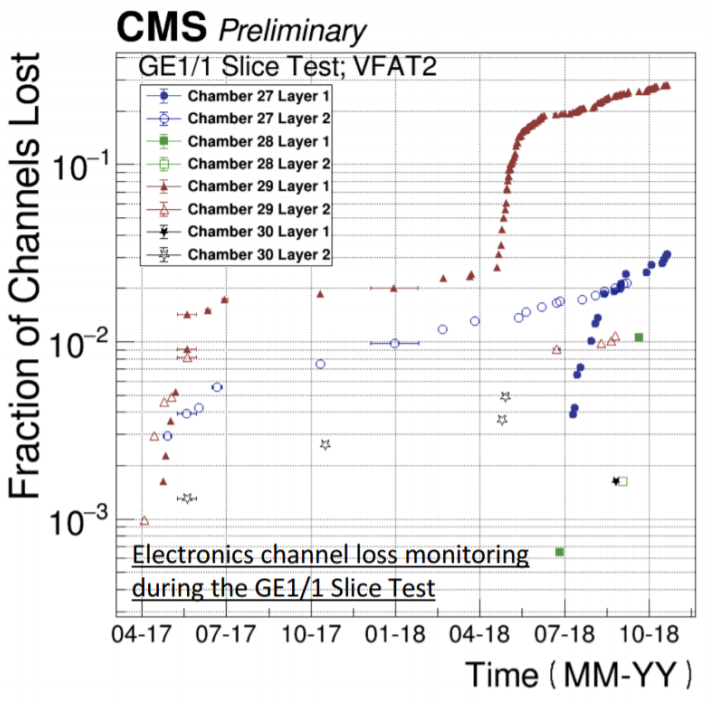
Figure 6.1: CMS GE1/1 GEM Slice Test with VFAT2 electronics (2017)

During the test, it was discovered that the VFAT2 had slowly accumulated irreversible channel loss. It was discovered that input channels were destroyed due to high voltage discharge propagation in the bottom GEM foil close to the readout strips, which eventually destroyed the VFAT2 input channels, as can be seen in Figure 6.2a.

The excess energy from the discharges caused damage to the silicon near the input channels of the VFAT2. A fractional channel loss data recording from April 2017 to October 2018 is also shown in Figure 6.2b. Eight different layers of four detectors were scrutinized during the Slice Test. All the observed chambers showed slowly growing channel loss, while chamber 29 layer 1 showed a much higher channel loss. The input protection circuits in both VFAT2 and VFAT3 are similar in protection strength. So it became necessary to evaluate the VFAT3 built-in protection capability against discharges as well. A VFAT3 Sustained Operation campaign was launched to assess the behavior of the VFAT3 chip and channel-loss probability in case of potential detector discharges.



(a) Damage produced by high voltage discharges to the input channels of the VFAT2 Hybrid. A microscopic zoomed snapshot taken from a damaged VFAT2 hybrid which is removed from slice test GEM detector



(b) GE1/1 channel loss timeline during Slice Test. A fractional channel loss is shown for 8 different layers of four detectors. All the chambers showed slowly growing channel loss with time. Only chamber 29 layer 1 showed much higher number of channel loss after the first quarter of 2018

Figure 6.2: VFAT2 channel channel damage and GE1/1 fractional channel loss during Slice Test beginning in 2017 [100].

6.2.2 VFAT3 channel loss investigation

A VFAT3 channel loss study was started to evaluate the effect of high voltage discharges on the front-end channels of the chip. Since VFAT3 has internal protection diodes, a VFAT3 hybrid without any external components was selected as a baseline for comparison with new hybrids with external protection components. This baseline hybrid is called HV3b_v2, an acronym for "Hybrid with VFAT3b".

As the first step of the VFAT3 channel loss study, the protection capability of the HV3b_v2 hybrid was measured. A custom discharge circuit was designed to produce GEM-like discharges with more control over discharge energy. A block diagram of the used discharge circuit is shown in Figure 6.3.

A DC power supply provides a stable fixed high voltage (HV) of 500 Volts. A capacitor bank C is charged through a series resistor of $1\,\mathrm{G}\Omega$. A discharge tube with a working voltage of 460 V is used to generate the desired discharge pulses. The discharge tube charges up to the threshold voltage and then discharges through the input VFAT3 channel, transferring the energy stored in the capacitor bank C to the VFAT3 input channel. As soon as the tube discharges, the tube voltage rises sharply, and a continuous train of discharge pulses is pro-

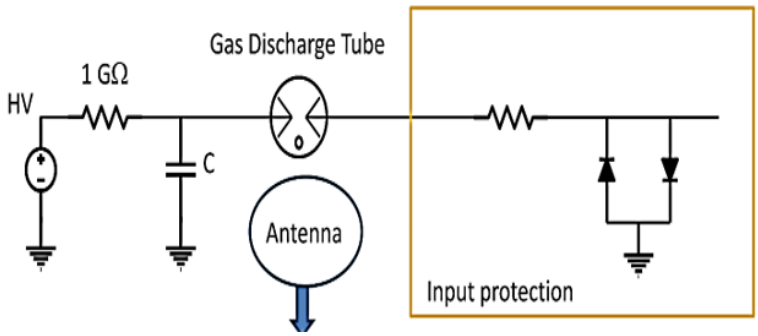
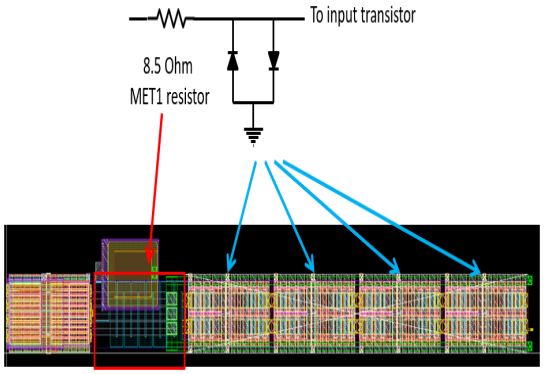


Figure 6.3: Discharge circuit schematic used to establish the VFAT3 baseline hybrid HV3b_v2 channel protection.

duced. The function of the 1 GΩ series resistor is to control the charging time and thus resulting pulse frequency.

Although VFAT3b had built-in input protection diodes and series resistor, yet this protection proved to be insufficient and worked only up to 28.2 µJ of discharge energy produced by the test circuit of Figure 6.3. The small internal series resistor could not dissipate discharge energy and burnt away quickly. A zoomed layout of the VFAT3b internal protection circuit and microscopic picture of the damaged internal series resistor is shown in Figure 6.4.



(a) VFAT3 internal protection circuit consists of standard protection diodes and 8.5 Ω MET1 series resistor

(b) The discharge energy is dissipated in the internal series resistor, and if this energy is greater than a certain threshold (28.2 µJ), the resistor burns.

Figure 6.4: VFAT3 internal protection circuit (a) and resistor damage due to laboratory discharges (b).

Multiple discharges were injected into VFAT3 front-end channels until the channel became unresponsive. The number of discharges for which a channel remained intact (N_d OK) is also counted. The number (N_d Fail) indicates the number of discharges contributed to damaging a channel. An average threshold discharge energy of 28.2 µJ is defined for the baseline hybrid, which showed its channel damage after the first single discharge.

C [pF]	V_d [V]	E (μJ)	N_d OK	N_d FAIL
220	460	23.3	26	0
242	460	25.6	25	0
267	460	28.2	1	3
330	460	34.9	1	2
440	460	46.5	0	1

Table 6.1: HV3b_v2 baseline hybrid discharge protection capability. The discharge energy is calculated by using HV Capacitor in the discharge circuit and discharge tube working voltage ($E = \frac{1}{2}CV_d^2$) is evaluated.

The energy stored in the GE1/1 GEM detector and transferred to individual channels is a complex phenomenon. It depends on the discharge propagation between different layers of triple GEM, applied voltage, and the gap between different layers of triple GEM foils. A simplistic model of parallel plate capacitor is adopted to estimate energy stored in GEM foil during discharge. A large capacitor is formed between readout strips and the bottom of the GEM foil facing them, called GEM3 bottom. The total capacitance between GEM3 bottom and readout strips can be evaluated by using the simple formula:

$$C = \frac{k\epsilon_0 A}{d} \tag{6.1}$$

where $\epsilon_0 = 8.854 \times 10^{-12} F/m$ is the permittivity of vacuum and k is the relative permitivity of dielectric used. In case of GEMs, k = 1.00054 for air is used. Using surface areas of 0.345 m^2 and 0.5 m^2 for short and long GEMs and d = 1 mm gap between GEM3 bottom and readout strips, GEM capacitance amount to:

- $C_{GEM_s} = 3\ nF$; (A=0.345 m^2, d=1 mm), short GEM
- $C_{GEM_l} = 4.4\ nF$;(A=0.5 m^2, d=1 mm), Long GEM

where C_{GEM_s} and C_{GEM_l} are the computed GEM foil capacitance for shorter and long detectors, respectively. The corresponding GEM energies can be computed by using the following formula:

$$E = \frac{1}{2}CV_d^2 \tag{6.2}$$

The major contribution in GEM discharges is from GEM3 bottom voltage, which is $V_d = 430V$. However, it is also observed that in case of worst discharges, a virtual short is observed between GEM3 bottom and top GEM layers, raising the maximum voltage at GEM3 bottom up to 2000 V. A detailed discussion of GEM discharge propagation and relevant plots are discussed in section 8.6. So using the Eq. 6.2 for both of these V_d values, GEM discharge energies E_{d_s} and E_{d_l} have the ranges $0.277 \leqslant E_{d_s} \leqslant 6mJ$ and $0.410 \leqslant E_{d_s} \leqslant 9\ mJ$ for short and long GEMs, respectively [100]. These computed discharge energies stored in GE1/1 foils are certainly far greater than the 28.2 µJ limit for HV3b_v2, the baseline hybrid for GE1/1 GEM detector. There was a specific requirement of increasing the input protection capability up to twice the minimum $E_d(GEM)$ to withstand several most probable GEM discharges. We proposed two different protection

schemes for new VFAT3 hybrids, keeping in mind the limited available space on the hybrids for protection components. The first was with the external series resistors and the other with the external ESD protection diodes. One can use a combination of both the protection approaches in a single scheme, but the available hybrid space limited the choice. The version with an external series resistor is HV3b_v3, and the one with external protection diodes is HV3b_v4.

Similar to baseline version HV3b_v2, bith new hybrid versions were tested with the high voltage circuit shown in Figure 6.3. Both upgraded hybrids were struck with 500 discharges with 470 μJ, and both the hybrids shown no signs of damage. Then by increasing the discharge energy up to 920 uJ, both hybrids showed channel damage. A comparison of protection capabilities for both hybrids with external protection is shown in Table 6.2.

	330Ω resistor	**ESD protection**
Break-down energy	800 μJ	$815 - 920\ \mu J$
Long test $(470\ \mu J)$	Channel Ok after 500 discharges	Channel Ok after 500 discharges
Noise	$750e^-$ (with simulation correction)	negligible
Cross talk	11 % (from simulation)	<0.8 %

Table 6.2: Protection comparison between HV3b_v3 and HV3b_v4 of hybrids with the laboratory setup.

The final selection was dependent on the performance of hybrids with actual GE1/1 detectors. Unfortunately, the HV3b_v4 showed 100 % damage probability with the GE1/1 detector. Further investigations revealed that the HV3b_v4 with external diodes showed sudden damage to the input channels because GEM discharges may last micro-seconds which are long enough to destroy the external protection diodes.

The ENC measurements for all three versions of the hybrids were also compared. It ensured that hybrid Version-3 noise was within the limits of 6000 e^- with the detector operation having a capacitance of 20 pF. The ENC comparison is shown in Figure 6.5.

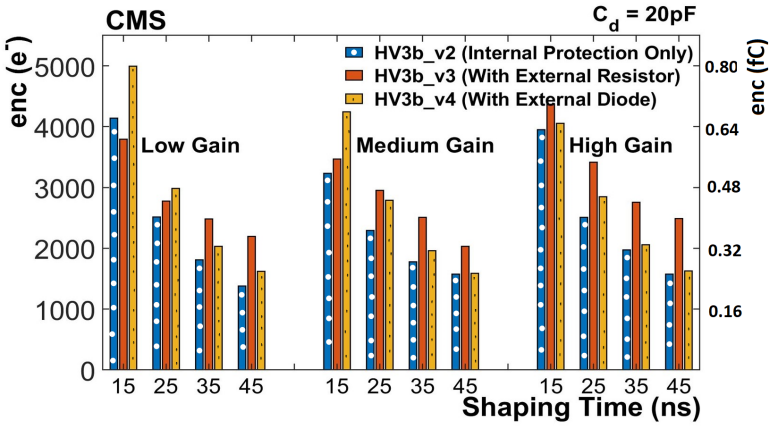


Figure 6.5: ENC comparison for VFAT3 hybrids with different protection circuits

The noise increase shown by HV3b_v3 is not significant compared to the robustness achieved for GE1/1 operation. The discharge protection summary for

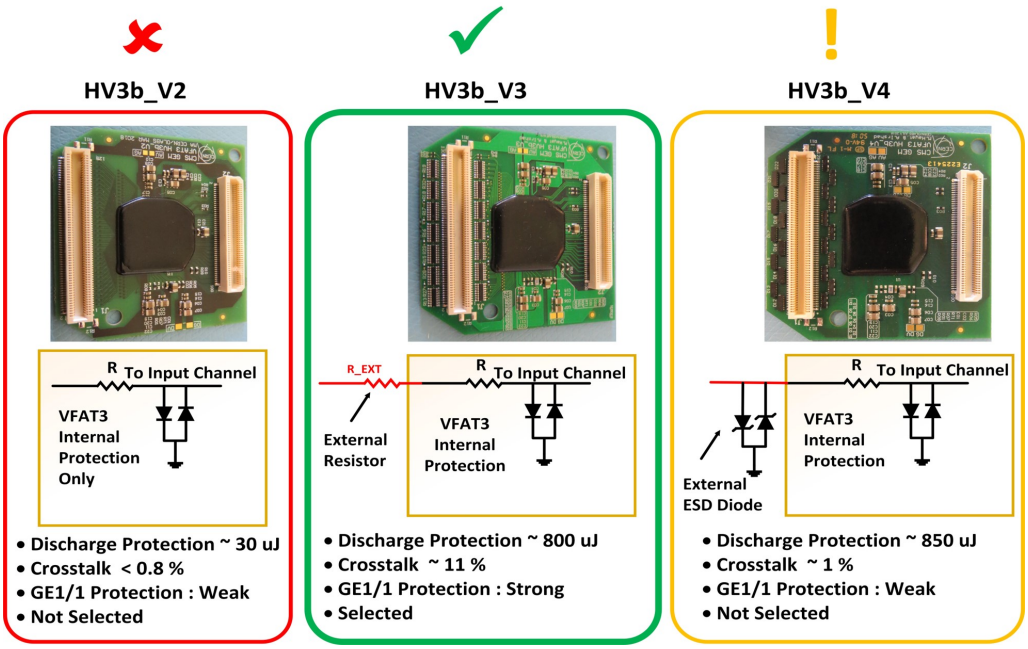


Figure 6.6: Hybrid discharge protection comparison

all hybrid versions is summarized in Figure 6.6. The HV3b_v3 showed a significant reduction in damage probability compared to HV3b_v2 and HV3b_v4 of hybrids. With the appropriate selection of external series resistor, the discharge probability with GE1/1 detector reduced to 3 % only. The choice of an external series resistor is also explained in detail in the section 6.2.3

6.2.3 Final GE1/1 Hybrid configuration

The selection of the HV3b_v3 hybrid was made, but the choice of resistor value further depends on the optimum values of VFAT3 cross-talk and efficiency of the GEM detector. Figure 6.7 shows the robustness of the HV3b_v3 hybrid against the discharge energy as a function of the external series resistors.

Both internal and external resistors share the discharge energy. The larger the external resistor, the more significant the proportion of the energy drop in the external resistor, and thus smaller will be the damage to the VFAT3 input channels. Two values of external series resistor were initially chosen for further experimentation with the GEM detector, 330Ω and 470 Ω. Different configurations of hybrid series resistors and GEM high voltage filter resistors [101] were experimented to achieve optimal GEM performance with minimum discharge probability. Figure 6.8 shows a VFAT3 channels damage probability plot instrumented on a GE1/1 detector for different configurations of VFAT hybrid, detector HV filter, and GEM electric field values.

A High voltage filter circuit is a crucial component of each GEM detector to reduce the HV noise in the GEM system. This circuit contains HV capacitors which also contribute to store GEM discharge energy and contributes to VFAT3 channel damage. The selection of optimum values of filter components is a trade-off between GEM performance and VFAT3 damage probability. Both baseline configuration-1 with HV3b_v2 and configuration-4 with HV3b_v4 pro-

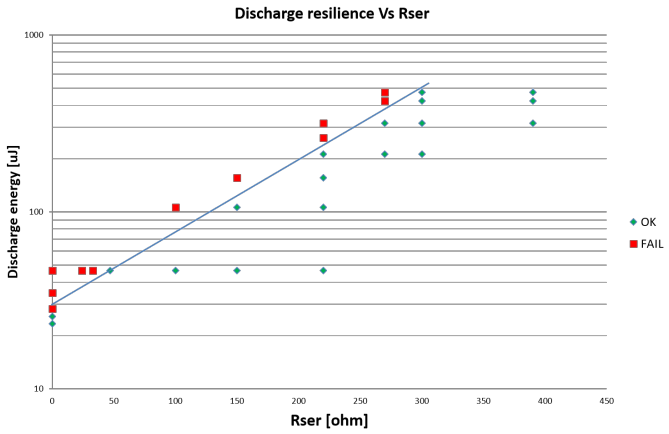


Figure 6.7: Robustness of HV3b_v3 hybrid against the discharge energy as a function of the external series resistor. A safe region of operation for the VFAT3 hybrid can be selected if we use the higher value of the series resistors. Nevertheless, cross-talk and efficiency reduction limit the choice of higher values.

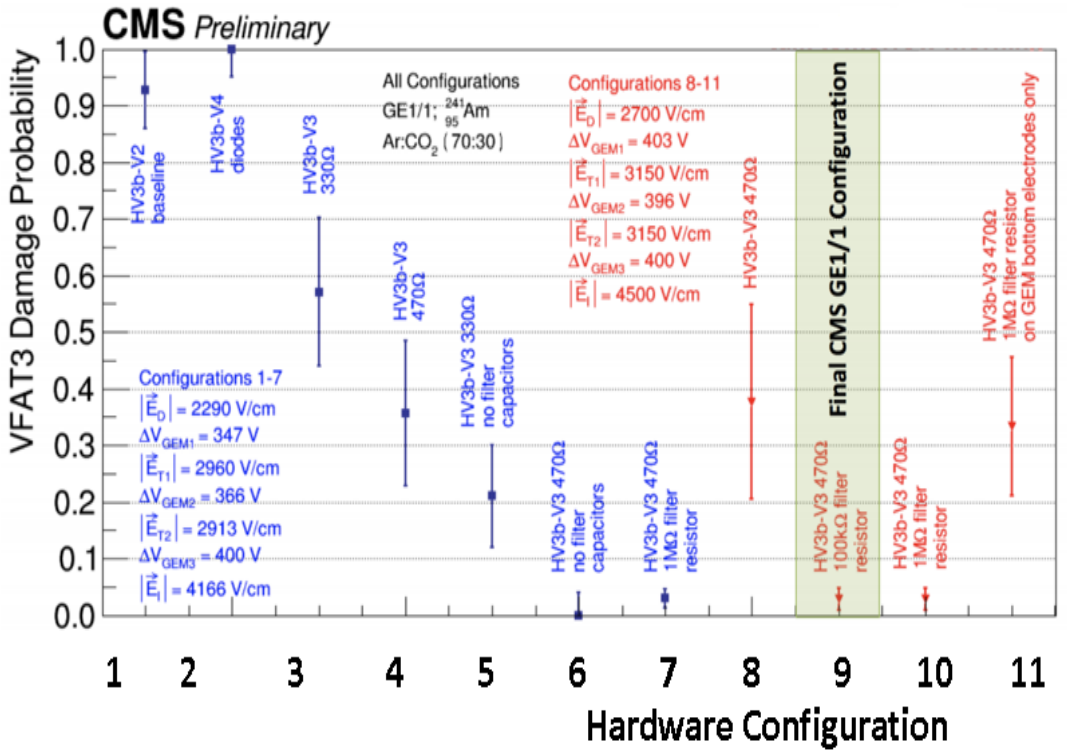


Figure 6.8: Different configurations of HV3b_v3 hybrid series resistor, GEM HV filter components and GEM gain parameters. The final chosen configuration is number 9, providing minimum damage probability with optimum GEM efficiency.

vided much higher damage probabilities of 93 % and 100 %. Next comes the configuration-3 with HVb_v3 of hybrid having 330Ω series resistors. This configuration significantly reduced the damage probability to 57 %. Then a change of series resistor value in the hybrid from 330 Ω to 470 Ω was made, which re-

sulted in further reduction of damage probability. Thus in configuration-4, with 470 Ω resistors, a damage probability of 35 % is achieved. The hardware configurations 1 to 4 lead us to select HV3b_v3 as a final choice for the GEM system. Next, configurations-5 and -6 were used to understand the effect of the GEM High Voltage (HV) filter circuit. Both these configurations provided a further reduction in damage probability. The configuration-5 provided 22 % and configuration-6 showed 0 % damage probability. However, the removal of the HV filter increased system noise levels. However, configuration-9 was the best acceptable scheme that used the HV3b_v3 hybrid with 470Ω series resistor and 100 kΩ HV filter resistor. The damage probability was reduced to 3 % with this combination. This trade-off is accepted to achieve maximum efficiency with a small channel loss probability [102].

6.3 VFAT3 Noise analysis with GE1/1

The most important characteristics that define the collective performance of the detector with readout ASIC are the ENC and the efficiency measurement. In the GE1/1 system, ENC is measured by injecting internal calibration pulses to the VFAT3 hybrids. An internal charge pulse is applied to all the VFAT3 channels one by one and measures the resultant hit efficiency from the built-in discriminator block. This procedure (S-curve) is explained in details in sections 4.7 and 4.8.

GE1/1 GEM detector production is subdivided into eight quality control (QC) tests, QC 1 - 8. The two last tests involve the complete electronics chain, including VFAT3. The noise results from these two steps are significant to estimate the performance of VFAT3 in a whole GEM system. QC7 is a detector electronics connectivity test. It is performed with full electronics but without detection of incoming particles. The ultimate qualifying test is QC8. Up to 15 super chambers can be tested at the same time in a large cosmic stand. In QC8, including the QC7 routines, the detection efficiency of the entire detector is measured as a function of the HV. QC8 is the most reliable and comprehensive test before integrating the detector in the CMS at LHC point-5 (P5). A comparison of the ENC of chamber GE1/1-X-S-INDIA-0006, installed in CMS in July 2020, in the three set-ups, QC7, QC8, and P5, is shown in Figure 6.9.

The mean ENC of ∼0.4 fC is achieved in the final plot at P5, an excellent noise level for the detector system. The measurements at QC7 also show a similar spread with slightly increased noise. This increase is justified as QC7 grounding is not optimal as in P5. The measurements in QC8 showed slightly more noise than QC7 and P5 measurements with an ENC of 0.6 fC. This high noise is explained by the low-quality grounding and noise introduced by photo-multiplier tubes in the proximity of the detectors.

The low noise achieved in the final system was due to an adequate shielding at P5 blocking unwanted electromagnetic interference (EMI) cross-talk. Another ENC plot for the same detector is also shown in Figure 6.10.

This plot shows the noise level contribution by individual VFAT3 hybrids to the detector. This plot also shows similar noise measurements. As expected, the P5 measurement resulted in the lowest noise levels, and QC8 measurements showed maximum noise levels. A mean noise of 0.4 fC is obtained in P5 mea-

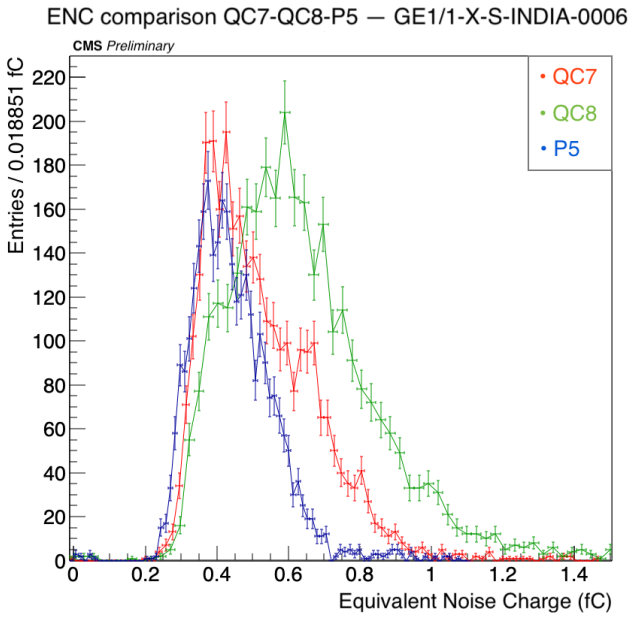


Figure 6.9: VFAT3 ENC comparison in QC7, QC8, and P5 for GE1/1-X-S-INDIA-0006 chamber which has been installed in CMS. These distributions compare ENC measurements of the all 3072 channels of the detector.

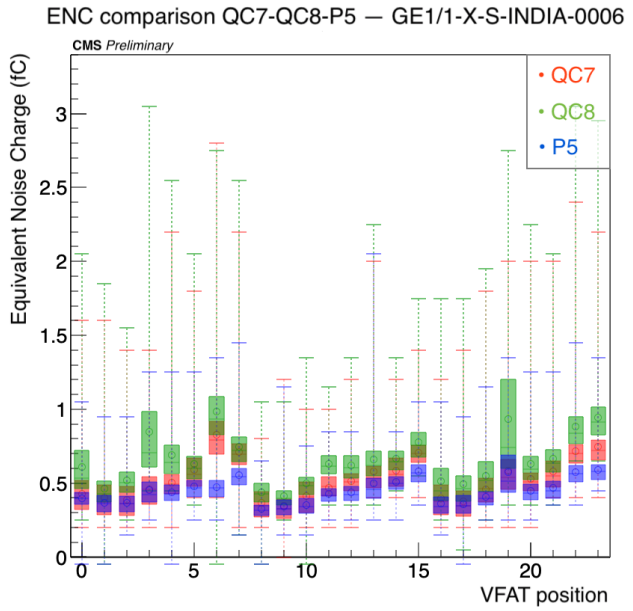


Figure 6.10: VFAT3 ENC comparison in QC7, QC8, and P5 per VFAT3 hybrid as a candle plot. The boxes represent the 50 % of the channels and the bars 100 % of the channels.

surements, which is consistent with the measurements shown in Figure 6.9. A staircase noise pattern reflects the slight capacitance difference between larger and smaller parts of the GE1/1 trapezoidal detector. The readout strips on the larger side have a slightly larger area, leading to an increase in the capacitance of these strips. The 8×3 arrangement of VFAT3 hybrids on the GEM detector is shown in section 2.9, which is perfectly consistent with the observed staircase

pattern.

6.4 GE1/1 Efficiency measurement with VFAT3

The efficiency measurements of GE1/1 with VFAT3 are shown in Figure 6.11 and Figure 6.12 with a long (GE1/1-X-L-CERN-0035) and a short (GE1/1-X-S-BARI-0001) chamber, respectively. Efficiency per VFAT partition (1D plot) is obtained from a cosmic run in the QC8 cosmic stand. The gas mixture of Ar/CO_2 (70/30) and an average effective-gain of (1.5 - 1.8) $\times$ 10^4 were used.

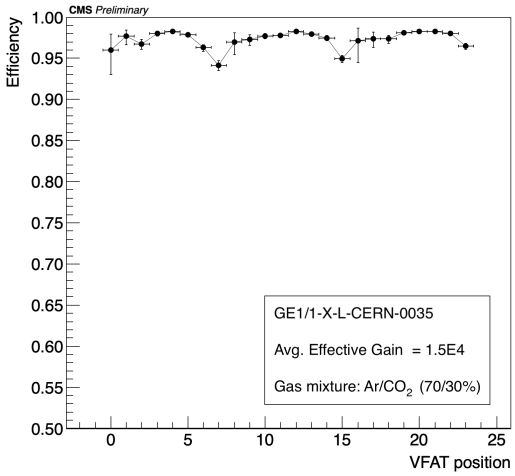


Figure 6.11: GE1/1 efficiency measurement plot for long GEM and VFAT3 hybrid. The detector used is GE1/1-X-L-CERN-0035

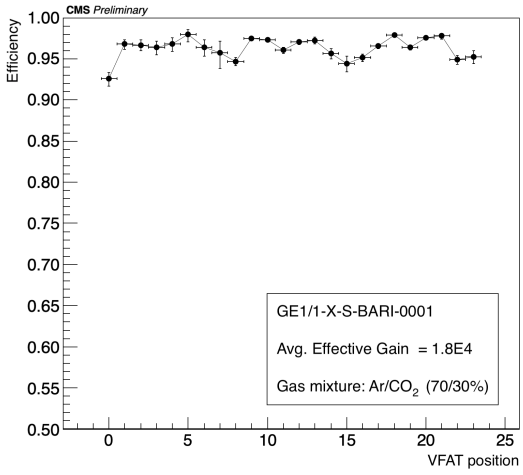


Figure 6.12: GE1/1 efficiency measurement plot for short GEM and VFAT3 hybrid. GE1/1-X-S-BARI-0001.

Both detector variants showed efficiency up to 98 % with cosmic rays. A slight drop in efficiency is visible on both plots in some positions. Those correspond to VFATs located along the edge of the GE1/1 detector. Some inefficiency can be due to the geometrical acceptance of the cosmic stand (slight misalignment of PMTs).

6.5 Chip-ID Multi-bit encoding

A 32-bit electrical fuse block is added in the VFAT3 to assign a unique Chip-ID to every production hybrid. This chip-ID is essential for the hybrid identification and auto loading of calibration data during CMS GEM operation. The readback of chip-ID in the GEM system showed rare bit-flips. This bit-flip is highly undesirable since it hinders the proper parameter loading to the targeted hybrids. Initial investigations reveal that possible reasons for bit-flips were power supply rails variation in the GEM electronics board and single event effects (SEE). A study of 12 VFAT3 hybrids was conducted to observe the variation of the number of chip-ID bit-flips with the increase in device power supply, shown in Figure 6.13.

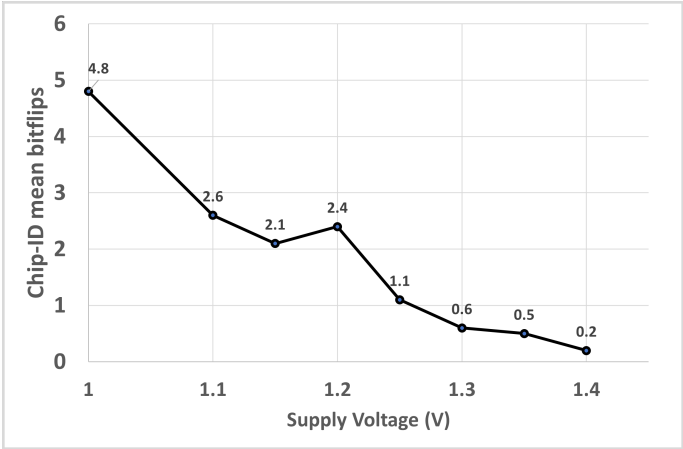


Figure 6.13: VFAT3 ChipID Bit-flips vs. chip power supply

The initial VFAT3 powering scheme of GE1/1 was not optimized, and powering DC/DC converters were targeted for 1.2V with no load conditions. The power measurements revealed that power rails dropped down to 1.15V for certain hybrids under full load conditions. It leads to an increase in the bit-flip probability as well as deteriorated the VFAT3 front-end performance. The design specifications of VFAT3 architecture allow the power rails up to a maximum of 1.2 V + 10 %. It was decided to increase the VFAT3 power supply from 1.2 V to 1.3 V in the GE1/1 system. These recommendations were also adopted for GE2/1 and ME0 GEM systems.

A total of 17000 VFAT3 hybrids are needed to cover complete muon endcaps with GE1/1, GE2/1, and ME0 of detectors. A total of 16-bits of e-fuses are thus required to store all the Chip-ID numbers, leaving only 16-bits to implement a suitable encoding scheme. Several encoding algorithms were analyzed to find an optimum lightweight encoding to correct the maximum possible number of random bit-flips within the 32-bit codeword budget. The basic process of bit-flips and the Chip-ID encoding is shown in the block diagram in Figure 6.14.

A thorough search for a suitable encoding scheme was conducted, and four different schemes, which could best solve the issue of random bit-flips in the VFAT3 chip-ID reading, were implemented in detail. Their pros and cons are listed in table 6.3. A combination of four 7-bit Hamming codes was evaluated first. A 7-bit Hamming code can correct 1-bit out of 7-bit. It means a total of 4-bits could be corrected with the concatenation of 4-simple hamming codes. Even

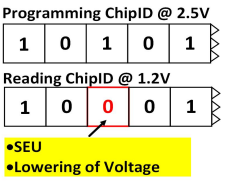


Figure 6.14: Process of Bit-flips.

Coding scheme	Error Correction capability for 32 bit word				Codeword size (bits)	Detailed correction capability
	1-bit	2-bit	3-bit	4-bit		
4-Hamming codes	Full	Partial			28	1/7 +1/7+1/7+1/7
1-Hamming +1-Golay	Full	Partial			30	3/23 + 1/7
Reed-Muller RM(2,5)	**Full**			**Detect only**	**32**	**3/32 correction, 4/32 detection**
Reed-Solomon Code 4 bits/symbol; m = 11, p = 4	Can correct 2 symbol i.e; minimum 2- bits , maximum 8-bits				32	2/32 minimum, 8/32 maximum

Table 6.3: Different multi-bit error correction encoding schemes considered for the Chip-ID encoding.

though Hamming codes provided 4-bit error correction capability for the whole 32-bit codeword, yet keeping in mind the full random nature of bit flipping in chip-ID, Hamming performed poorly in our case. If we consider the case where 2-bits were flipped in a single byte of the codeword, Hamming will not correct such cases.

The limitations of Hamming codes lead us to search for some more complex encoding schemes like Golay codes. A combination of hamming and Golay-code was evaluated to correct the random nature of bit-flipping in the data. The Golay code proved to be effective in correcting 3-random errors out of a total of 23-bits. The main issue with this Golay code was its limitation to correct only 12-bits of information message length. This limitation was compensated with a combination of hamming code and Golay-code. However, the last byte of the codeword became a bottleneck, and if there are multi-bit errors in the last byte of the codeword, it could not be corrected by Hamming code in that region.

After the poor performance of Hamming and Golay codes in Chip-ID multi-bit error correction, we experimented with modern block codes named Reed-Solomon codes (RS). These are block codes and require relatively large blocks of data streams to effectively correct multi-bit errors in the data. RS-codes work on symbols, and for the VFAT3 chip-ID, only 32-bit space was available to implement the algorithm.

If m represents the number of bits per symbol, n is the total number of symbols in codeword, and $2t$ defines the size of the check codes (parity symbols). Then the following equations exist for the RS-encoding:

$$n = 2^m - 1$$
$$2t = n - k$$
$$d_{min} = 2t + 1$$

Using $m = 4\ bits/symbol$, we have a total of $n = 15$ symbols for the final codeword. Taking $k = 11$ symbols for message information (including 4 chip-ID symbols padded with 7 zero symbols), results in $2t = 4$. It shows that $t = 2$ is the number of symbols that RS-coding can correct. Thus, depending on the location of bit-flips in the corrupted codeword, RS-encoding can correct 2 to 8-bits. RS-encoding was a good choice compared to the previous two methods providing at least 2-bit correction as a worst-case scenario.

We then tried Reed-Muller (RM) coding algorithm, which performed exceptionally well, corrected three random bit errors, and detected 4^{th} bit error. A simplified block diagram of Reed-Muller encoding and decoding is shown in Figure 6.15.

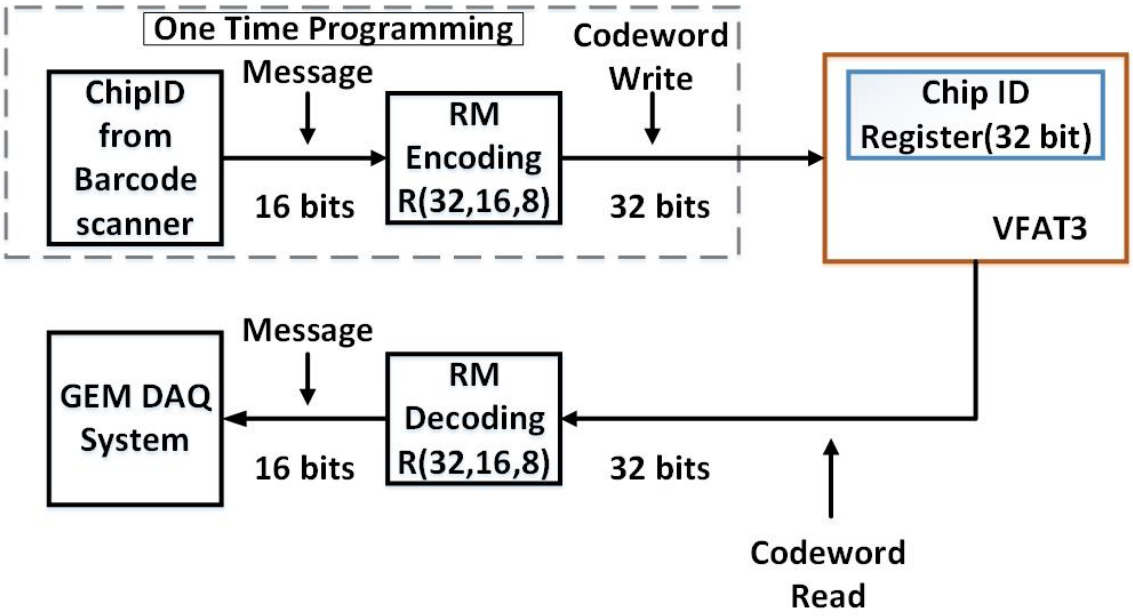


Figure 6.15: Chip-ID encoding Block Diagram.

6.5.1 Construction of Reed-Muller code

Reed-Muller (RM) codes are binary codes in which messages and codewords are transmitted as binary strings [103]. RM codes are based on a greedy approach. These codes are linear block codes having a length in powers of two. To generate a basis vector for RM codes, we can start by picking the all-0 block code. If we need to pick a second codeword with maximum distance, then a codeword with all-1 would be the best choice. If we continue with this approach of collecting codewords by maximizing the distance and keeping the previous codes, then the next codeword would be a half-0 and half-1 vector. In this way, we can build a simplex code space sequentially by reducing the basis vector code distance. We reach saturation with alternating 1-0 pattern codewords if we continue like this. Then we iterate the simplex construction approach on any previously picked vectors and keep on iterating this at each saturation, thus reducing the Hamming distance by half. This iterative approach provides a simple RM-code, whose basis is equally well defined by the monomials of bounded degrees.

6.5.2 RM encoding

Let us assume we want to encode a message m of length k using $\mathcal{RM}(r, m)$. The message length k is related to parameters r and m as:

$$k = \sum_{i=0}^{r} \binom{m}{i} \tag{6.3}$$

Then the encoded message c can be obtained by the following matrix multiplication:

$$c = m \times G_{\mathcal{RM}(r,m)} \tag{6.4}$$

Where the codeword c has the length $n = 2^m$ with a distance of 2^{m-r} between each codeword. Hence, it can correct the errors of $(2^{m-r-1} - 1)$ bits. The term $G_{\mathcal{RM}(r,m)}$ is a generator matrix for codeword c having dimensions of $(k * n)$. The rows of $G_{\mathcal{RM}(r,m)}$ form a basis for the elements of "c." The generator matrix is defined as follows:

$$G_{\mathcal{RM}(r,m)} = \begin{bmatrix} \psi(1) \\ \psi(x_0) \\ \psi(x_1) \\ . \\ . \\ . \\ \psi(x_{m-1}) \\ \psi(x_0 x_1) \\ \psi(x_0 x_2) \\ . \\ . \\ . \\ \psi(x_{m-2} x_{m-1}) \\ \psi(x_0 x_1 x_2) \\ . \\ . \\ . \\ \psi(x_{m-r} x_{m-r+1} \ldots x_{m-1}) \end{bmatrix} \tag{6.5}$$

where the mapping $\psi : \mathcal{R}_m \rightarrow \mathcal{F}_2^{2m}$ is defined as follows:

$$
\begin{aligned}
\psi(0) &= \underbrace{00...0}_{2^m} \\
\psi(1) &= \underbrace{11...1}_{2^m} \\
\psi(x_0) &= \underbrace{11...1}_{2^{m-1}}\underbrace{00...0}_{2^{m-1}} \\
\psi(x_1) &= \underbrace{11...1}_{2^{m-2}}\underbrace{00...0}_{2^{m-2}}\underbrace{11...1}_{2^{m-2}}\underbrace{00...0}_{2^{m-2}} \\
\psi(x_2) &= \underbrace{11...1}_{2^{m-3}}\underbrace{00...0}_{2^{m-3}}\underbrace{11...1}_{2^{m-3}}\underbrace{00...0}_{2^{m-3}}\underbrace{11...1}_{2^{m-3}}\underbrace{00...0}_{2^{m-3}}\underbrace{11...1}_{2^{m-3}}\underbrace{00...0}_{2^{m-3}} \\
&\vdots \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \vdots \\
\psi(x_i) &= \underbrace{11...1}_{2^{m-i}}\underbrace{00...0}_{2^{m-i}} \ldots \\
&\vdots \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \vdots
\end{aligned}
$$

During the HL-LHC run of the experiment, all three different GEM detector stations, namely GE1/1, GE2/1, and ME0, would be operational with $\sim$ 17000 VFAT3 operating in the system. So we need at least 16 bits for message ID numbers "m." Maximizing the RM-code error correction capability, we chose $r = 2$, and $m = 5$ to provide 3-bits of error correction by having a codeword of 2^{m} = 32-bits. The generator matrix for $\mathcal{RM}(2, 5)$ can be written as:

$$
G_{\mathcal{RM}(2,5)} = \begin{bmatrix} \psi(1) \\ \psi(x_0) \\ \psi(x_1) \\ \psi(x_2) \\ \psi(x_3) \\ \psi(x_4) \\ \psi(x_0x_1) \\ \psi(x_0x_2) \\ \psi(x_0x_3) \\ \psi(x_0x_4) \\ \psi(x_1x_2) \\ \psi(x_1x_3) \\ \psi(x_1x_4) \\ \psi(x_2x_3) \\ \psi(x_2x_4) \\ \psi(x_3x_4) \end{bmatrix} = \begin{bmatrix}
1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1 \\
1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&1&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&1&1&1&1&1&1&1&0&0&0&0&0&0&0&0&1&1&1&1&1&1&1&1&0&0&0&0&0&0&0&0 \\
1&1&1&1&0&0&0&0&1&1&1&1&0&0&0&0&1&1&1&1&0&0&0&0&1&1&1&1&0&0&0&0 \\
1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0 \\
1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0 \\
1&1&1&1&1&1&1&1&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&1&1&1&0&0&0&0&1&1&1&1&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&1&0&0&1&1&0&0&1&1&0&0&1&1&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&0&1&0&1&0&1&0&1&0&1&0&1&0&1&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&1&1&1&0&0&0&0&0&0&0&0&0&0&0&0&1&1&1&1&0&0&0&0&0&0&0&0&0&0&0&0 \\
1&1&0&0&1&1&0&0&0&0&0&0&0&0&0&0&1&1&0&0&1&1&0&0&0&0&0&0&0&0&0&0 \\
1&0&1&0&1&0&1&0&0&0&0&0&0&0&0&0&1&0&1&0&1&0&1&0&0&0&0&0&0&0&0&0 \\
1&1&0&0&0&0&0&0&1&1&0&0&0&0&0&0&1&1&0&0&0&0&0&0&1&1&0&0&0&0&0&0 \\
1&0&1&0&0&0&0&0&1&0&1&0&0&0&0&0&1&0&1&0&0&0&0&0&1&0&1&0&0&0&0&0 \\
1&0&0&0&1&0&0&0&1&0&0&0&1&0&0&0&1&0&0&0&1&0&0&0&1&0&0&0&1&0&0&0
\end{bmatrix} \tag{6.6}
$$

The implementation of RM-encoding proved to be straightforward, and codewords were programmed in all the production chips. A barcode scanner is used to read the hybrid number, and then a 32-bit codeword is generated by multiplying it with the $G_{\mathcal{RM}(2,5)}$ generator matrix. Afterward, this codeword is programmed in the 32-bit e-fuse with a particular programming sequence required by VFAT3 e-fuse programming, which also requires raising the power supply to 2.50 V.

6.5.3 RM decoding

The decoding algorithms are the more complex topics in coding theory. RM-codes have several decoding algorithms, and we used a majority logic decoding method. This decoding algorithm uses the majority vote to determine if a particular row of the generator matrix was employed to generate the corresponding codeword bit or not. During the device operation in the experiment, we read the 32-bit codeword, which was programmed during production testing. This codeword is then passed to an RM-decoder function, correcting up to 3-random bit errors in the codeword and generating the original 16-bit message (chip-ID). This correction proved extremely useful to correctly read the programmed chip-ID, making it possible to automatically load the device configuration at the system startup or reset.

6.6 Summary

The integration and the operation of the VFAT3 with GE1/1 triple-GEM detector were evaluated before starting the complete VFAT3 hybrid production phase. The VFAT3 hybrid is made robust against GEM HV discharges. Three different versions of the VFAT3 hybrid were designed and tested against GEM discharges in the laboratory and with real GEM detector. Combining the hybrid with a series resistor of 470 Ω (HV3b_v3) and 100 $k\Omega$ GEM filter resistor is chosen as a final GE1/1 configuration. This configuration achieved a damage probability as low as 3 % compared to several other schemes, with negligible efficiency loss. The GE1/1 noise performance and efficiency with HV3b_v3 hybrids were also evaluated. A noise floor of 0.4 fC is achieved with 98 % efficiency detectors. A Reed-Muller encoding scheme was also implemented in the VFAT3 chip-ID to mitigate bit-flips during GEM operation. The results from the Chip_ID read are promising, and no single event of misread is reported to date. Lastly, this study resulted in a redesign of the powering schemes of the GE2/1 & ME0 GEBs (see chapter 8).

Chapter 7

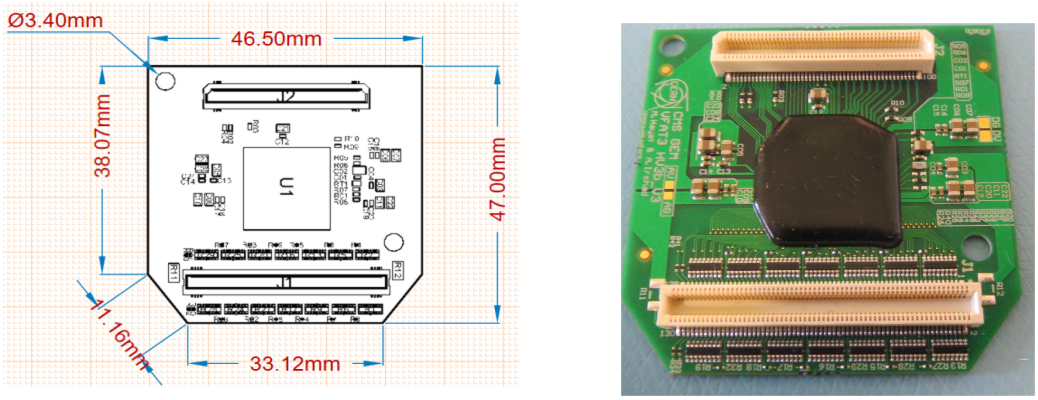
VFAT3 hybrid production and quality control

7.1 Introduction

GE1/1 GEM installation requires 144 Triple GEM detectors for both muon endcaps, each requiring 24 VFAT3 hybrids. A total of 3456 VFAT3 hybrids were required to instrument these GEM detectors. Mass production of 5000 hybrids, including spares, was launched to accomplish this task. The complexity of the VFAT3 hybrid imposed several design and manufacturing challenges to achieve a robust production-worthy hybrid. This chapter discusses the challenges faced to produce such a robust hybrid. The proposed solutions and their implementations have been discussed in detail. An automated Quality Control procedure and fast test setup equivalent to the level of what industry would provide was realized [104]. Finally, the detailed statistics of hybrid mass production are discussed, and major modes of hybrid failure are described.

7.2 GE1/1 VFAT3 hybrid Design

The GE1/1 hybrid is a small 46.5 × 47 mm multi-layer PCB designed to host the VFAT3 die directly. Figure 7.1 shows an assembled VFAT3 hybrid.



(a) VFAT3 hybrid dimensions (b) VFAT3 HV3B_V3 PCB

Figure 7.1: VFAT3 ASIC mounted on production hybrid for GE1/1 GEM detector. The ASIC is encapsulated in resin glob-top to protect it from external environment.

The key specifications are provided in table 7.1. Given the very high number of VFAT3 pins ($\sim$ 520), it imposes tight constraints on the size and the disposition of the wire bonding landing pads, which should have at most a width and pitch of 60 µm. Due to the small available space and hundreds of routing tracks, High-Density Interconnect (HDI) blind/buried laser vias were used. Miniature series resistor arrays of 0402 dimensions are added at the input channels.

Dimensions	46.5 cm $\times$ 46.5 cm
Layers	4
Minimum clearance	60 µm
Minimum Track Width	50 µm
Through-hole Pad to Track Clearance	120 µm
Via types	Through-hole, blind and burried
Minimum Hole size & diameter	125 µm and 280 µm
Material Type	FR-4 (Halogen free)
Board Thickness	1 mm ($\pm$200 µm)
Plating Finish	ENIG
IPC Class	IPC-A-600 Class II

Table 7.1: VFAT3 hybrid Design specifications.

Two AXK-5S series of Panasonic connectors were used, having a maximum composite insertion force of 0.785N per contact. This considerable insertion pressure imposed a minimum thickness requirement on the design and manufacturing of hybrid PCB to avoid bow and bending effects during PCB removal. A thick center core of 700 µm was used in the stack-up to achieve the desired 1 mm PCB thickness. The mass-scale hybrid fabrication struggled with over-etching and shortening of fine-pitch copper tracks during the gold plating process. A controlled routing strategy was used to distribute uniform copper density over the entire PCB area. The increase in the inner layer clearance from 60 to 75 µm and sparse landing pad size enlargement also helped to achieve the desired manufacturing yield. The critical design parameters of the VFAT3 hybrid are also listed in Table 7.1.

7.3 GE1/1 VFAT3 hybrid production

7.3.1 Hybrid quality concerns

Several design requirements posed challenges to the quality of the hybrid. Firstly, the small 60 µm landing pads and track clearance imposed the minimum possible manufacturing starting copper thickness of 5 µm. Secondly, the mounting of two rigid Panasonic connectors required a more rigid and thick PCB. Due to the use of the Panasonic connectors, the insertion force was significantly high. The Panasonic connectors use was unavoidable, as detector assemblies had already been fabricated with a counterpart connector. These conflicting constraints led to the choice of an optimum PCB thickness of 1 mm along with the use of High-Density Interconnect (HDI) blind and buried vias. As a comparison, a usual HDI PCB is manufacturable with a maximum of 400 µm thickness while GE1/1 hybrid is 1 mm thick.

7.3.2 Hybrid manufacturing issues

The central region of the hybrid PCB, dedicated for die placement and wire-bonding, is named as Pristine area. This area posed worst-case challenges during manufacturing, such as frequent over-etching, track bridging and flatness issues, and unwanted nodules

on the landing pads. Figure 7.2 shows a pristine area of the VFAT3 hybrid. During the

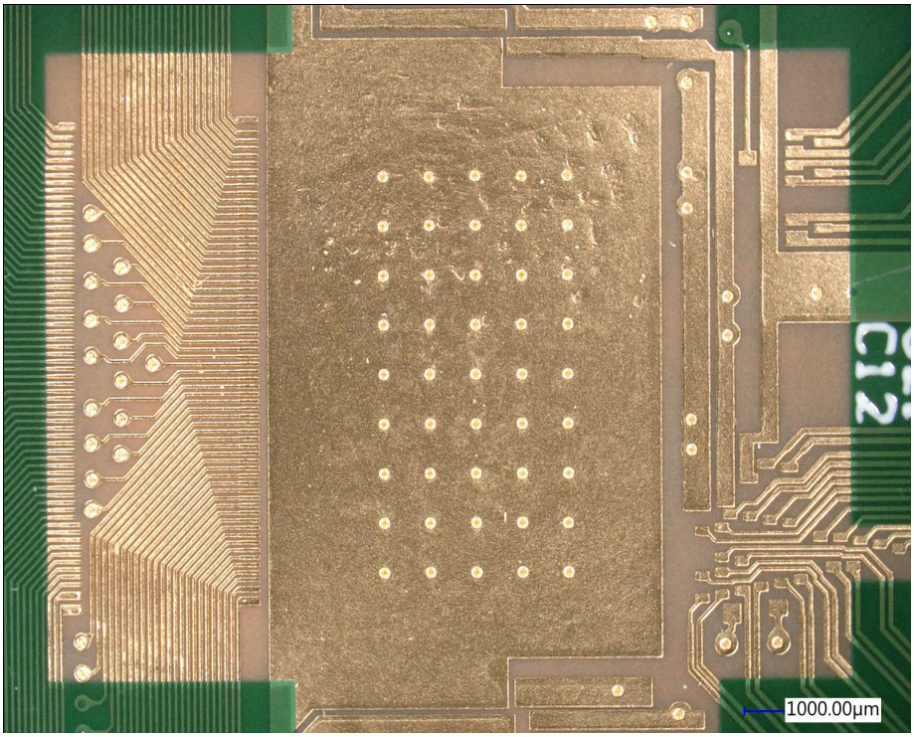


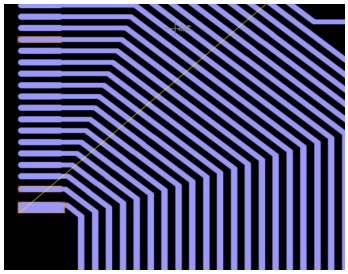
Figure 7.2: Prestine area of VFAT3 hybrid. Most of the production and bonding issues were found in this area. The minimum track clearance is 60 µm

prototyping phase of the hybrid, very few leading PCB manufacturers could produce this board in smaller quantities with a low yield of around 15 - 20 %, ultimately increasing the production cost. Nevertheless, this yield was not sufficient enough for any company to produce hybrid in mass volumes. Several essential adjustments were made in the production-ready PCB design in close collaboration with the manufacturer to avoid over-etching and shortening of fine-pitch copper tracks during the gold plating manufacturing process. A careful, controlled routing strategy distributes the uniform copper density over the entire PCB area to minimize the over-etching. The increase in the inner layer clearance from 60 to 75 µm and use of sparse landing pads enlargement also helped to achieve the desired manufacturing yield.

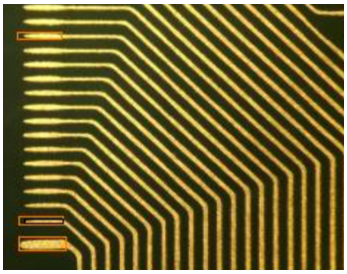
Figure 7.3 shows a comparison of the quality of pristine area for two vendors, "A" and "B." The minimum acceptable bond pad thickness is 60 µm, which can be bonded during the mass scale bonding of hybrids. The bond pads produced by manufacturer "A" were suffering from over-etching, and a shape deformation was also observed, as shown in Figure 7.3b.

In contrast, a reasonably good quality landing pad thickness was achieved by the manufacturer "B." These are achieved after several discussions with the manufacturer by reducing the final track copper thickness. The idea was to start with a fine thickness of 5 µm and gradually achieve the desired thickness of 22 µm by applying several layers of metal plating electroless nickel immersion gold (ENIG) process. The target track thickness parameter also plays a significant role in achieving a uniform differential impedance of 100 Ω for the digital tracks of the layout. Furthermore, several other manufacturing issues were also observed, such as the creation of Nodules and pad catering, as shown in Figure 7.4.

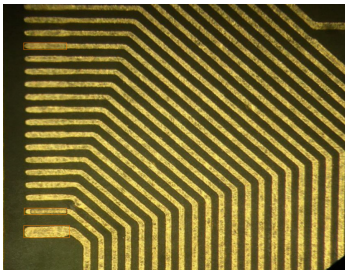
The plating defects can result in nodules that increase local stress concentrations and lead to crack formation upon exposure to excessive temperatures. Pad cratering is the



(a) VFAT3 HV3b_v3 production hybrid Gerber sketch of prestine area.

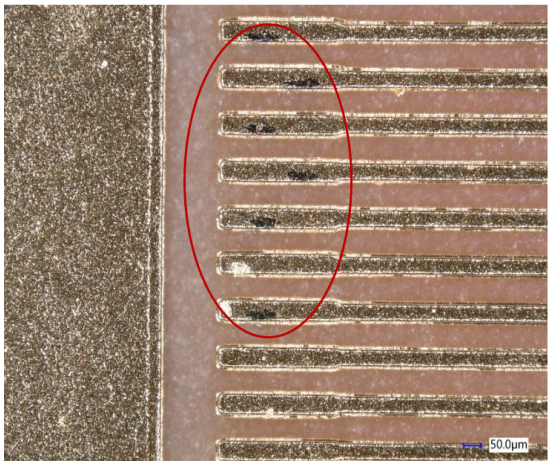


(b) VFAT3 HV3b_v3 production hybrid: Manufacturer A (Poor quality landing pads with over etching observed in prestine area)

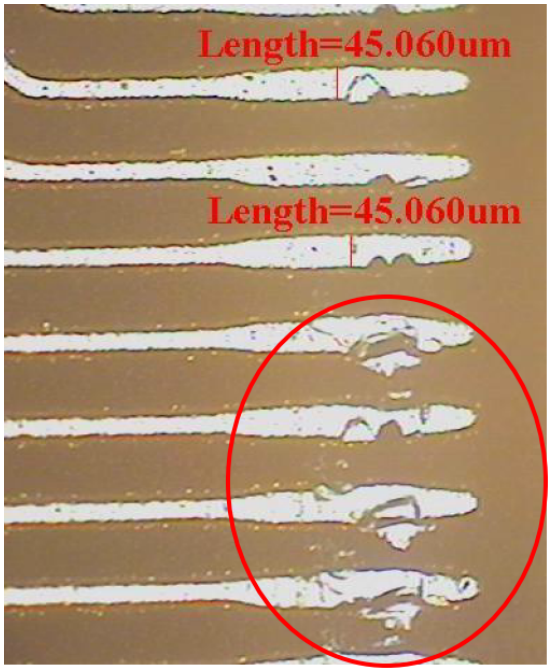


(c) VFAT3 HV3b_v3 production hybrid: Manufacturer B (slected). Very small over etching in prestine area, within acceptable limits

Figure 7.3: VFAT3 production hybrid pristine area comparison from two different manufacturers. A Gerber file sketch is on the left (a). The over-etching produced by manufacturer A is shown in (b) Acceptable landing pads by manufacturer B.



(a) Nodules and some material resins on landing pads



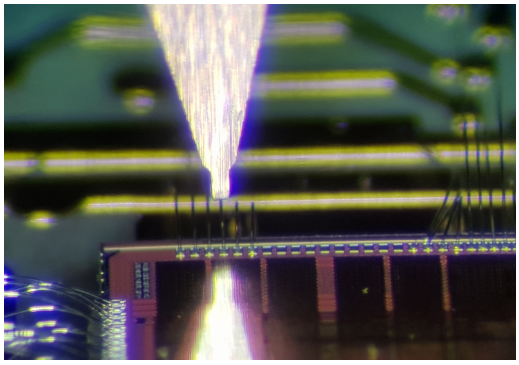
(b) Pad cratering issue

Figure 7.4: Creation of Nodules and pad catering observed with several manufacturers during pilot runs of the hybrid production.

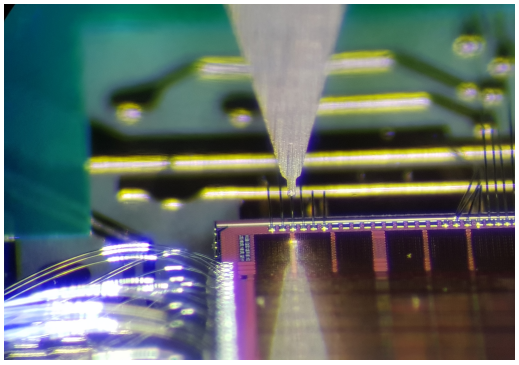
separation of the pads from the resin. In recent years, pad catering has become more dominant as the industry shifted to lead-free soldering; both nodules and pad cratering impact the production yield and long-term reliability.

7.3.3 Wire-bonding issues

The mass-scale wire bonding process also suffered with hybrid shorts and severely affected the initial yield. The rule of thumb for the choice of bond wire diameter states that the pad size width should be greater than 1.2× (chosen wire diameter). VFAT3 bond pads dimensions are 50 × 66 µm, and 25 µm wire is used during the prototyping phase, as shown in Figure 7.5a.



(a) Wire-bonding with 25 µm wire showing tooltip scratches with neighboring bonds and produces unreliability and shorts on die pads.



(b) Wire-bonding with 18 µm wire enhanced bond strength and avoids shorts

Figure 7.5: Wire-bonding thickness reduction to improve VFAT3 hybrid assembly yield. A special miniature tool was designed to avoid scratching of inner layer of channel side bonds [105].

Although bond wire diameter was correctly chosen, yet during pre-production runs, frequent bonding failures occurred, reducing the yield down to 60 %. Microscopic analysis of die pad dimensions revealed a relatively large variation in the pad dimensions, and some pads measured with 30 × 45 µm. This 30 µm pad width was insufficient to tolerate bond-wire expansion, and it contributed in shorts with neighboring pads and scratching of nearby bond wires by the bonding tool. The reduction of bond wire diameter to 18 µm, shown in Figure 7.5b, helped to achieve the optimum yield and added reliability in the process. The production yield was maintained around 90 % by choice of 18 µm bond wire.

It is also important to mention that Aluminium wedge bonding for VFAT3 was close to the tolerance limits of the machines used by the company, and a custom bonding tool was designed to allow the wiring of the second row of VFAT3 channel bonds without damaging the first [105].

7.4 VFAT3 Hybrid Production Test System

To perform the production QC of the 5000 VFAT3 hybrids needed for GE1/1, we developed a performant, fast, and highly automatized test stand worthy of an industrial QC stand. The designed QC stand is shown in Figure 7.6

It was developed around a Kintex-7 evaluation board and the custom "Verification Board" presented in chapter 4. The firmware was based on a System-on-Chip (SoC) architecture with a Microblaze processor connected to the Verilog HDL peripherals within the FPGA through Advanced Extensible Interface (AXI) bus architecture as shown in figure 7.7.

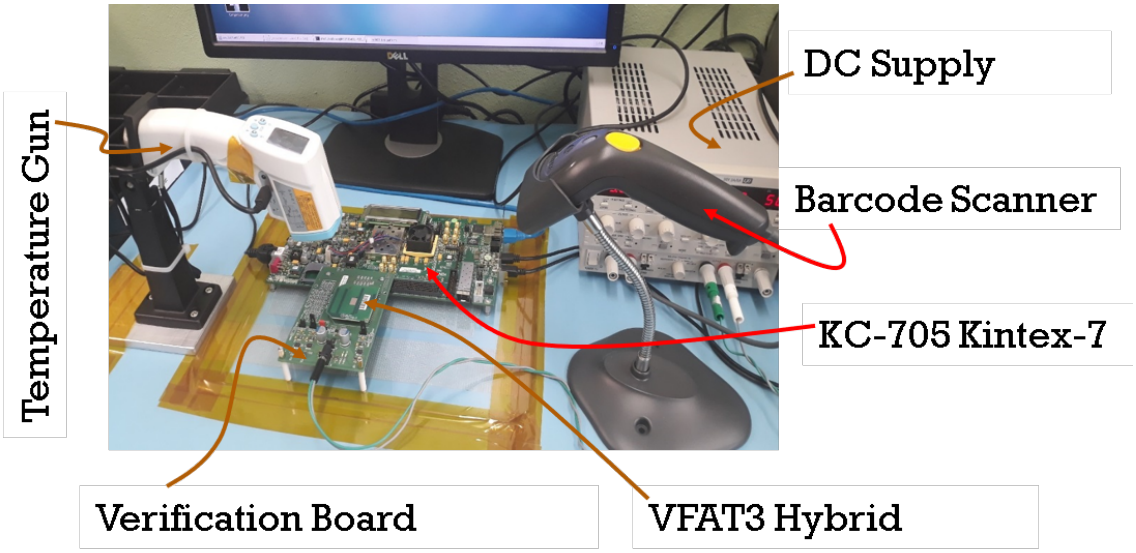


Figure 7.6: VFAT3 QC test bench

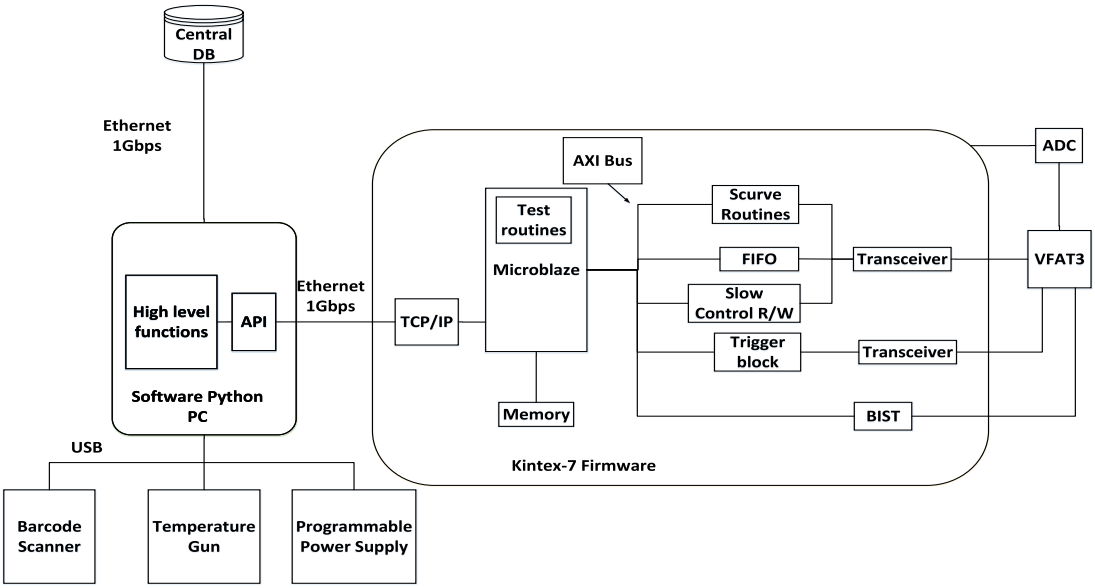


Figure 7.7: VFAT3 hybrid Production test system flow diagram

This firmware is a major upgrade of the functional characterization IP-bus-based firmware discussed in [74]. Several test functions have been discussed in detail in [79] during the characterization of VFAT2. Most of these test functions have similar algorithms between both test systems, such as S-curve and DAC scans.
VFAT3 also has a built-in temperature sensor that would be used to acquire a full GEM system temperature map during CMS operational runs. The offset correction of each sensor is required to compensate for response variation in these sensors. An infrared temperature gun is used to measure the temperature of each hybrid during production. This production test system is a highly optimized and extended version of the VFAT3 functional test system depicted in chapter 4. The more time-consuming routines were migrated to firmware to achieve production scale throughput from the test system. The characterization system performed the complete typical device characterization in around thirty minutes. Using pipelined hardware blocks written in Verilog, with cycle-accurate timing,

helped reduce the test time to around 2 minutes.

7.5 VFAT3 hybrid production test flow

The VFAT3 hybrid production test system design was based on a user-friendly traffic light system approach. The user inserts the hybrid to the designated test port and presses a start button. The system displays the test results in either red, green, or yellow and takes care of the necessary hybrid powering. The user must read the label code displayed on the computer screen and attach the corresponding color sticker on the hybrid, and place it in a respected color basket. The red code indicates that the hybrid cannot be used in the experiment or any other R&D test stand. The typical problems associated with the red hybrids are power short and communication issues. The yellow label indicates that the hybrid still cannot be used in the experiment, but it could be used for R&D purposes in the test stands such as cosmic stands. A typical yellow hybrid involves broken DAC, ADC, or multiple dead channels. The yellow hybrids are used for R&D purposes only since communication with the VFAT3 device on these hybrids is possible. The green label indicates the good production hybrid with an optional number of 1, 2, or 3 bad channels. We accepted a maximum of 3 bad channels for one good hybrid. The reason for this trade-off was that if we reject all the hybrids with at least a single bad channel, then we end up with a shortage of hybrids and VFAT3 chips for the GE1/1 experiment. In GE1/1, the accepted theoretical inefficiency is 1 % per η partition, which translates to at most three dead channels on one hybrid per η partition. We evenly distributed the hybrids with bad channels over the entire GEM detectors area to maintain an efficiency loss of less than 1 percent.

Figure 7.8: Color coding used for production hybrids based on the test results.

The hybrid QC flow is shown in Figure 7.9. Before the start of electrical testing, the hybrid is visually inspected, and a barcode is attached to it. Then the two first tests series (columns 1 and 2 in Figure 7.9) look for global functionalities, which would immediately lead to a red flag if encountered. Then the QC procedure starts the VFAT3 calibrations. If the Calibration, Bias, and Monitoring (CBM) block is problematic, the hybrid is yellow. Afterward, the chip is biased, the DACs are scanned, and the settings are adjusted accordingly. Finally, internal test pulses of known amplitudes are injected into the VFAT3 input channels to characterize the noise level, identify possible dead channels. At the end of the QC procedure, the data and calibration coefficients are stored in the VFAT3 database. We will now discuss in detail the individual steps.

7.5.1 Hybrid visual inspection & barcode labeling

It was decided to affix the barcode labels on each production hybrid before the production test. The main reason for adopting this approach is to track and identify each hybrid regardless of its production status. A barcode scanner was used to read and register the

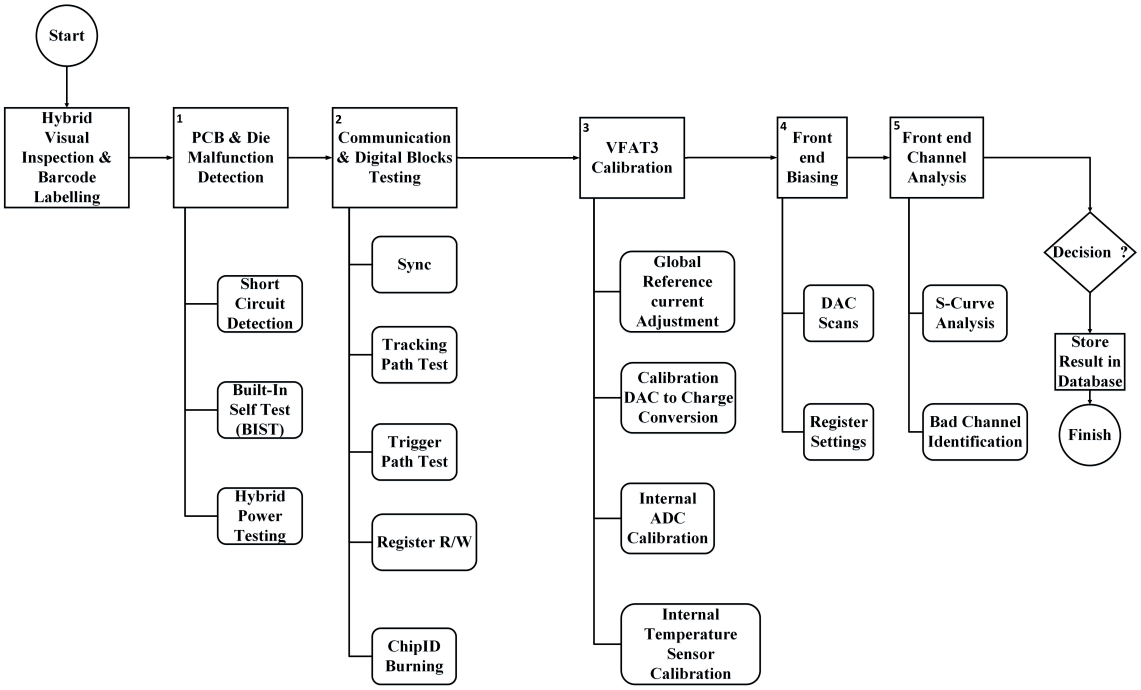


Figure 7.9: VFAT3 hybrid Production test flow diagram

chip-ID for each hybrid in the production software. This approach rules out the operator error and registering of the wrong chip-ID in the system. The chip-ID is converted into an encoded 32-bit Reed-Muller codeword capable of correcting three random bit errors during the read operation. The encoding algorithm is only implemented in test bench production software, while decoding is required afterward during a chip-ID read operation in the CMS GEM system.

7.5.2 VFAT3 BIST & power testing

VFAT3 has been produced in volumes for GEM production. Keeping in mind that it is the only ASIC for all three GEM stations GE1/1, GE2/1, and ME0, several built-in testability features were embedded in the device along with desired features that facilitate the production testing of the hybrid. A Built-In Self Test (BIST) is incorporated into the device to test the faulty memories. All the digital logic in the device is triplicated, and there is no option in the device to load the known pattern in the two SRAMs. Hence, BIST is the only reliable test that can be initiated externally through dedicated pins. This test monitors every memory sector and terminates the test if any issue in the pattern read-write program is detected. The clock cycles during the BIST test are counted and compared with reference cycles of 1080300-1080301. A smaller number represents the faulty memory block.

Figure 7.10 shows the returned value of the BIST test for 4742 GE1/1 hybrids.

Note the logarithmic scale on the Y-axis. Three clusters of different BIST cycles can be observed. The peak at 1080300 corresponds to the expected value. 4604 GE1/1 hybrids, that is 97 % of them, returned the exact value of 1080300. The two other peaks are due to misbehaving hybrids. The leftmost cluster of 39 hybrids is most likely due to SRAM1 issues. The second cluster counting 99 hybrids is attributed to issues within SRAM2.

The VFAT3 power domains were also monitored during the production testing of the hybrids. During production testing, two different stations were used to test the hybrids. Both the digital and analog power domains were measured while VFATs were configured

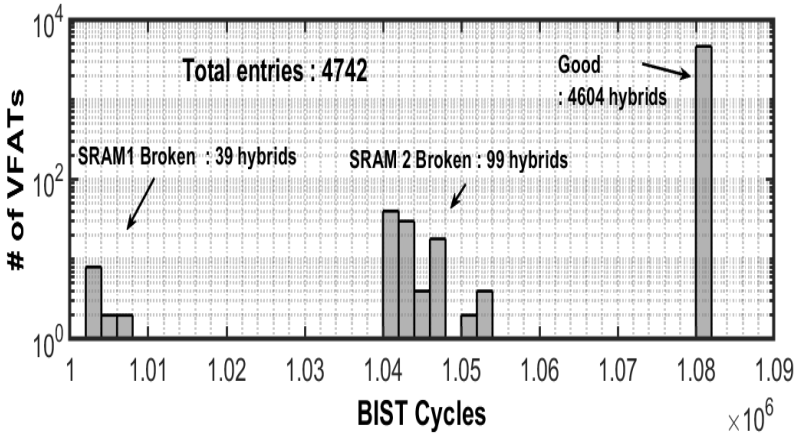
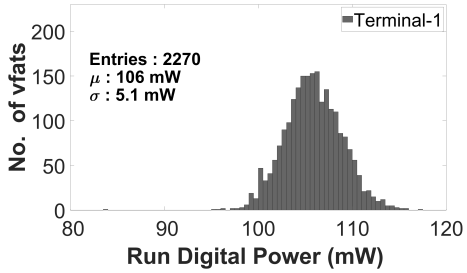
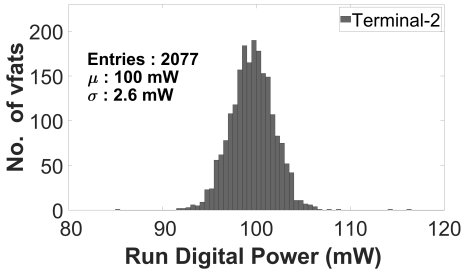


Figure 7.10: Built-in Self-test production analysis plot. The vertical axis shows a logarithmic scale.

in run mode. The run mode turns on all the internal functional blocks inside the chip. A run digital power ($VDD = 1.2\ V$) plot is shown in Figure 7.11, representing all the production hybrids tested on both of the stations.



(a) A histogram plot showing digital power domain of VFATs tested on Terminal-1



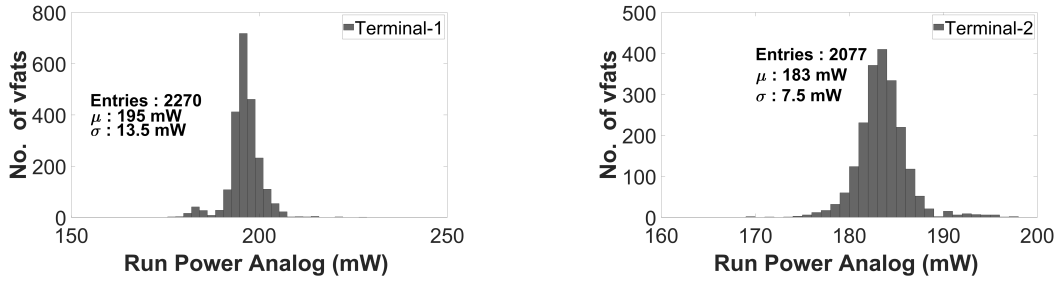
(b) Wire-bonding with 18 µm wire enhanced bond strength and avoids shorts

Figure 7.11: A histogram plot showing digital power domain of VFATs tested on Terminal-2

The Mean power of 106 mW and 100 mW are observed on both the terminals with a maximum deviation of 5 mW. We labeled the hybrid as yellow if power measured beyond mean $\pm 3\sigma$. A similar set of plots for the analog power in run mode is also shown in Figure 7.12.

The mean of 195 mW and 183 mW were observed from two stations with a maximum spread of 13 mW. A similar criterion of mean $\pm 3\sigma$ is also applied to filter the faulty hybrids with a wide analog power deviation. It can be seen that the spread of analog power is higher than digital power. One possible reason for this is related to many analog channels and the occurrence of adjacent channels shorts and un-bonded channels. The power nets short is not visible in these plots. Such hybrids are discarded at the first step, and no further production tests were performed for rejected hybrids.

A slight difference (< 10 mW) in mean power measured by both terminals was observed. This was caused by the current monitoring circuit calibration tolerance between the two systems. This was compensated by the adjustment of selection criteria for power domains for both stations.



(a) A histogram plot showing analog power domain (in mW) of VFATs tested on Terminal-1

(b) Wire-bonding with 18 µm wire enhanced bond strength and avoids shorts

Figure 7.12: A histogram plot showing analog power domain (in mW) of VFATs tested on Terminal-2

7.5.3 VFAT3 CBM production results

The functionality of CBM block is discussed in detail in 3 section 3.7. During production testing, the monitoring of key parameters of the CBM block was evaluated. It includes tuning of a bandgap reference voltage and global reference current, calibration of charge injection circuit and related DAC, and calibration of internal ADCs.

As described in section 3.7, at the core of the VFAT3 bias block, a bandgap circuit (see Figure 3.14) generates stable voltage and current references. However, due to a strong dependence on the underlying technology process, a device-to-device variation exhibits in the bandgap expected voltage. Figure 7.13 shows the bandgap voltage spread for all GE1/1 hybrids, measured with an external 16-bit ADC connected on the VFAT3 V_BGR pin. The mean value of the distribution is 340.4 mV with a standard deviation of 6.2 mV.

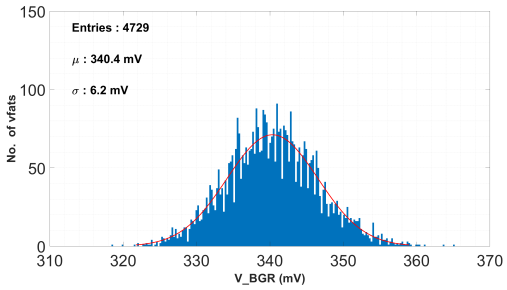


Figure 7.13: Band-gap reference voltage spread for production VFAT3 hybrids, monitored by an external 16-bit ADC on V_BGR pin

The bandgap voltage generates a stable Iref current of 5 µA, called a global reference current, which provides a reference to other current DACs. A 6-bit tuning DAC is provided to further fine-tune the Iref value for each VFAT3. A precise 20 kΩ external resistor is mounted to convert this current to 100 mV reference voltage. During the production testing, the reference voltage at the Imon device pin is monitored for each hybrid and adjusted precisely to 100 mV. This Imon adjustment is achieved by varying the Iref tuning DAC. A histogram showing a post-calibration plot for the Imon values of the production hybrids is shown in Figure 7.14.

It is essential to mention that the stored value of Iref is volatile, and the device loses its configuration if powered off or by an assertion of hard reset. Thus, it is necessary to reload the correct configuration each time before the start of device operation for actual

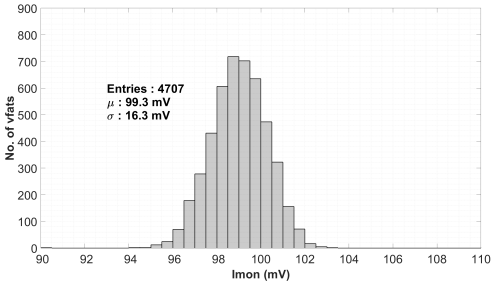
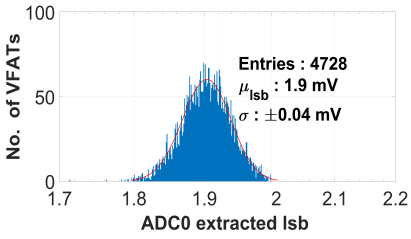


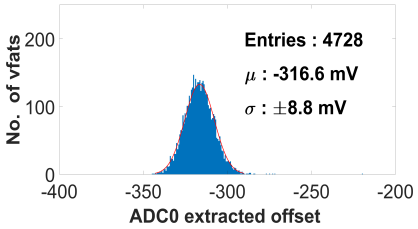
Figure 7.14: Corrected Imon values (mV) measured through external 16-bit ADC during production calibration

signal acquisition. Once the correct value of Iref is loaded, all the biasing DACs generate correct voltages and currents. It is not recommended to vary the Iref value during the device user operation. All the calibrations and adjustments will become invalid if the Iref value is changed.

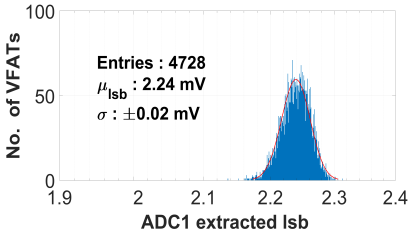
VFAT3 has two redundant monitoring ADCs, called ADC0 and ADC1, to facilitate in-situ calibration and configuration of the device during operation in the CMS environment (see Section 3.7.3). It is vital to characterize each ADC during production testing and extract the gain and offset coefficients from the linear fit of both the ADCs. These coefficients must be reloaded before using ADCs for other calibration and biasing of the device. A 16-bit external ADC is used to calibrate both ADCs, and linear fit the parameters. A linear ramp is provided through a DAC at the inputs of internal ADCs and external calibration ADC. A detailed ADC characterization procedure is explained in Section 4.5.3. The production data plots for both ADCs calibration coefficients are shown in Figure 7.15.



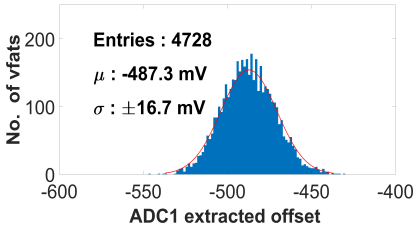
(a) LSB of ADC0 measured during the production of VFAT3 hybrids



(b) DC offset coefficient for ADC0 measured during the production of VFAT3 hybrids



(c) LSB of ADC1 measured during the production of VFAT3 hybrids

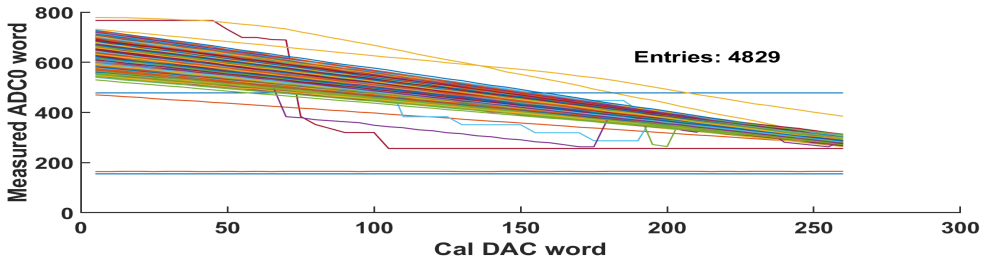


(d) DC offset coefficient for ADC1 measured during the production of VFAT3 hybrids

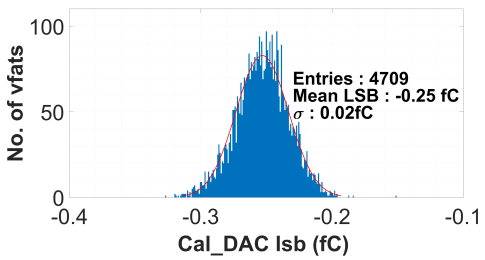
Figure 7.15: Gain and offset plots for ADC0 and ADC1 blocks for production hybrids.

ADC0 showed a mean LSB of 1.9 mV with a mean dc offset of -316.6 mV. The ADC1 showed a mean LSB of 2.2mV with an offset of -487 mV. The ADC0 block proved to be highly precise, and no discontinuities were observed while testing these sub-modules. A few converters showed out-of-range LSBs and offset coefficients, marked as yellow hybrids and isolated from the green hybrids.

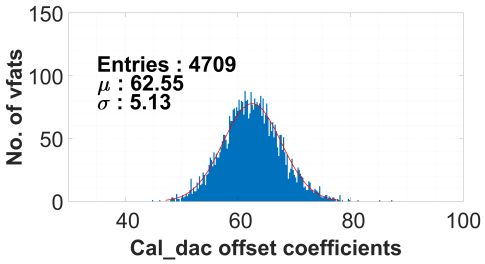
Once ADC0 and ADC1 are calibrated, we can use them to calibrate the DACs, like the CAL_DAC, an 8-bit DAC used for the injection of voltage and current pulses depending on the injection-mode configuration. The detailed procedure of DACs calibration is described in Section 4.6. The calibration of CAL_DAC showed that its response is highly linear, and first-order fitting is sufficient to get the reliable fitting. Figure 7.16 shows production plots for the calibration DAC for all the GE1/1 hybrids. CAL_DAC scan measured with ADC0 for all the hybrids is plotted in Figure 7.16a. A few non-linear DAC plots are visible, representing missing codes and broken DAC modules. Hybrids with such DAC responses were identified and tagged as yellow. The calibration of front-end channels for the hybrids exhibiting bad CAL_DAC modules is not possible.



(a) Calibration DAC production plots for VFAT3 hybrids, measured by ADC0



(b) Gain coefficients spread, extracted from production plots of cal_dac



(c) DC offset coefficients spread, extracted from production plots of cal_dac

Figure 7.16: Calibration DAC production plots for all the hybrids showing the precision of measurements and calibration accuracy of the DAC.

The linear fit parameters for the production hybrids are shown in Figures 7.16b and 7.16c. A mean charge step of $-0.25\,\mathrm{fC}$ is observed with a mean offset of 62 fC. This DAC is used to produce precise calibration pulses with increments of +0.25 fC during the front-end channel calibration procedure. This DAC produces negative charge pulses to emulate the GEM charge, usually a negative signal pulse.

7.5.4 Front-end biasing testing

The VFAT3 preamplifier is the most sensitive part of the front-end channel, and it is highly programmable. The gain and peaking time of the preamplifier can be programmed through slow control registers. Three current DACs and one voltage DAC control the functionality of the VFAT3 channel preamplifier. The linearity of these DACs is essential throughout the whole dynamic range. We scanned these DACs for linearity during the hybrid production. The hybrid was also categorized as yellow if any of the front-end DACs showed non-linearity or missing codes. A preamplifier Bias Input Transistor (Pre_I_BIT) current DAC adjusts the current at the input transistor in the preamplifier in the units of μA. The Pre_I_BIT linear plots for all the production hybrids are shown in Figure 7.17.

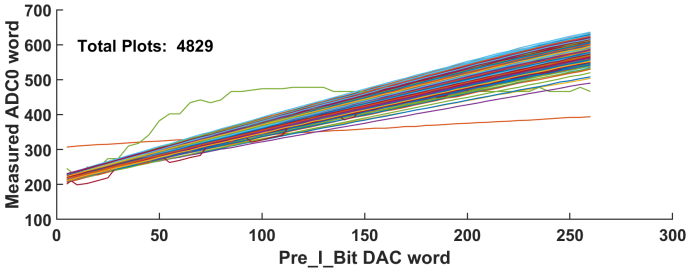


Figure 7.17: Front-end biasing DAC pre_I_BIT (8-bit DAC) plots for all VFAT3 GE1/1 Prouction, measured by internal ADC0

Most of the hybrids showed a highly linear behavior in the operating region, and only a very few devices showed broken DAC. The selection criteria were based on 3σ ranges of linear and goodness of fit parameters. The chi-square value was evaluated for each hybrid, and any value far from 1 was considered a failure. The problem of missing codes is evident in a few DACs showing a staircase effect and unresponsive behavior. A nominal current of 150 µA is required to properly bias the DAC, which corresponds to a default word of 150. A margin of 100 DAC words is available to precisely adjust the DAC to the targeted current.

The Preamplifier Bias Leakage Compensation Current (Pre_I_BLCC) DAC controls a susceptible node and adjusts the current in a few tens of the nA range. The plots in Figure 7.18 show scans for the production hybrids.

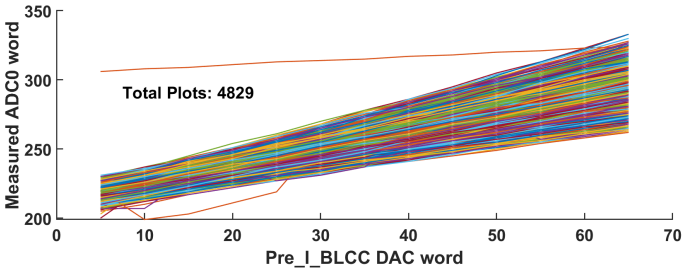


Figure 7.18: Front-end biasing DAC Pre_I_BLCC (6-bit DAC) plots for all VFAT3 GE1/1 Production lots, measured with internal ADC0.

Most of the hybrids showed linear Pre_I_BLCC DAC response when measured with internal ADC0 within the chip. A very few DACs showed missing codes and non-linearity, which were sorted out by fit parameters. The nominal desired current output by this DAC is 25 nA, which corresponds to a default word of 25. A wide margin is also

available to fine-tune the DAC to achieve the best results. The other front-end DACs also showed similar responses and were fitted with polynomials for precise biasing during the GEM operation. These front-end DACs must be tuned to specified current and voltage levels to properly amplify and process the input charge signal from GEM readout strips. To provide the calibration flexibility during GEM operation, we provided the raw lookup tables in the database to apply the desired polynomial fit function later on by the DAQ experts based on the desired biasing precision. We ensured the detection and isolation of problematic front-end DACs during the VFAT3 production and only passed the hybrids with good front-end biasing DACs.

The analog signal from each channel enters a constant fraction discriminator (CFD), where it is converted to a discrete pulse with precise timing information. Two 6-bit DACs control the biasing of the CFD. These DACs adjust the CFD bias in large process variations, which are not observed during production testing. The default word configuration is sufficient for the desired performance of the CFD. The production plots for all of the VFAT3 hybrids showing a full scan of CFD DAC1 are shown in Figure 7.19. The default

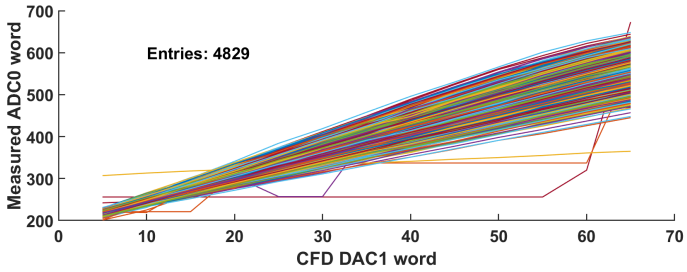


Figure 7.19: CFD biasing DAC1 plots for all production hybrids

word for CFD DAC1 is 40 (decimal), which is within the center of the DAC linear functional range. It shows that the slope difference between the DACs is minimal and only by adjusting slight offset all coincide responses. A nominal current of 20 µA is required for all the DACs to bias the discriminator with the same response. There is plenty of margin available around the default word of 40 to adjust the desired current bias with an LSB of 500 nA. Other important arming DACs plots are shown in Figure 7.20. The voltage generated by arming DAC is used as a threshold voltage for the discriminator.

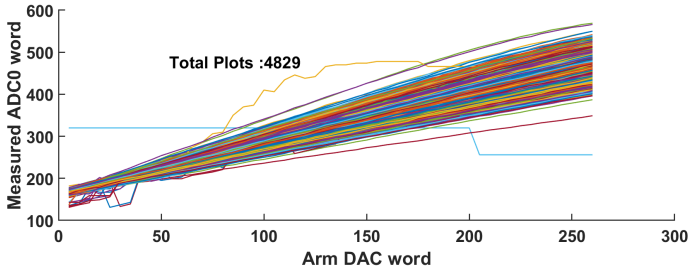


Figure 7.20: arming DAC production plots for all VFAT3 production hybrids

The nominal threshold settings in CMS GEMs at a medium gain and 45 *ns* shaping time is around 10 fC that corresponds to arming word of 70. This is mid-range, and a wide margin is available on both sides of the DAC-word of 70 to produce 10 fC for all the VFATs resulting in the same global threshold (in fC). It is also interesting to mention that most of the broken DACs found in the above plots belong to faulty hybrids declared during previous tests.

7.5.5 Bad channel Identification

The identification of bad channels is an important quality control test during the VFAT3 hybrid production phase. After the hybrid assembly and device mounting phase, we categorized the bad channels into four different types:

- **Dead channels:** The channels showing no–response to internal injected signals during the s-curve test
- **Un-bonded channels:** The channels with low ENC close to Cd =0
- **Noisy channels:** The channels showing very high ENC
- **Un-trimmable channels:** The channels showing Thresholds out of Trimming range

To distinguish between all the bad channels during production, we added two detector emulator cables with 40 pF capacitance per channel. As a reference, the GE1/1 detector strip capacitance is around 20 pF per strip. The idea behind adding the cable is to enhance the front-end noise and distinguish between noisy and un-bonded channels with absolute certainty. It can be seen in Figure 7.21 that the mean ENC for all the channels for a random nine different production hybrids without capacitance is 0.2 fC, while ENC increased to 1.9 fC by adding a capacitance of 40 pF at the input of each hybrid.

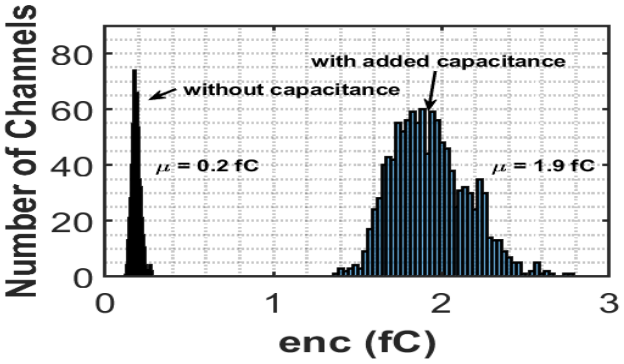
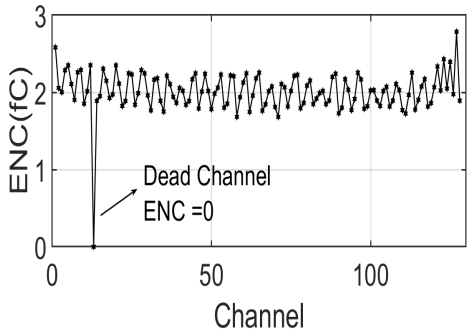


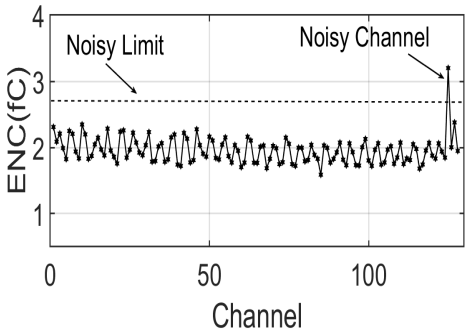
Figure 7.21: ENC comparison histograms for 9 different VFAT3 production hybrids with and without input capacitance.

Additional capacitance moved the mean of ENC for all the channels tenfold, distinguishing unbonded and dead channels more explicitly. Noisy channels also showed an apparent significant increase in ENC due to added capacitance at their inputs. This enhancement of noise is visible in the ENC plots of production hybrids, as shown in Figure 7.22.

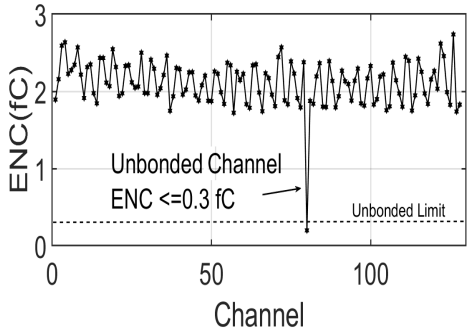
A dead channel is visible in Figure 7.22a with no response to the internal injection circuit. The detection of dead channels is quite straightforward and has no dependency on input capacitance. The second example of a noisy channel is shown in Figure 7.22b. A nominal noise limit is extracted for a channel to be good, based on the training of several hybrids testing with GE1/1 detector. Any channel crossing that threshold is marked as noisy. The noisy channel can be masked in the system. The third category is an unbonded channel shown in Figure 7.22c, which has a broken connection from the device pads to the interface connector. It could happen either due to missing wire bonding or bad soldering of a miniature series resistor array on the hybrid PCB. An unbonded channel has a small ENC as compared to connected channels. We have a wide noise span to classify the unbonded channels. The last kind of bad-channel is an un-trimmable channel, shown in Figure 7.22d. The front-end was configured in medium gain and shaping



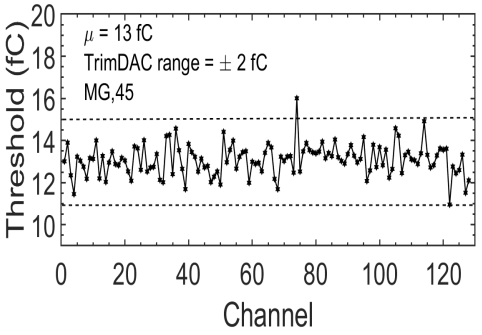
(a) VFAT3 with one Dead channel. A dead channel shows no response to input pulses. S-curve plot for dead channels always return ENC= 0.



(b) VFAT3 with a noisy channel. The noisy channel limit is obtained by training of several test hybrids with GE1/1 detector. Trimming is not useful to calmdown a noisy channel. Masking is the only solution to use a hybrid with noisy channel



(c) VFAT3 with one unbonded channel showing low noise. Unbonded channel does not see large cable capacitance, so produces lowest possible noise around 0.2fC. It is easy to distinguish unbonded channel by setting a threshold limit in the middle of the wide margin from 0.2fC to 2.2fC.



(d) VFAT3 with two untrimmable channels. Trimming ranges were precalculated befre production and any channel which gives its threshold out of that window is declared as untrimmable. A untrimmable channel responds to trimDAC adjustment but unable to be tuned within acceptable limits of 3 σ of threshold spread.

Figure 7.22: Bad channel detection plots with additional detector emulator cable of 40 pF capacitance. These plots indicate how the addition of cables made easier the distinguishing of different kinds of bad channels.

time of 45 ns during hybrid production testing, the same as will be used in GEMs. The maximum trimming span in this configuration is ± 2 fC. If the threshold of any channel exceeds the trimming limits, then we declare that channel as un-trimmable. We apply these un-trimmable criteria on both directions of the mean threshold. An un-trimmable channel might show more threshold or less than the mean value of the threshold for a particular VFAT.

The distribution of a different number of bad channels found during the production is also shown in Figure 7.23.

The Y-axis shows a logarithmic scale to enhance the small number of multiple dead channels. Mostly green hybrids were observed without any dead channels. The hybrids with one bad channel were second-highest in numbers, and we found around 100 green

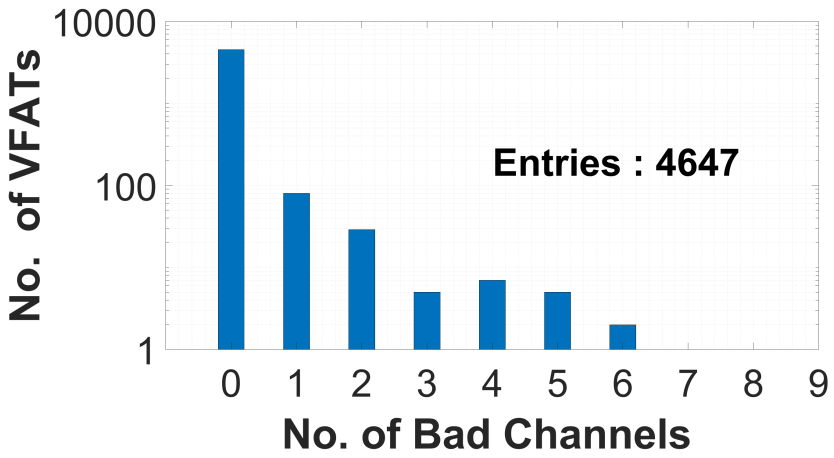


Figure 7.23: Distribution of bad channels in the production data showing number of VFAT hybrids with 0, 1,2....8 bad channels. Y-axis is labelled in logarithmic scale

hybrids with a 1-bad channel. The selection criteria for green hybrids are limited to 3 bad channels at the most per hybrid, and the hybrid is declared yellow if found four or more bad channels. The number of problematic hybrids with four or more bad channels is less than 0.5 % of the total production volume, which is a negligibly small number.

In the production plots of previous sections, we have seen that the total number of hybrids slightly varies from plot to plot. It is because a small number of hybrids were found with unknown issues which halted the test system during production testing. So data for some kind of tests were not available for a few hybrids, and we marked these hybrids as a yellow category. The test sequence is already shown in the block diagram of Figure 7.9. The S-curve and dead channel analysis come in the end; that is why the total number of hybrids was minimum in the dead channel analysis plot of Figure 7.23.

7.5.6 VFAT3 GE1/1 hybrid Production database

The CERN database service fully supports the VFAT3 database on demand (DBoD) service [106]. The main idea of the CERN DBoD project is to provide the CERN user community service to quickly develop and run database services supporting the CERN central Oracle-based service. This service enables the user to perform several tasks themselves, traditionally performed by database administrators, including running the database engines of their own choices such as PostgreSQL, Oracle, and MySQL.

The DBoD service allowed us to store and manage the VFAT3 database on CERN central DB servers. All the data tables for the hybrid tests are stored on the central servers, and multiple testing platforms access the database concurrently. A maximum of three test stations was used for the entire production of VFAT3 hybrids. The concept of central database storage is shown in Figure 7.24.

The central storage of production data ensures that no duplicated entries could exist on multiple PCs for the same hybrid if re-tested. Only the latest results will be available for the user while accessing the particular database entry. For example, suppose one particular hybrid is tested on multiple stations on different time instances. In that case, only the latest results will be stored in the central database as final data for that particular hybrid, overriding the earlier results. This feature is highly desirable to ensure database integrity and avoid multiple copies of hybrid configuration data. A large amount of data for each hybrid is stored in 21 tables with chip-ID as a Primary Key. The stored data

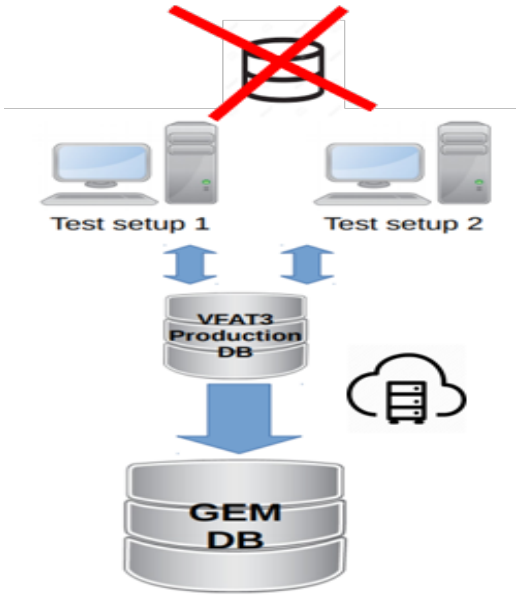


Figure 7.24: VFAT3 Production database central storage block diagram, managed by CERN DBoD service.

includes different test results, calibration data, scan data for internal DACs, and detailed front-end channel information. A simple view of VFAT3 database tables is shown in Figure 7.25.

Multiple online queries are possible to monitor different production parameters. A new table for channel categorization was also added during the bad channel selection criteria upgrade. A 4-bit word was used to store the information regarding the bad channel category in the database. The idea was to load the bad channel information from the database to mask these channels before data acquisition during CMS GEM operation.

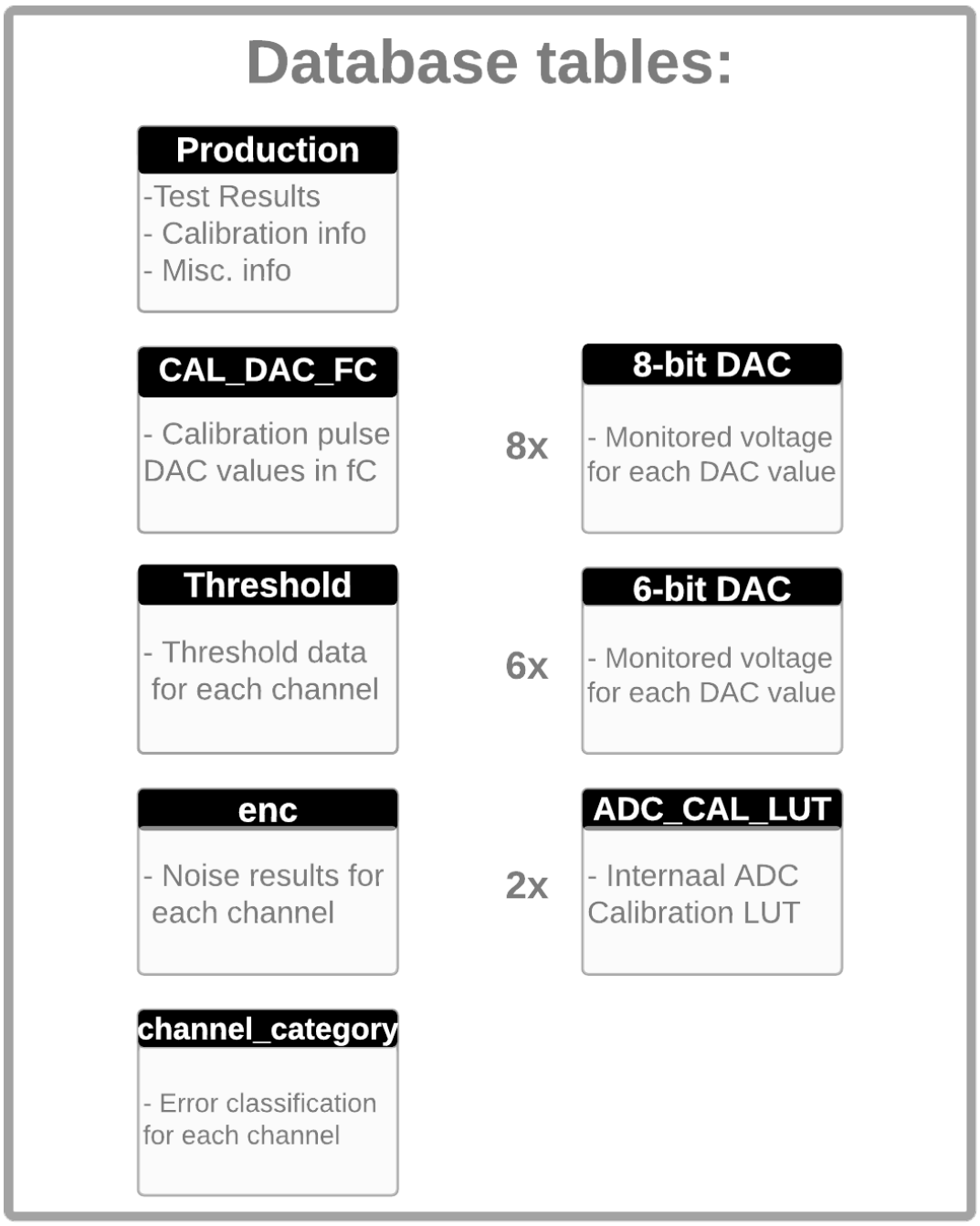


Figure 7.25: VFAT3 Production database tables for each hybrid, with Chip-ID as primary Key

7.6 Hybrid Production Statistics

The VFAT3 hybrid production is split into thirteen smaller batches to coincide with the PCB fabrication and wire bonding production rates. The wire bonding of the VFAT3 becomes a key parameter to define the overall hybrid robustness. Strict quality control was implemented to verify small batches of wire bonded hybrids to avoid significant production loss in case of minor bonding issues. So the distribution of production hybrids in small batches alleviated the additional pressure on bonding personnel. A cumulative

production profile for the VFAT3 hybrids is shown in Figure 7.26.

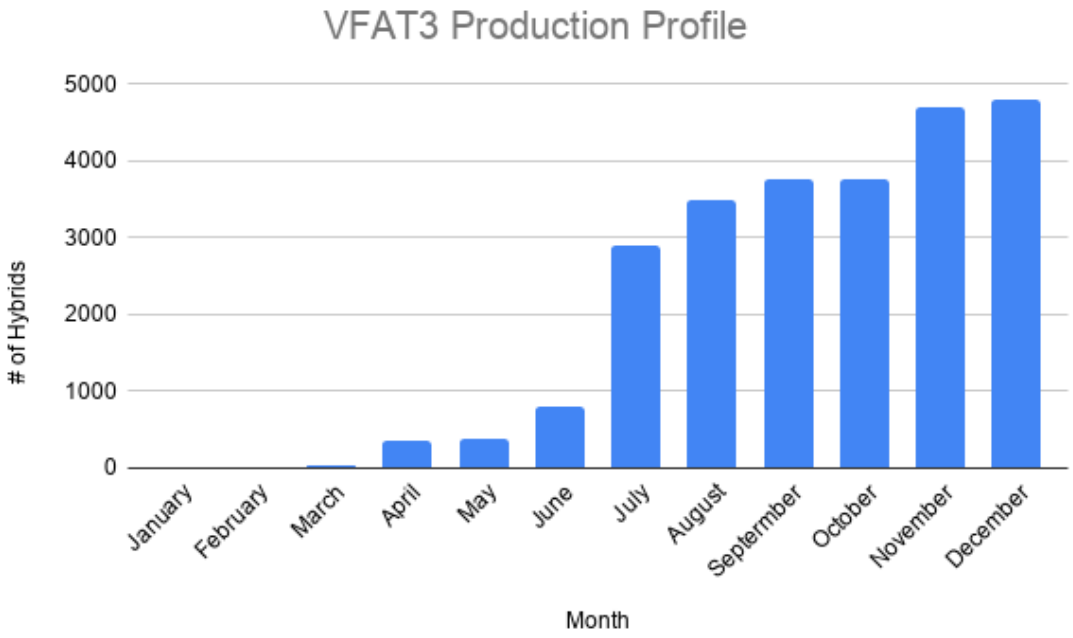


Figure 7.26: A cumulative production profile for the VFAT3 production testing.

In the initial three months of the production phase, the throughput of the test system was low compared to the peak production month of July 2019. The reason for this sharp jump is that it took longer to finalize the bad-channel selection criteria to identify all types of bad channels robustly. Particular bad hybrids were analyzed, and training was adopted as reference criteria for the following production lots. A flex cable with additional detector capacitance was also added to obtain the exact, robust thresholds for hybrid selection. The target was to achieve repeatability of results between different terminal-to- terminal of the test system. Once a robust selection criterion was achieved with minimal parameter variations between test terminals, the production yield was boosted to provide a bulk of VFAT3 hybrids to the experiment. The significant number of VFAT3 hybrids required for the GEM installation is 3456 for all 144 GEM detectors. Once the critical number was delivered to the integration team, a relatively low uniform pace was maintained until total production was completed in December 2019.

Due to the adoption of strict quality acceptance criteria on production hybrids and tight test criteria implementation on the testbench, a uniform yield was expected in each lot. An important bar graph displaying the number of hybrids with green, yellow, and red hybrids and relative percentages of good hybrids is shown in Figure 7.27.

An overall production yield of 89.4 % is achieved, representing green hybrids. The production test system only rejected 10.6 % of the hybrids. This plot also shows a relatively low number of hybrids in the initial lots, and a considerable rise is visible during lot number 7, which was completed in July 2019. An increased yield of 94 % is achieved for lot numbers 1 and 2. These represent the initial tuning phase of bad-channel criteria, which is finally adjusted before lot number 3. The test system initially missed a few tens of some hybrids with bad channels, and the GEM integration team identified them during the QC-7 phase of the GEM QC. A detailed breakdown of the 10.6 % rejected hybrids is also shown in Figure 7.28. This bar graph shows the relative percentage of the different kinds of problematic hybrids rejected during production. Internal ADC issues,

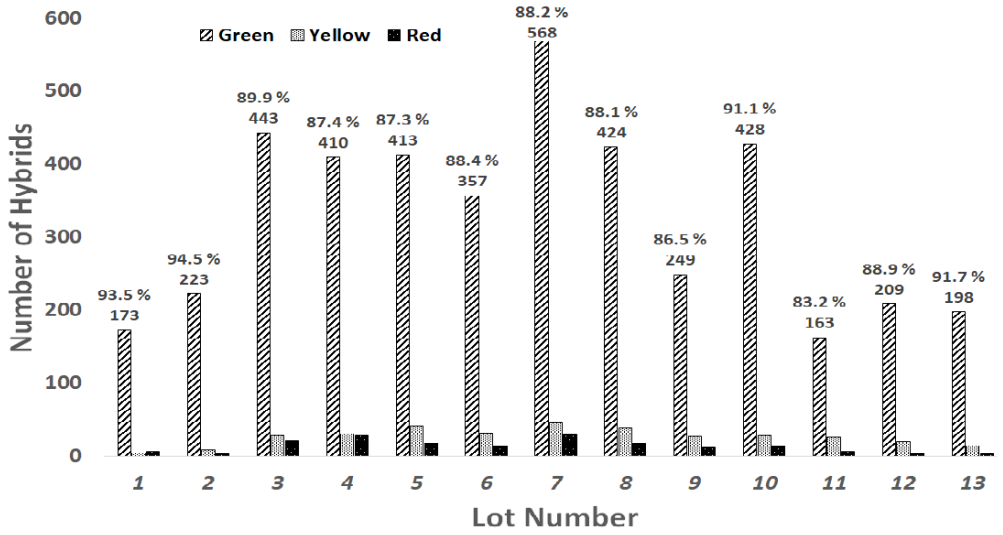


Figure 7.27: A bar graph showing VFAT3 hybrid production yield

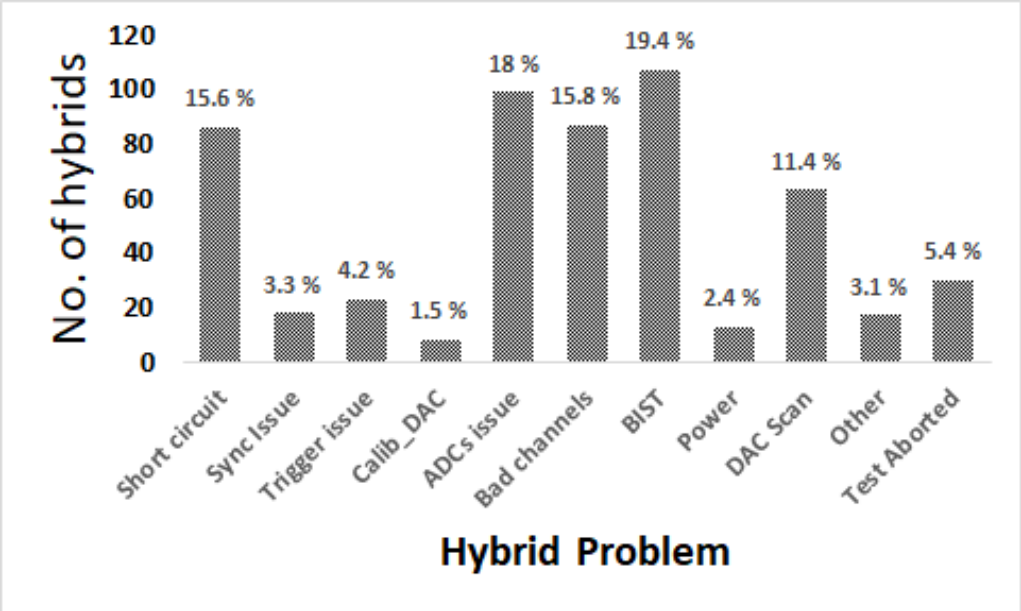


Figure 7.28: A detailed breakdown of the 10.6 % rejected hybrids showing different modes of failures of hybrids during production testing

broken Memories, dead channels, and hybrid shorts were the most frequent issues found during production. VFAT3 is wire bonded to the hybrid PCB, and many of the faults encountered during the production tests may be correlated to bonding imperfections. Dead Analog channels mainly occurred due to missing bonds, and short-circuit reflects shorts between neighboring bonds. This illustrates the challenge to bond the VFAT3 die on a small PCB, as it was discussed in Section 7.3.3. The three main issues encountered during the production phase were broken memories, broken ADC, and noisy Analog channels.

7.7 Summary

An industry-like VFAT3 hybrid QC, comprehensive and fast production test bench was developed to test the 5000 of the VFAT3 hybrids for GE1/1 GEM stations. The production test speed was optimized for two minutes per hybrid, starting from 30 minutes per hybrid characterization time with the characterization system. This was achieved by implementation of time-consuming blocks to HDL and controlling with a MicroBlaze processor within the Xilinx Kintex-7 FPGA.

VFAT3 prototype hybrid faced several manufacturing issues. These issues also influenced future mass production strategy and testing procedures. The major hybrid issues were over-etching, plating defects, and pad catering. The plating defects can result in nodules that increase local stress concentrations and lead to crack formation upon exposure to excessive temperatures. Pad cratering is the separation of the pads from the resin. Several critical changes were made in production hybrid design to overcome manufacturing issues. During PCB manufacturing, starting with a base copper thickness of 5 µm and achieving the desired thickness of 22 µm by applying several layers of metal plating electroless nickel immersion gold (ENIG) process helped to overcome manufacturing issues.

As a standard choice, a 25 µm bond wire thickness for VFAT3 Alumunium wire bonding was chosen. It is also supported by the majority of the leading wire bonders. 25 µm thickness also ensures sufficient current for power pins up to 1 A per bond. Like PCB manufacturing, VFAT3 bonding also proved to be quite challenging, and 45 µm pad width showed fabrication tolerances reducing pad sizes up to 30 µm. This 30 µm pad width was insufficient to tolerate bond-wire expansion, and it contributed in shorts with neighboring pads and scratching of nearby bond wires by the bonding tool. The reduction of bond wire diameter to 18 µm helped to achieve the optimum yield and added reliability in the process along with 500 mA of allowance for a single bond-wire. VFAT3 has a small power requirement of just a few milliamperes per pin due to many power pins, so this reduction of wire thickness did not affect device power delivery.

Several PCB and bonding shorts tests were added to verify the manufacturability and bonding of hybrids. The test bench evaluated all VFAT3 front-end noise levels using internal injection pulses of varying amplitudes. The test system also thoroughly checked the internal calibration and bias blocks of the devices. A production yield of 89.4 % was achieved, including device and hybrid assembly losses. A production database was created to access and load the optimum configuration parameters for regular device operation. The database is centrally managed and available to the GEM DAQ system. It will be used for the whole HL-LHC GE1/1 operation.

Chapter 8

Future GEM detectors in CMS: A brief status

8.1 Introduction

The installation of three GEM stations is a vital part of the CMS phase-2 muon upgrade. The first station, GE1/1, was installed during LS2 (2019-2021). The GE1/1 detector system is the precursor of the two future GEM stations, namely GE2/1 and ME0. The construction of GE2/1 has been started in 2021. Its installation in CMS is planned for the next (EYETS) of 2024. For ME0, the R&D phase is close to its end; the installation is planned during LS3.

This chapter briefly discusses the importance of GE2/1 and ME0 systems in the CMS physics program and the key improvements made over the GE1/1 system. The experiences gained during the GE1/1 system and lessons learned from electronics debugging and discharge mitigation studies that are ported to these systems are also discussed. The VFAT3 BGA packaging and design of the new rigid-flex plugin PCB are also the predecessors of GE1/1 hybrid design work. Finally, improvements in powering scheme and VFAT3 chip-ID encoding for GE1/1 have also been adopted for these new systems.

8.2 Introduction to GE2/1 and ME0 Detector Systems

The GE2/1 and ME0 detectors are also trapezoidal GEM detectors like GE1/1 and will cover the pseudo-rapidity region $1.6 \leq| \eta |\leq 2.4$ and $2.03 \leq| \eta |\leq 2.82$ respectively as shown in Figure 8.1.

The GE2/1 detector will be installed at the back of the ME2/1 CSC stations. The main goals of GE2/1 detector installation are to extend the GEM detector acceptance region to $2.15 \leq| \eta |\leq 2.4$, which will enhance the redundancy of particle trigger and tracking to CSC measurements. With the addition of GE2/1 and including GE1/1, a robust track reconstruction and reduction in the Level-1 trigger rate enhanced the transverse momentum reduction thanks to the extended local lever arm between GEM and CSC detectors. There are no iron yoke layers between GEMs and CSC detectors, and there is almost no multiple scattering.

A GE2/1 chamber covers an area of 1.45 m^2 and consists of four complete single detector modules with full functioning on-detector electronics. The GE2/1 is the largest state-of-art GEM detector in the world. The complete GE2/1 system comprises 72 chambers, each covering 20.3° of the YE0 disc, with 36 chambers per muon end-cap arranged in two layers. ME0 detector system consists of 6 layers of triple-GEM chambers covering

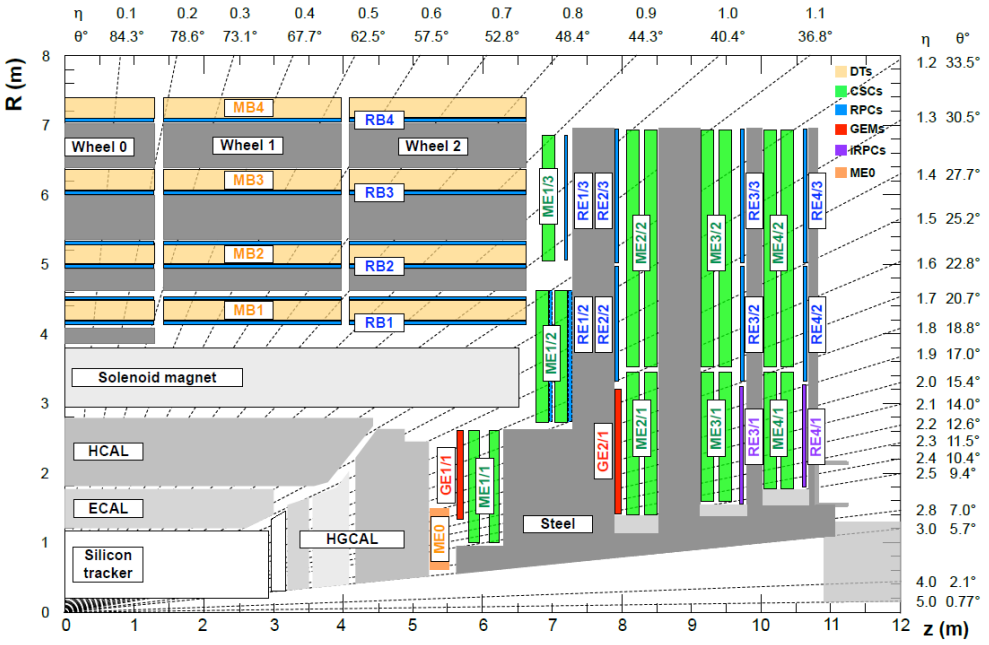


Figure 8.1: An R-z cross-section of a quadrant of the upgraded CMS detector. GE1/1 and GE2/1 detectors are shown as red bars, while ME0 GEM is shown in orange.

20° on CMS disc. ME0 Chamber dimensions are slightly smaller than GE1/1 due to spatial placement near the CMS end-cap Calorimeter. A total of 18 ME0 stacks per end-cap will cover the entire area, with 36 stacks for both end caps.

The ME0 detector will cover the very forward muon region and significantly extend the muon acceptance up to $\mid \eta \mid = 2.82$. Unlike GE1/1 and GE2/1, these stations will be installed in an entirely new space just behind the future CMS Calorimeter. This region has a high background rate and is out of reach of all existing muon systems. This installation will enable CMS to detect multi-muon final states and rare forward particle production processes. Also, ME0 will provide new trigger information in the forward region, which was not available by any existing muon subsystems. The ME0 GEM will have a six-layer detector stack providing up to six measurement points per event, which will enhance the redundancy to reject neutron-induced backgrounds.

The GE2/1 detectors are the largest, and ME0 detectors will be the smallest of the three stations. The GE1/1 and GE2/1 consist of double layers of GEMs, while ME0 consists of 6 layers of GEMS. The three GEM stations are compared in Figure 8.2 showing the relative size difference between the rings. The key design and operating specifications of all three detectors are also shown in Table 8.1. It can be seen that GE1/1 is the baseline design for all three GEM stations. All the extensive R&D done for GE1/1 is used to build robust GE2/1 and ME0 detectors. Almost all the detector fabrication, electronics testing, and CMS integration steps for GE1/1 have been adopted as a baseline for GE2/1 and ME0 detector systems.

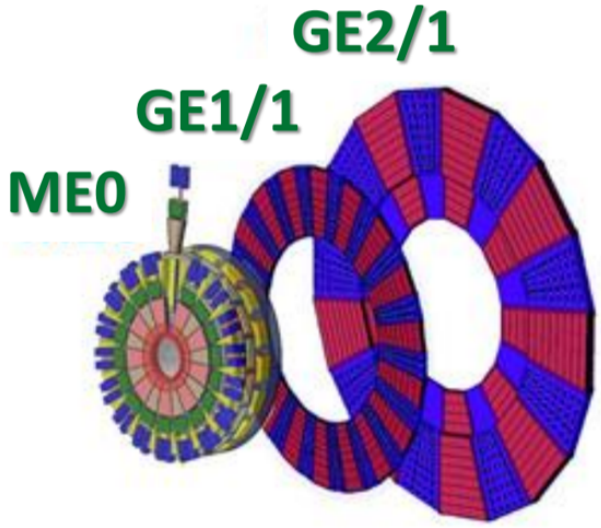


Figure 8.2: GE1/1, GE2/1, and ME0 rings show the relative size difference.

	GE1/1	GE2/1	ME0
Installation	**LS-2 (2019-2020)**	**LS-3 (2024-2026)**	**LS-3 (2024-2026)**
Start of data taking	**Run-3**	**Run-4**	**Run-4**
Number of Detectors	**144**	**72**	**216**
Coverage in ϕ	10°	20°	20°
Chamber Thickness	**35 mm**	**36.6 mm**	**33.4 mm**
Chamber Dimensions for GE1/1: short (Long)	**L: 106.1 (121) cm W: [23.1 (23.1) - 42 (44.6)] cm H: 0.7 (0.7) cm**	**L: 183.3 cm (Center-line) W: (53.3 - 177.4) cm H: 0.72 cm**	**L: 78.8 cm (Center-line) W: (23.6 - 51.4) cm H: 1.8 cm**
Active Area	**0.345 m^2 (short) 0.409 m^2 (long)**	**1.45 m^2**	**0.296 m^2**
Geometric Acceptance in η	$1.61 - 2.18$**; short** $1.55 - 2.18$**; long**	$1.62 - 2.43$	$2.03 - 2.8$
Readout Strips / stack GE1/1 & GE2/1: 2 layers per stack ME0: 6 layers per stack	**6144** (3072×2)	**6144** (3072×2)	**18432** (3072×6)
Gas Mixture	Ar/CO_2 **(70:30)**	Ar/CO_2**(70:30)**	Ar/CO_2 **(70:30)**
Nominal Drift Voltage	**3200 V**	**3200 V**	**3200 V**
Gas Gain	$1\text{-}2 \times 10^4$	$1\text{-}2 \times 10^4$	$1\text{-}2 \times 10^4$

Table 8.1: A comparison of key design & operational parameters of CMS GEM detectors GE1/1, GE2/1, and ME0. The last three rows show that GE1/1 is a baseline design for the next two detectors.

8.3 VFAT3 suitability for GE2/1 & ME0

In the Chapter 4, the phase-2 compatibility of VFAT3 for GE1/1 operation is presented. All parameters of the VFAT3 discussed earlier are also compatible with GE2/1 and ME0 GEM stations. The main differences between these detector characteristics are tabulated in the table 8.2. The VFAT3 analog front-end baseline restores within 500 ns, which provides a rate capability of 2 MHz per channel. Thus the front-end is fully capable of sustaining GE2/1 and ME0 hit rates (*The highest L1 rate per channel in ME0 is expected to be 96 kHz*). Regarding the gain linearity, VFAT3 gain plots at all three possible gains (Low, Medium, and High) are shown in Figure 8.3.

The Low and Medium gain settings show good linearity for full charge ranges, but the High gain linearity is reduced for higher GEM charges. So it is better to use the Medium or Low gain for both GEM detectors.

The total strip capacitance directly affects the VFAT3 equivalent noise charge (ENC).

Parameter	Value		Notes
	GE2/1	ME0	
Hit rate per channel (Gain $\approx$ 8000)	$< 2.6\ kHz$	$< 46\ kHz$	Max. GE2/1 hit rate: 700 Hz/cm^2 Max. ME0 hit rate: 48 kHz/cm^2
Signal charge per strip - 96% have charge above - MPV - Mean - Maximum	 2 fC 4 fC 11 fC 115 fC	 2 fC 4 fC 11 fC 115 fC	For MIP-like particles at gain 8000; (based on GE1/1 measurements)
Capacitance to ground per channel (min-max.)	$(3-4)\ pF$ $(8-10)\ pF$	$(2-4)\ pF$ (like GE1/1)	No GEB (GE2/1) with GEB (GE2/1)
Total strip capacitance (min-max)	$(33-41) pF$	$(10-22)\ pF$	GE2/1:$\approx$ 1.5 pF/cm ME0 strip lengths are $6.7-13\ cm$

Table 8.2: GE2/1 & ME0 compatibility with VFAT3

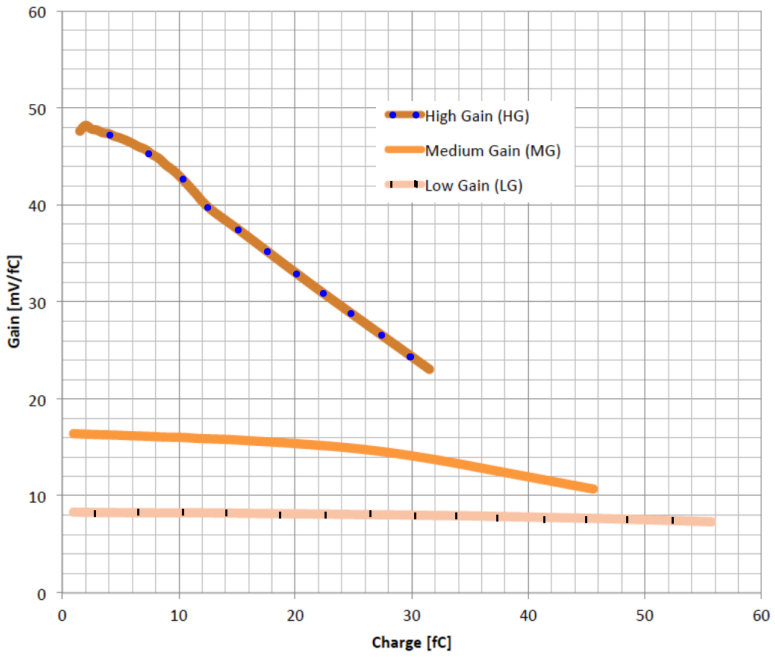


Figure 8.3: VFAT3 gain linearity at High, medium, and Low gan settings

The capacitance to the ground varies with the strip area, while the inter-strip capacitance varies with the strip length and pitch. The measured interstrip capacitance for GE2/1 based on the original TDR design was 25.8 pF, including facing copper plate [107]. The new modified geometry with double strip width and half strip length resulted in 20.1 pF interstrip capacitance, the same as the GE1/1 detector. Hence the expected noise contribution due to strip capacitance in GE2/1 and ME0 systems would be similar to the GE1/1 system.

Finally, VFAT3 is designed to be compatible with the GBT and has SLVS levels with a common mode of 200 mV. The LpGBT, a new version of gigabit transceiver that will replace the GBT in ME0, has SLVS levels with a common mode of 600mV. The LpGBT is backward compatible with GBT and can accept VFAT3 SLVS common mode of 200 mV.

8.4 Front-End electronics improvements concerning GE2/1

During GE1/1 front-end electronics design and integration phase, several important observations were recorded. Some of them were implemented in the GE1/1, and others were proposed for GE2/1 and ME0 GEMs. VFAT3 packaging, VFAT3 channel protection, plugin card design, and modified power distribution for new GEMs are recommended.

8.4.1 VFAT3 packaging

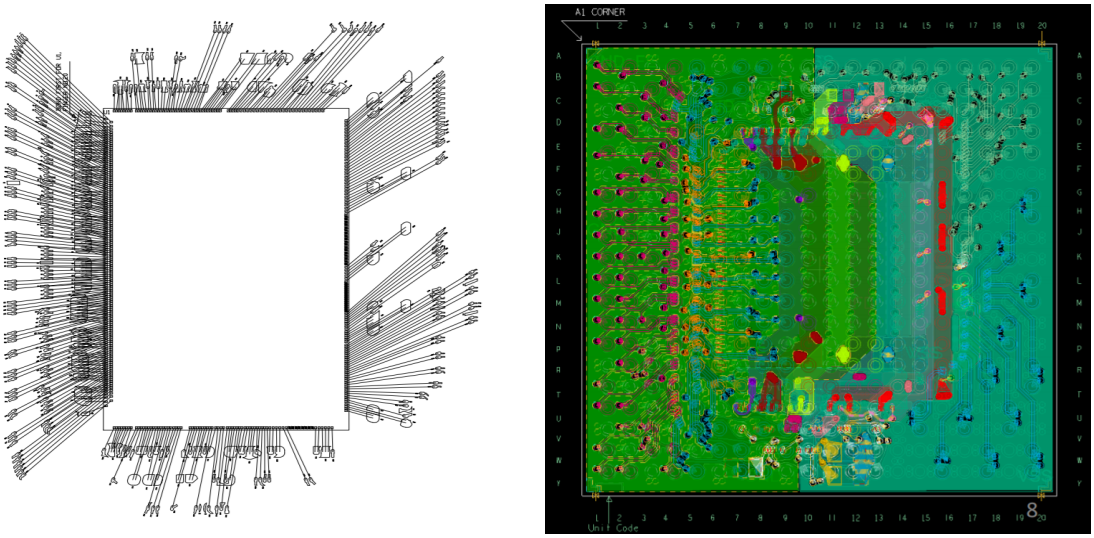
The GE1/1 hybrid used a bare VFAT3 die, and the mounting of such a complex chip on board made the wire bonding step more complicated. The robustness of the hybrid was slightly compromised in the GE1/1 production hybrid. It added extra care in the handling of the GE1/1 hybrid. Several production issues attributed to the use of the bare chip, including pad catering, over-etching on channel landing pads, and breakage on the PCB surface, were a few of the problems encountered during GE1/1 hybrid mass production (see Chapter 7).

It was decided to package the VFAT3 chip for GE2/1 and ME0 detectors to achieve better production yield, robust GE2/1 front-end PCBs, and reduced noise interference to the chip. The packaging will also provide a more straightforward PCB design and more reliable standard BGA soldering during future production. The VFAT3 is packaged in a full Ball Grid Array (BGA) plastic package. The package substrate is a small PCB designed by advanced techniques that host VFAT3 die and connect die pads and solder balls. The plastic encapsulation made the whole package protected and robust against vibrations and electromagnetic interference. The key features of the VFAT3 package are shown in table 8.3. The bonding diagram and layout of the package design are shown in

Package Parameter	**Value**
Ball Grid Array	20×20 *matrix*
Package Size	17 mm^2
Ball Pitch	800 μm
Encapsulation	Plastic
Bonding	Ball bonding
Ball Solder Composition	SAC 305 (96.5% Sn, 3% Ag, 0.5% Cu)

Table 8.3: VFAT3 packaging specifications

Figure 8.4.



(a) VFAT3 package bonding diagram showing die connectivity wth the substrate. The analog channels are on the left side of the chip.

(b) VFAT3 package substrate PCB layout. Analog and digital power planes are separated to enhance signal integrity and reduce cross-talk

Figure 8.4: VFAT3 package design bonding diagram and package layout.

8.4.2 Additional VFAT3 input protection

During the GE1/1 discharge mitigation studies, the underlying discharge propagation and damage processes were deeply analyzed. Different versions of VFAT3 hybrids were also used to quantify the discharge propagation strength and analyze damage probability with real VFAT3 channel destruction. Keeping in mind the difficulty of changing miniature multiple protection components on small hybrids, a proposal to design and fabricate a Sandwich board, which could be placed between GEB and VFAT3, is presented. The schematic view of the channel protection components for the Sandwich board is shown in Figure 8.5. The circuit consists of discharge propagation prevention components and

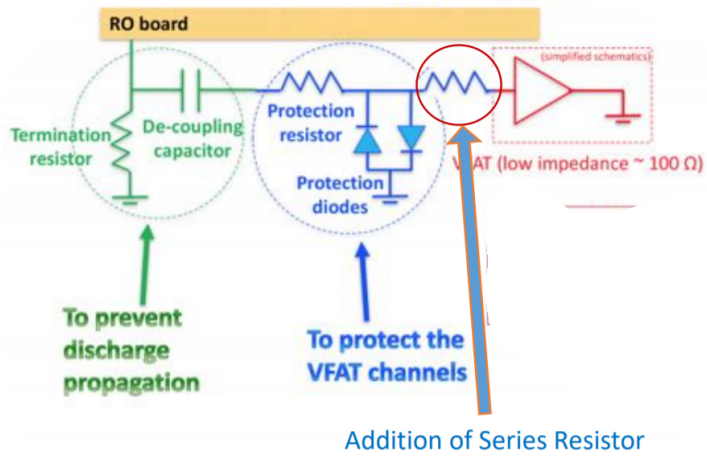


Figure 8.5: Sandwich board schematic for discharge protection studies.

a damage protection sub-circuit. The main objective of the Sandwich board is to help search for the most efficient protection circuits and appropriate component values for

GE2/1 and ME0 discharge mitigation. The existing GE1/1 baseline hybrid (HV3b_V2) is used, and different combinations of protection components on the Sandwich board were evaluated to find the most optimum and robust solution for new detectors. The use of the Sandwich board accelerated the search for an optimum solution without fabricating different VFAT3 hybrids with multiple protection schemes and layouts. The larger components used on the Sandwich board can be replaced easily, and different VFAT3 channels are tested with different protection schemes simultaneously. The final subset of the protection circuit for the GE2/1 detector is discussed in section 8.6.3. The PCB layout of the Sandwich board is shown in Figure 8.6.

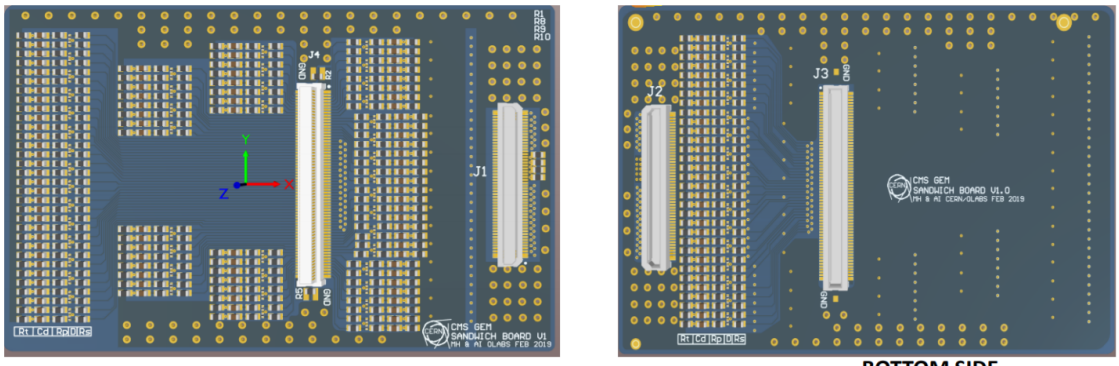


Figure 8.6: Sandwich board layout designed to accelerate discharge mitigation studies for GE2/1 & ME0 detectors. The mechanical dimensions of PCB are $94.9 \times 60.7\ mm$.

Four Panasonic connectors were used in the Sandwich board for connection with GEB and VFAT3 hybrids. The circuit is routed to insert protection components between readout strips and VFAT3 input channels. The digital signals from hybrid are passed through on the Sandwich board without any modifications.

8.4.3 Plugin card

The GE2/1 uses packaged VFAT3 chip mounted on a rigid-flex PCB called a plugin card. The analog channels are routed on flex cable to absorb the stress on the connectors, which improves plugin connectivity with the system compared to the GE1/1 hybrid. A new 140-pins Hirose connector (J1) was used for the flex part, and a 100-pins Panasonic connector (J2) was used on the rigid part of the plugin for connection with the GEB. A prototype plugin for the GE2/1 system is shown in Figure 8.7.

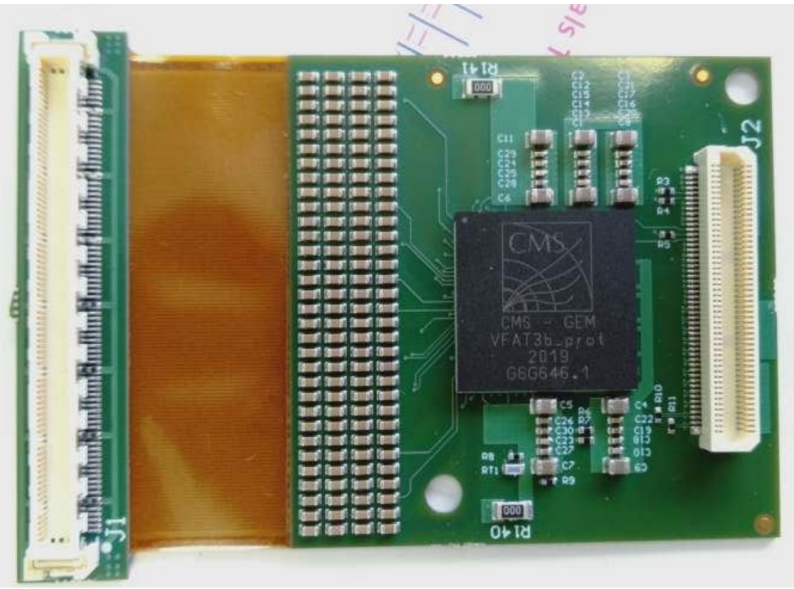


Figure 8.7: GE2/1 plugin card

A total of 110 GE2/1 plugins have been produced by January 2021 and tested with the existing GE1/1 VFAT3 production test system. The GE2/1 plugin was designed to maintain pin compatibility with GE1/1 hybrids with the addition of three digital pins for HDLC addressing at spare connector locations. The subtle differences between plugin and hybrid PCB design are the packaged chip, large, robust protection components, and a 140-pin Hirose connector on the channel side of the plugin card.

8.4.4 Power distribution

VFAT3 has four different power domains, namely AVDD, DVDD, VDD-IO, and VDD-efuse. To simplify the layout of hybrid and GEB electronics boards, VDD-efuse and VDD-IO have been tied to a digital power domain (DVDD = 1.2 V). GE1/1 experience showed that VDD-efuse needed to be at 2.5 V to avoid bit flipping of Chip-ID. Hence, the power scheme for GE2/1 and onward has been modified to separate the VDD-efuse and VDD-IO from the rest of the supplies and tied to separate 2.5 V. This would completely mitigate the Chip-ID and communication issues in the future GEM systems.

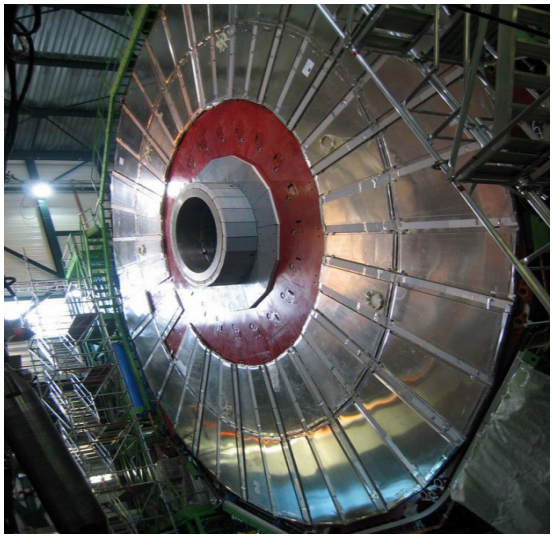
8.5 GE2/1 Detector System

The following sections will discuss the GE2/1 detector position constraints, geometry and construction, electronics system, and detector performance.

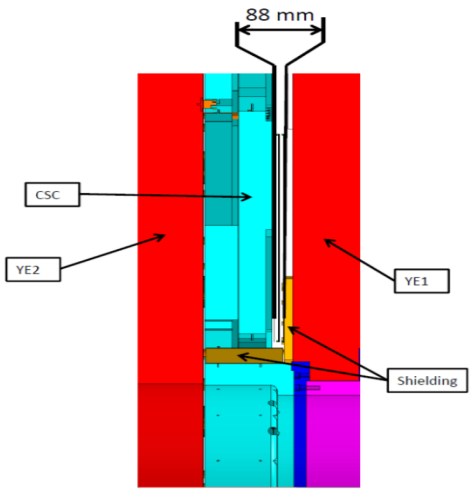
8.5.1 GE2/1 position & constraints

GE2/1 detectors will be installed on the back of YE1, station2 of CMS spectrometer. All the services for GE2/1 have been installed during the LS2 shutdown. The vacant ring on YE1 of CMS is shown in Figure 8.8a.

GE2/1 has to be inserted in the available space left on YE1. The already existing CSC station is only 153 mm away from YE1. Note the presence of a thick shielding layer of 65 mm, just after YE1 leaving only a limited space of 88 mm for the GE2/1 detector. The expected fabrication thickness of a full GE2/1 super-chamber is around 74 mm, just like



(a) YE1 station-2 GE2/1 installation position.



(b) GE2/1 installation space requirement

Figure 8.8: GE2/1 installation position & spce requirement.

GE1/1, still leaving a margin of 14 mm. The GE2/1 geometrical clearance is shown in Figure 8.8b.

8.5.2 GE2/1 Geometry & Construction

The GE2/1 detector system comprises 36 trapezoidal super-chambers, each covering 20° in ϕ direction. The GE2/1 would be the largest GEM at the time, with dimensions of $\sim$ 2.5 times larger than the GE1/1. At present, there is no production facility in the world to produce PCBs with such large dimensions. So each GE2/1 chamber is divided into four trapezoidal sub-modules having a separate readout board (ROB), GEM electronics Board (GEB), and Optohybrid. Like the GE1/1 detector, two GE2/1 detectors are joined together to form a super-chamber. In total, eight different GE2/1 sub-modules are aligned, four on each side to have one full GE2/1 super chamber. As shown in Figure 8.9, the individual module geometry has been optimized to avoid any muons passing through successive "cracks" or dead areas. This results in the design of eight modules called M1-M4 on the back chambers (with reference to the interaction point) and M5-M8 on the front chambers.

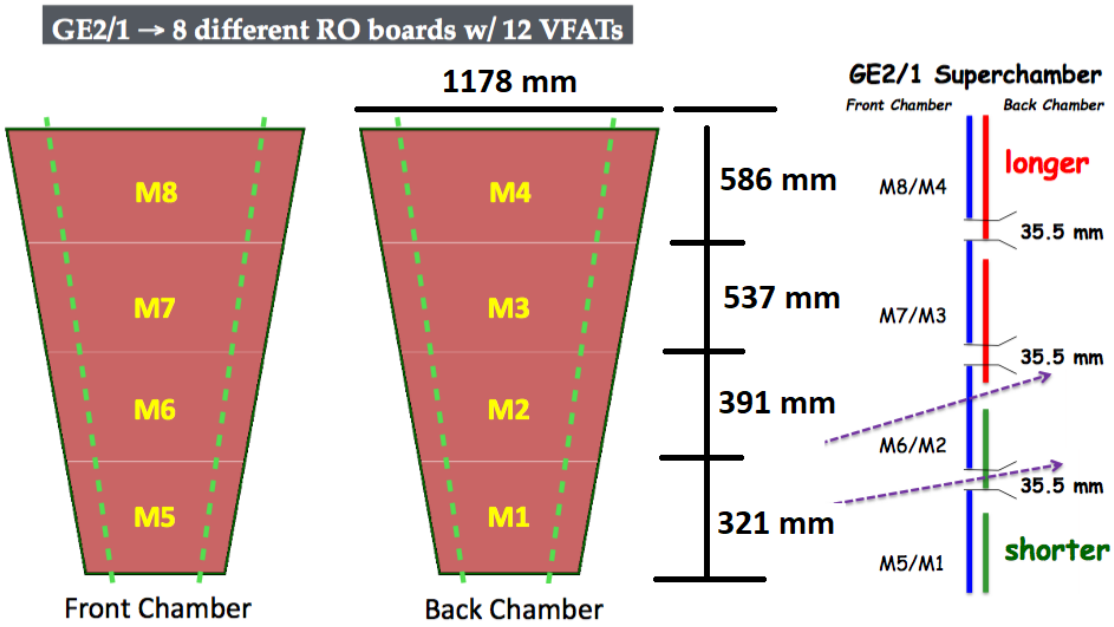
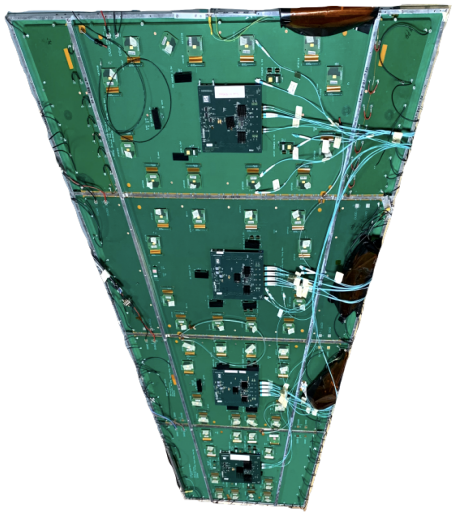


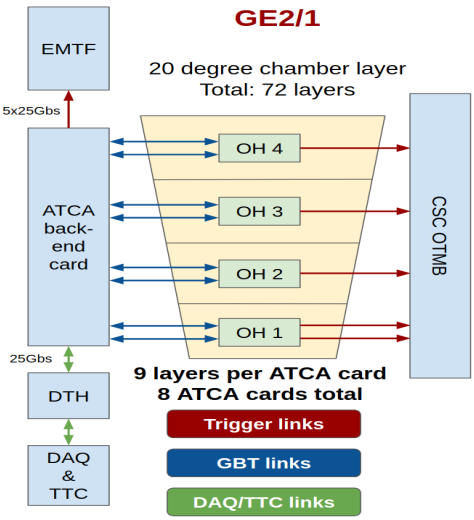
Figure 8.9: GE2/1 triple-GEM module numbering (left) and the overlap between the front and back chambers (right) that minimizes the gaps in the acceptance. [108]

8.5.3 GE2/1 Electronics System

Each GE2/1 module behaves as an independent detector. Each module has its ROB, GEB, 12 VFAT3 plugin cards and one Optohybrid as seen in Figure 8.10a.



(a) GE2/1 detector with full on-detector electronics



(b) GE2/1 electronics system interfaces

Figure 8.10: GE2/1 electronics

Figure 8.10b shows a block diagram of the GE2/1 electronics system. Each GE2/1 detector module has its Opto-hybrid, linked to the back-end system through two GBTs running 4.8 Gbps bidirectional links. Thus in total, $288 \times 2 = 576$ links are used to connect front-end plugins to the back-end through VTRx optical transceivers. In each Opto-

hybrid, these links communicate 12 VFAT3 chips and route clock, TTC, and slow control signals to the chips. Besides, the GBT links are used to communicate with the SCA, which controls ADC, I2C, JTAG, and GPIO signals. Finally, the links are also used to provide FPGA communication with the back-end electronics. These links provide remote programming of FPGA, slow control data transfer, clock distribution, and s-bit trigger data reception. The distribution of bandwidth between all these interfaces is listed in table 8.4.

Interface	12xVFAT3	SCA	FPGA programming	FPGA, TTC & slow control	Trigger data	Total
Backend TX	3.84 Gb/s	80 Mb/s	640 Mb/s	320 Mb/s	N/A	4.88 Gb/s
Backend RX	3.84 Gb/s	80 Mb/s	N/A	320 Mb/s	3.52 Gb/s	7.76 Gb/s

Table 8.4: GE2/1 OptoHybrid interface bandwidth breakdown

Table 8.5 summarizes the number of components required for GE2/1 front-end electronics.

Component	Per Module	Per Chamber 20°	Per endcap	In full GE2/1
VFAT3 Plugin card	**12**	**48**	**1728**	**3456**
GEB	**1**	**4**	**144**	**288**
OH	**1**	**4**	**144**	**288**
FEAST DC-DC	**5**	**20**	**720**	**1440**
VTRx	**2**	**8**	**288**	**576**
VTTx	**1(2 on M1 & M5)**	**5**	**180**	**360**

Table 8.5: Required number of GE2/1 front-end components

8.5.4 GE2/1 Detector Performance

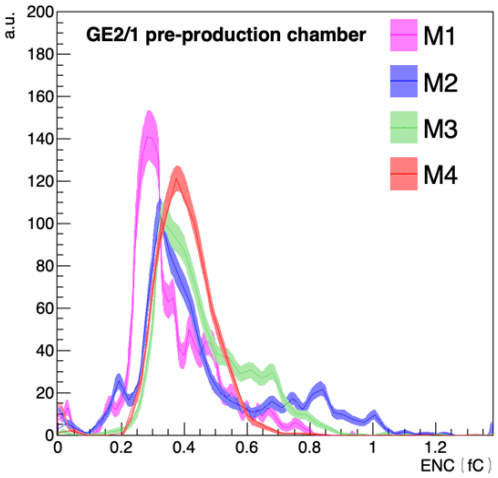
The GE2/1 performance measurements were obtained from a fully assembled pre-production detector. The detector was fully equipped with electronics; only the cooling plate and the Aluminium cover were missing. Figure 8.11a shows the distribution of the ENC measured on every VFAT3 channel of the M1-M4 modules of the pre-production detector.

The Lines indicate fitted response, and broad bands show fit uncertainties. The M1 module with the shortest strips indicates a maximum noise of 0.25 fC, while the M4 module with the large strip area resulted in a 0.4 fC noise peak. Most of the channels show noise below 0.6 fC for all VFAT3 positions.

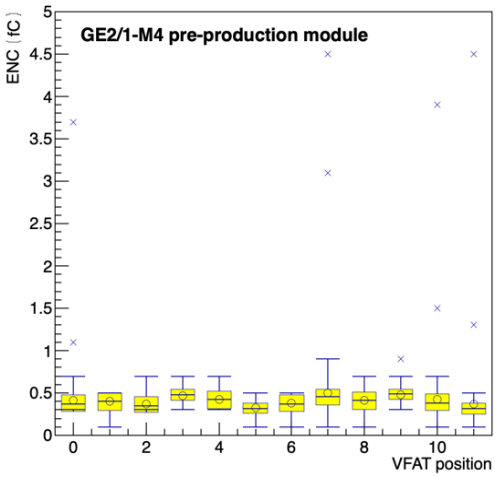
A box plot showing ENC measurement of M4 module per VFAT position is shown in Figure 8.11b. The yellow-colored boxes represent at least 50% of the channels. The 99.3% of the channels are within the horizontal lines. The small circles and lines within the boxes indicate the mean and median of ENC, respectively. These measurements indicate that noise is primarily uniform and independent of the particular VFAT3 position.

8.5.5 GE2/1 system design progress

Two GE2/1 chambers, one front, and one back are assembled, and performance testing was done in 2019. The firmware and software of GE2/1 are based on GE1/1 and ported to GE2/1 requirements. According to TDR, GE2/1 Optohybrid should incorporate new gigabit transceivers, namely Low Power Gigabit Transceiver (LpGBT) [109]. However, due to unavoidable production delays in LpGBTs, the use of well-proven GBTs is adopted for GE2/1. The GBTs will be used in "wide-bus" mode to achieve the required bandwidth



(a) Noise comparison plots for GE2/1 (M1-M4) modules. Lines represent the fitted values and bands represent fit uncertainties. [108]



(b) Box plot of the ENC extracted from the S-curves of the GE2/1 M4 module.

Figure 8.11: Noise performance plots of the first full GE2/1 pre-production detector made of M1-M4 modules

necessary for GE2/1 electronics. The 110 package plugin cards have already been produced and qualified on the GE1/1 VFAT3 test bench. These will be used to finalize the GE2/1 electronics chain and electronics system review in 2021.

8.6 Discharge protection studies for GE2/1

8.6.1 Baseline discharge mitigation study

During the GE1/1 slice test, VFAT2 channel loss was observed, and it was demonstrated that VFAT3 would suffer as well from damages in GE1/1 (see section 6.2.2). The assembly of the GE1/1 GEM part was finished at that time, so the focus was to reduce the damage probability by minimal permissible changes in the electronics design of the detector system.

Later on, a comprehensive study was launched to deeply understand and mitigate the channel loss issue for GE2/1 and ME0 detectors. It was discovered that GEM discharges are mostly confined within holes. Upon high voltage breakdown across holes, discharge can propagate towards the readout board and ultimately damage the front-end electronics. It is formulated that channel loss probability depends on three factors related to GEM discharges [110]. Mathematically, channel loss probability $P_{channel}$ can be written as:

$$P_{channel} \propto P_{discharge} \times P_{propagation} \times P_{damage} \tag{8.1}$$

where

$P_{discharge}$ is discharge occurrence probability
$P_{propagation}$ is the discharge propagation probability
P_{damage} is probability of damage produced by discharge,

GEMs, like any other MPGD detectors, will suffer from discharges. The obvious way to avoid them is to lower the detector gain, which will directly affect the detection efficiency. In triple-GEM detectors, it has been demonstrated that an alternative exists by reducing the probability of discharge propagation from foil to foil. Moreover, the addition of protection components on the front-end hybrid is recommended to reduce the channel loss probability close to zero.

The discharge probability was first understood with $10 \times 10\ cm^2$ small detectors. A discharge propagation phenomenon in CERN $10 \times 10\ cm^2$ detector is shown in Figure 8.12 below:

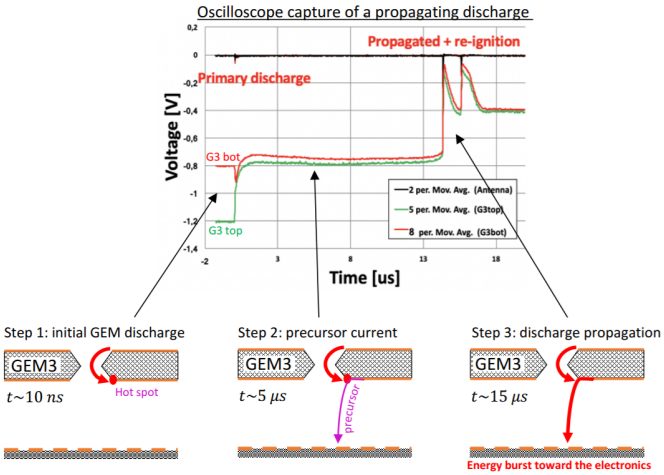


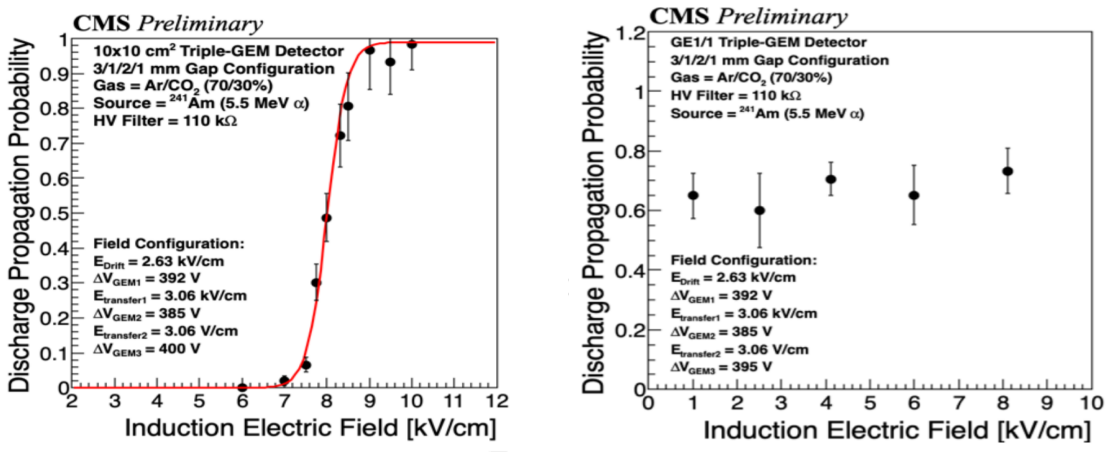
Figure 8.12: Three steps for a primary discharge to propagate to readout strips

When a primary discharge occurs, it creates a short circuit between the top and bottom of the GEM foil. A precursor current rises from the hot spot and becomes a streamer by energy stored in GEM foil. Ultimately secondary discharge occurs between GEM bottom and readout strips, thus destroys connected front-end channels. The discharge propagation probability as a function of the electric field in the induction region is shown in Figure 8.13a for a small detector.

The discharge propagation probability for small detectors can be made significantly low if the induction field remains below a threshold of $7\ kV/cm$. In general, CMS GEMs have an induction field between $4.1 - 4.5$ kV/cm.

It is observed that despite the low induction field used in large CMS detectors, the discharge propagation probability turned out to be significantly high, as shown in Figure 8.13b. The discharge propagation probability for GE1/1 detectors is around 0.7, independent of the electric field in the induction gap.

The discharge propagation process is complex in large area GEMs compared to small GEMS. The reasons are the storage of enormous energy in their foils and a high HV filter capacitor. It is observed that the primary discharge in GEM3 is systematically followed with a backward propagation towards GEM2 and GEM1 as shown in Figure 8.14. This backward propagation accumulates enough energy in the primary discharge to propagate towards the readout board even with sufficiently low induction fields. The GE1/1 detector with large foils acts as a large capacitor and stores a bulk of energy to induce discharge propagation towards the readout board. Reducing the gap capacitance is the way to control the foil energy. Moreover, the energy stored outside, such as HV filter capacitors, also worsens the issue. The adjustment of the filter resistor value proved to reduce the external energy transfer to the foils.



(a) Discharge propagation probability for $10 \times 10\ cm^2$ small GEM detector

(b) Discharge propagation probability for large GEM detector

Figure 8.13: A comparison between discharge propagation probabilities of small and large GEMs

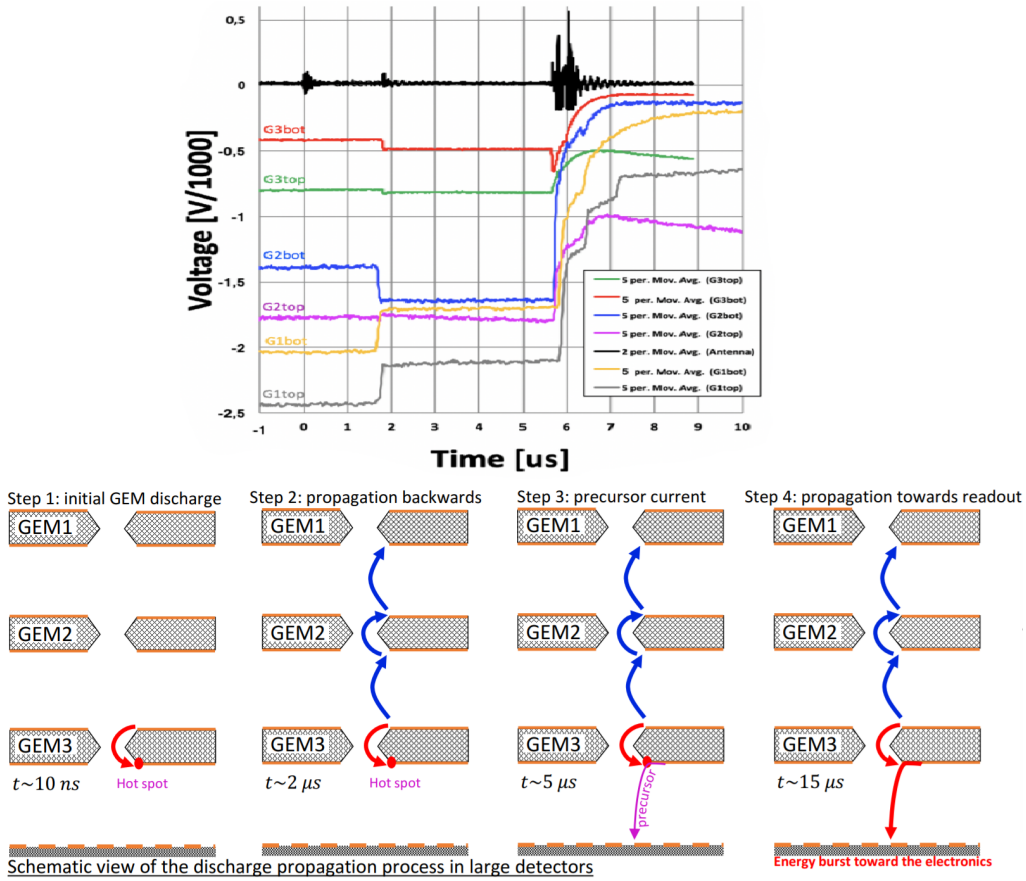


Figure 8.14: A four-step process for a discharge propagation in large GEM detector

8.6.2 GE2/1 double segmentation

GE1/1 GEM detector foils are top segmented to protect against regular discharges. A top segmentation principle is shown in Figure 8.15.

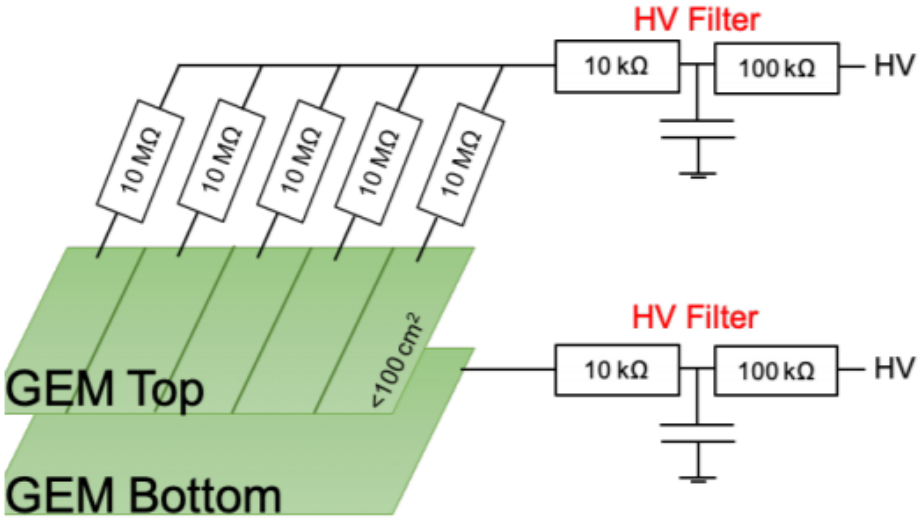
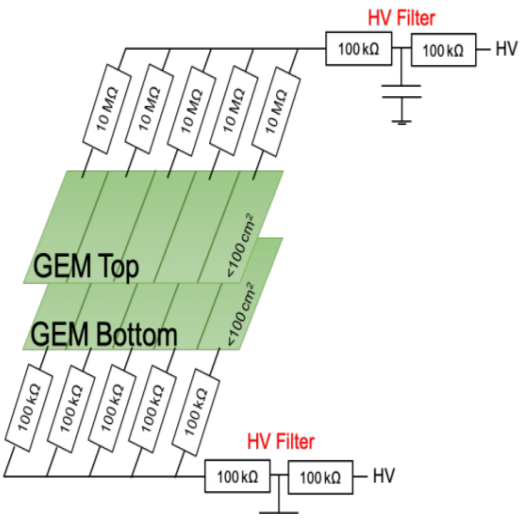
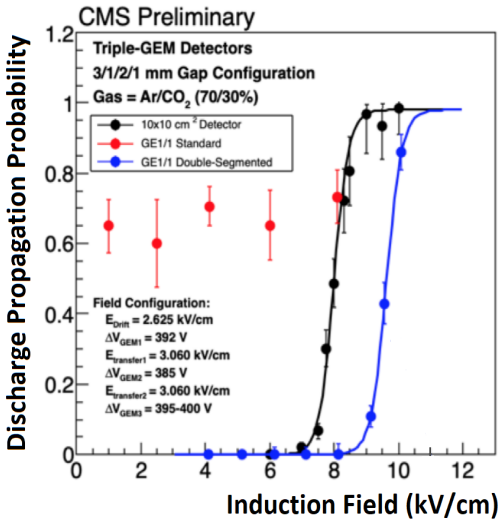


Figure 8.15: A top segmented foil to mitigate regular GEM discharges [110]

A double segmentation is also evaluated, and it was observed that double segmentation of foils (top and bottom segmentation) helps reduce discharge propagation to the readout board [110]. A double segmentation principle is explained in Figure 8.16a.



(a) A double segmented foil to mitigate GEM discharge propagation towards readout plane.



(b) Discharge propagation comparison between 10 × 10, single segmented GE1/1 and double segmented GE1/1 GEM detectors.

Figure 8.16: Double segmentation principle and discharge propagation comparison between single and double segmentation GEMs [110].

A comparison between discharge propagation probabilities of small $10 \times 10\ cm^2$ GEM, GE1/1 single-segmented and double segmented GEMs is shown in Figure 8.16b. The induction field for small GEMs showed a 7 kV/cm threshold. In small GEMs, only GEM3 and readout board are involved in discharge propagation. In large single-segmented GEMs, the propagation probability is large and uniform, around 0.7. All GEM layers and readout boards contribute to propagating discharges in single-segmented foils. For double segmented foils, the discharge probability behaved like small GEMs, and an induction-field threshold of 8 kV/cm is achieved, which shows its effectiveness. Better control of discharge energy is achieved with a significant reduction in propagation probability ($> 10^4$) by using double segmented GEMs.

However, a detailed evaluation of the double segmentation technique revealed problems associated with this method. The size reduction of HV segments on the last GEM enhanced the high-frequency impedance to the ground and induced a cross-talk effect between strips. The group of strips associated with the same HV partition indicated a cross-talk. The simulations showed (see Figure 8.17) that with the energetic incoming particles, the cross-talk induces unnecessary triggers in the electronics, which introduces a significant dead time of 50 bunch crossings with a typical energy deposit of 100 keV. Once triggered, the VFAT3 baseline returns to ground after 500 *ns*.

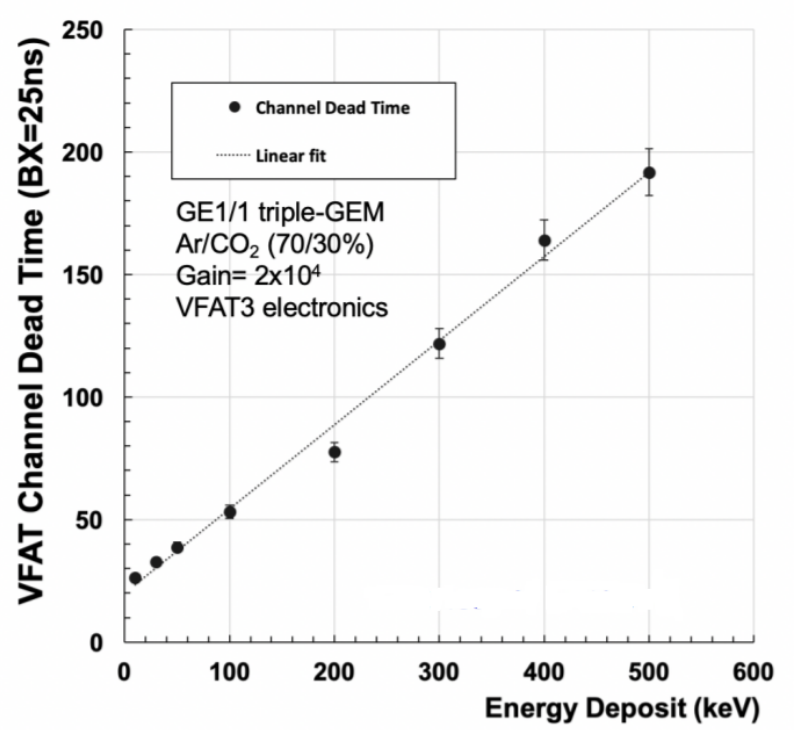
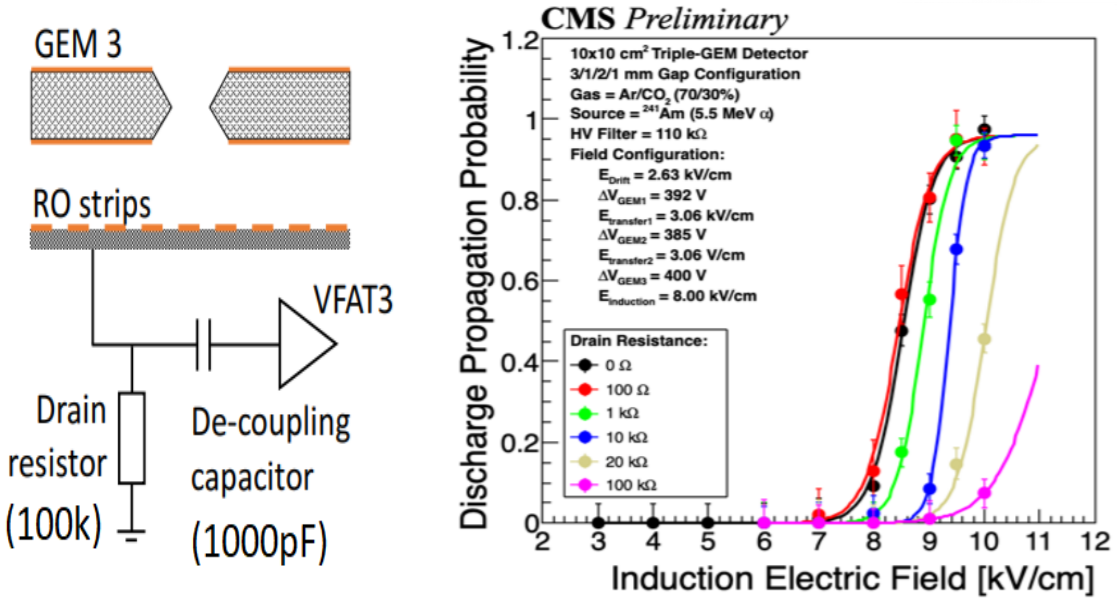


Figure 8.17: VFAT3 channel dead time versus deposited energy in to a channel (Simulation courtesy, F.Licciulli)

The final GE2/1 configuration is chosen based on the double segmentation method. A **"mixed segmentation design"** is finalized, which drastically mitigates the cross-talk effect. The mixed segmentation design uses double segmentation in GEM1 and GEM2 layers and single segmentation in GEM3. The double segmentation in GEM1 and GEM2 prevents the discharge propagation, while GEM3 single segmentation suppresses the cross-talk.

8.6.3 GE2/1 plugin protection circuit

Additional protection is added on the GE2/1 plugin to stop the discharge propagation at readout strip levels and protect the front-end channels. A sub-circuit chosen from a complete Sandwich board circuit is implemented in the plugin card to remove the discharge propagation towards front-end channels. A drain resistor and AC coupling capacitor combination are used for this purpose, as shown in Figure 8.18a.



(a) GE2/1 plugin protection circuit used to stop discharge propagation towards front-end channels.

(b) Variation of discharge propagation probability with different drain resistor values. The lowest propagation is achieved with 100 $k\Omega$ drain resistance.

Figure 8.18: GE2/1 plugin discharge protection circuit implemented on final prototype plugin-cards and selection of drain resistor plots

The idea is to drain the precursor current through a drain resistor before the formation of discharge. A voltage drop across the resistor momentarily suppresses the induction field. The resistor acts as a quenching device and prevents discharge propagation towards readout channels. A drain resistor of 100 $k\Omega$ is used in prototype GE2/1 plugin-cards, and a decoupling capacitor is also added to provide additional isolation. This reduced the propagation probability by at least three orders of magnitude [110]. Figure 8.18b also shows reduction of discharge propagation probability by the drain resistor of 100 $k\Omega$.

Table 8.6 shows that the estimated percentage of damaged channels for GEM operation in HL-LHC conditions will be 100% channel loss per ReadOut(RO) sector with baseline hybrid and no GEM foil double segmentation. This damage probability reduces to 4.79% per RO sector using HV3b_v3 hybrid with an external series resistor of 470 Ω and a modified GEM HV filter with 200 kΩ resistors. After successfully installing GE1/1 GEM detectors in CMS last year, further studies of discharge propagation led to the use of the semi-double segmentation GEM foil scheme [110] for GE2/1 and ME0 GEMs, which solved the issue of discharge propagation towards VFAT3 channels. This improvement brought down the discharge transfer probability from 0.5 to $<10^{-4}$. In addition, the implementation of a new robust R, C circuit scheme on plugin card brought down the induction propagation probability to $< 10^{-3}$. Combining the effect of these reduced probabilities

helped us achieve ∼0% damage probability for GE2/1 and ME0 of detectors for HL-LHC operation.

				Semi-double-segmentation	R+C circuit on plug-in cards	VFAT Protection circuit		
System	Max HIP Rate ($E_{dep} > 30$ keV)	Max Discharge Rate	Number of Discharges Per Year	Transfer Propagation Probability	Induction Propagation Probability	Damage Probability	Number of Damaged Channels per 10 years	Percentage of Damaged Channels per 10 years
Slice Test	3.15×10^3 Hz/ROsector	3.90×10^{-6}	39 per ROsector	0.5	1	0.95	185 per ROsector	100% per ROsector
GE1/1	3.15×10^3 Hz/ROsector	3.90×10^{-6}	39 per ROsector	0.5	1	0.03	6 per ROsector	4.79% per ROsector
GE2/1	1.92×10^3 Hz/ROsector	2.38×10^{-6}	24 per ROsector	$<10^{-4}$	$<10^{-3}$	0.03	7×10^{-7} per ROsector	∼0%
ME0	2.36×10^5 Hz/ROsector	2.93×10^{-4}	2.937 per ROsector	$<10^{-4}$	$<10^{-3}$	0.03	9×10^{-5} per ROsector	∼0%

Table 8.6: Summary of CMS GEM detectors discharge mitigation study and percent of channel loss during 10 LHC years with and without protection circuits [110].

8.7 ME0 Detector System

The ME0 electronics system design is already well advanced, and prototypes of almost every component are now available. ME0 GEM stations will extend the current η coverage from 2.4 to 2.8. This increase of coverage will enable us to record 20% more Higgs bosons events with four muons detection as shown:

$$H \rightarrow ZZ^* \rightarrow 4\mu \tag{8.2}$$

A record number of exciting physics events could be captured using six highly segmented layers of ME0 detectors. This detector will be segmented in 20° ϕ-slices with a total of 18 detectors per end-cap disc. Each detector layer is partitioned in 8 η and 3 ϕ layers. One readout board is assembled on top of each detector layer. In total, there are 384 strips per partition.

8.7.1 ME0 Geometry & Construction

The ME0 detector system consists of 36 module stacks, 18 in each end-cap [2]. Each ME0 stack is constructed with the six layers of triple GEM detectors staggered to achieve the active areas of adjacent stacks overlap in ϕ direction. A 3-D view of ME0 GEM detector is shown in Figure 8.19.

The ME0 GEB mechanical designs have been completed and consist of two different sub-modules per detector. Each GEB module will have two ASIAGO (ASIC And Gigabit Optics) Optohybrids as shown in Figure 8.20.

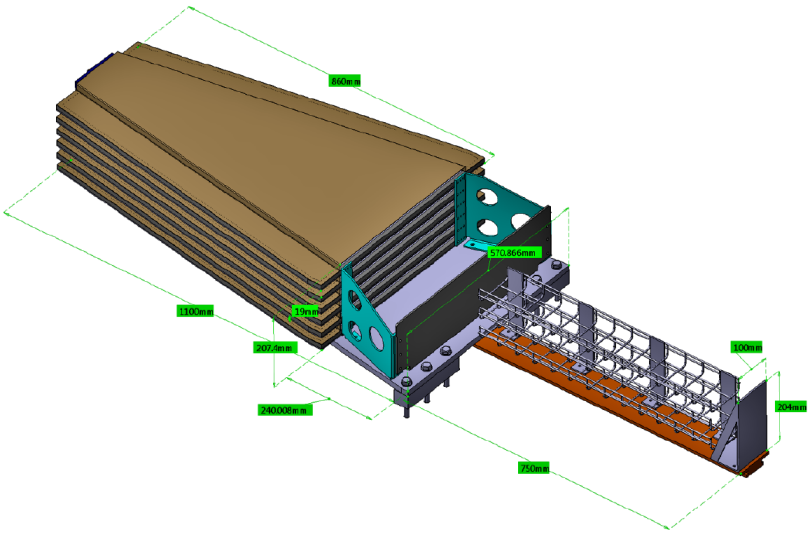


Figure 8.19: A 3-D view of ME0 stack showing six triple-GEM layers including cable trays shown in the lower right side.

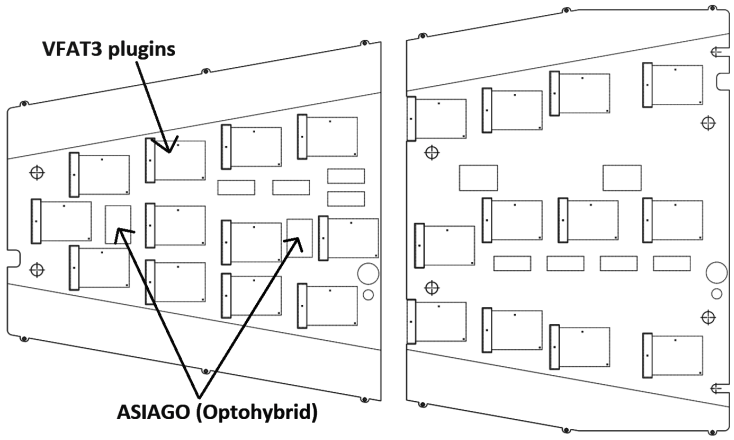


Figure 8.20: ME0 GEB consists of two separate PCBs each hosting 12 VFAT3 plugins and two ASIAGO Optohybrid with the LpGBTs. Each ASIAGO hosts two LpGBTs and each LpGBT communicates with 3 VFATs.

8.7.2 ME0 Electronics System

The ME0 electronics system is proposed and is being developed. A simplified block diagram of half a GEB is shown in Figure 8.21.

Each of the two GEB has one Optohybrid (ASIAGO) module, consisting of two LpGBTs. Each LpGBT is connected to 3 VFATs (plugin cards). Each VFAT3 sends trigger data via eight trigger links at 320 Mb/s to the LpGBTs. So one entire ME0 GEB board will have 2 ASIAGO boards. The ME0 detector will have 2 GEBs per layer (super-chamber) of the detector in CMS. In total, 12 GEBs will constitute six layers of ME0 covering 20° of the ϕ slice in CMS. The use of radiation-hard LpGBT for on-detector data processing is the most notable difference between ME0 and previous generations of GEMs. This LpGBT also provides two advantages over the old generations of Optohybrids. The first is the removal of on-detector FPGA for trigger data transmission. As particle rates are

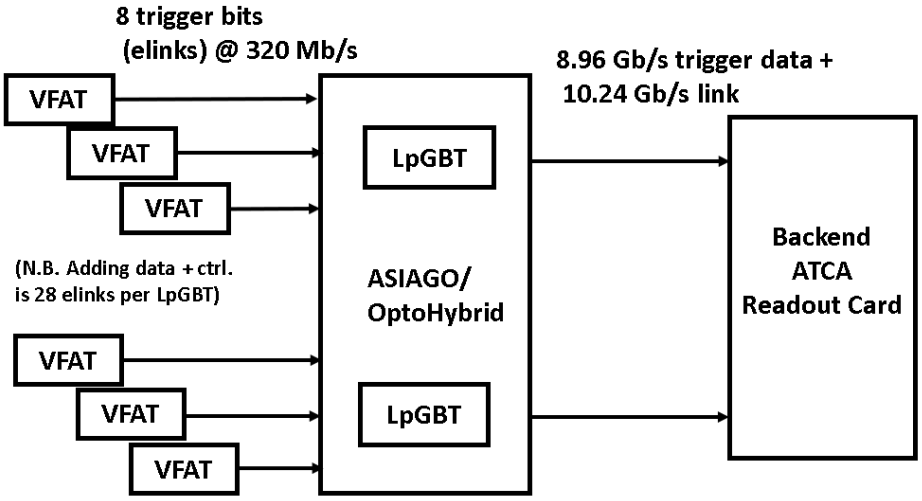


Figure 8.21: Simplified ME0 (Half a GEB) electronics system, showing uplink data-flow, without controls (A front-end perspective).

sufficiently high at the ME0 location, FPGA will not sustain high rates, and SEU rates will be high, interrupting regular device operation. Secondly, ASIAGO Optohybrid is small compared to its predecessors, which provides sufficient space for GEB routing and plugin-cards placement. The prototype of ASIAGO Optohybrid is shown in Figure 8.22.

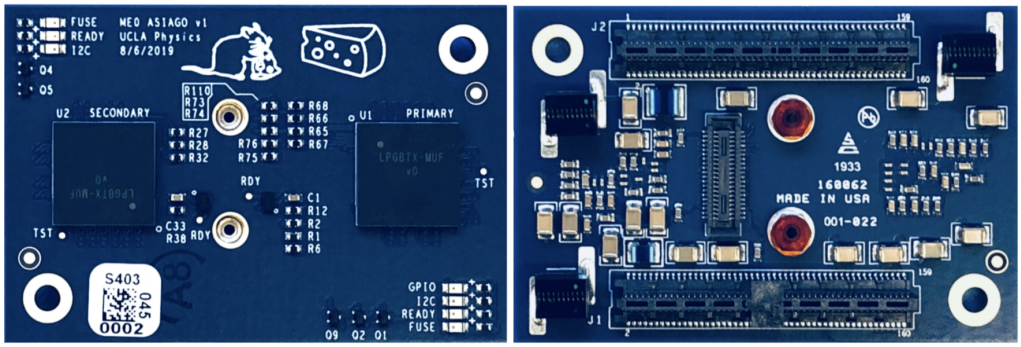


Figure 8.22: First prototype of an ME0 ASIAGO board

Each onboard LpGBT provides 5 to 10 Gb/s for uplinks and 2.5 Gb/s for downlinks with a Forward Error Correction (FEC)-5/12. It can work in the temperature range of -35° to $+60^{\circ}$. The chip is a small form factor having dimensions of $9 \times 9 \times 1.25\ mm$ with a total of 289 pins. The LpGBT also provides one 10 bit ADC, one 12-bit voltage DAC, one 8-bit current DAC, a temperature sensor, three I^2C masters, and a 16-bit general-purpose input-output (GPIO) port to facilitate the user to control and monitor on-detector electronics. A radiation hardness up to 200 Mrad TID is proven, and non-ionizing Energy loss (NIEL) radiation up to 10^{15} 1-MeV n_{eq}/cm^2 is tested, which is mainly a concern for Optoelectronic chips in radiation environments. The SEU tolerance is enhanced by using novel low jitter clock and data recovery (CDR) and phase lock loop (PLL) circuits [111].

The back-end electronics for ME0 strictly used typical LHC Phase-2 back-end systems, including DTH, Central DAQ, and EMTF processor subsystems. A block diagram of ME0 back-end electronics is shown in Figure 8.23.

Each ATCA card communicates with two detector stacks (6-layers) on the back-end side, covering 40° in ϕ. A total of 96 10.24 Gbps links are used per ATCA card for the trig-

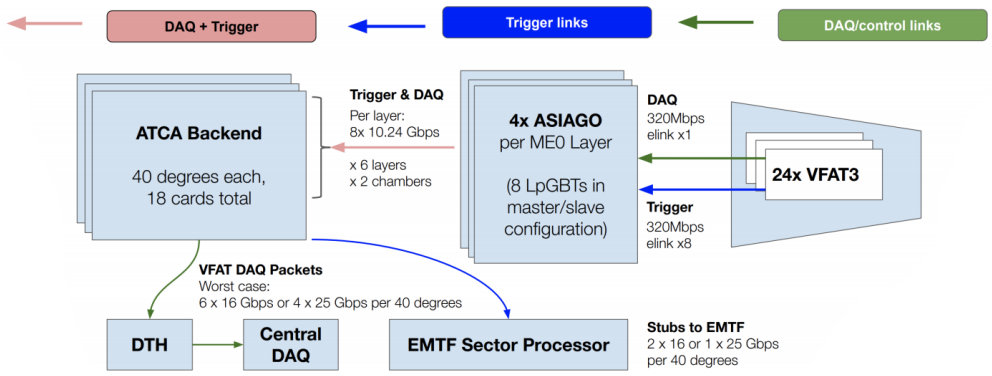


Figure 8.23: ME0 whole system block diagram

ger, Data Acquisition (DAQ), and control communication with LpGBTs. On the backed side of ATCA, one 25-Gbps (or two 16-Gbps) and four 25-Gbps (or six 16-Gbps) links are used to communicate with EMTF and DTH concentrator modules.

8.8 Summary

The GE2/1 and ME0 detectors are in the R&D phase, and laboratory testing is well advanced, particularly for GE2/1 detectors. Both have utilized the experience gained from extensive GE1/1 R&D and CMS installation. Many issues encountered during GE1/1 implementation have been resolved for GE2/1 and ME0. These improvements are the VFAT3 packaging, the redesign of the VFAT3 hybrid in the plugin card, including a flexible PCB and improved input channel protection, and the optimization of the GEB power scheme to avoid chip-ID bit-flip.

The GE2/1 detectors are the largest of three stations, while ME0 detectors will be exposed to much higher particle rates and radiation levels. Thanks to its six detection layers, ME0 will enhance the CMS muon trigger and tracking coverage up to $\eta \approx 2.8$. A new asset for the CMS muon system.

GE1/1 has been installed in CMS in 2019-2020 and will take part in CMS data taking during Run-3, from 2022. The GE2/1 and ME0 will be installed during LS-3 starting from 2024. All three GEM stations will be fully exploited to search for new physics during the Phase-2 run of the CMS starting after 2026.

Chapter 9

Summary

This research work has been performed in the framework of the CMS muon Phase-2 upgrade program. For Phase-2, the LHC will increase its instantaneous luminosity from 10^{34} $cm^{-2}s^{-1}$ to 5 x 10^{34} $cm^{-2}s^{-1}$. This phase is commonly called the High-Luminosity LHC or HL-LHC. With this rise of instantaneous luminosity, the particle rates and radiation levels, which the LHC experiments will have to sustain, will increase accordingly. To levels the experiments have not been built for. The LHC experiments are therefore preparing major upgrades as well.

In CMS, to maintain and improve the muon triggering and tracking performance, three rings of Triple-GEM detectors will be installed. The first one, called GE1/1, has been installed in 2019 and 2020. GE1/1 is the precursor of the two others, GE2/1 and ME0 which will be installed in a couple of years from now.

With GE1/1, it is the very first time large (1m-long) Triple-GEM detectors are used in CMS. To meet the phase-2 requirements in term of trigger and tracking, a dedicated ASIC had to be designed: the VFAT3. The VFAT3 consists of 128 channels, low power, low noise front-end, highly configurable through an on-chip calibration block. The data transfer and device control is performed through a fast communication port operating at 320 MHz. VFAT3 uses these fast-links to transmit trigger and tracking information to backend electronics through dedicated links. The GEM detectors will have a considerable variation in readout strip capacitance due to radial strip geometry. The VFAT3 should perform well for the whole GEM capacitance range and background particle flux.

The VFAT3 architecture, design specifications, and expected Phase-2 compatibility requirements were discussed. A detailed functional characterization of the device is performed to evaluate its internal submodules. The front-end channels were characterized by the injection of external and internal pulses. A detailed characterization of internal ADCs and DACs was performed. The front-end noise and threshold levels were calibrated with and without threshold trimming. The device's functional characterization showed that VFAT3 is compatible with the entire Phase-2 LHC operation.

The CMS environment has high radiation levels. Several radiation tests for VFAT3 were conducted, up to several Mrads of TID, to extrapolate device aging and short term radiation damages in HL-LHC conditions. All three GEMs stations will receive up to 1 Mrad of TID during ten HL-LHC years. VFAT3 indicated flawless operation up to 35 Mrad TID. Complex devices like VFAT3 also suffer from random digital nodes upset by a single high energy particle strike. This upset can alter the device configuration or lead to memory corruption. Several SEU tests were done to find the device cross-section for high energy ion-beams at the Louvain-La-Neuve Cyclotron facility. The register saturation cross-section proved extremely low due to the device's digital logic triplication. A frequent device synchronization loss was observed during the beam test. An extrapolation to the HL-LHC conditions was calculated for the device synchronization loss. This

calculation showed one VFAT3 synchronization loss after 65 hrs, 138 hrs, and 2.3 hrs for GE1/1, GE2/1, and ME0 of detectors, respectively, in the HL-LHC environment. The ME0 sync-loss rate is slightly higher, thanks to frequent global resets issued by central DAQ and CMS trigger; this event could be dominant by global resets. In the worst case, a dedicated rest request can be issued to the Central CMS DAQ system by the affected GEM detector to issue a global reset, provided the rate of reset request is kept low.

In 2017, five GE1/1 super-chambers were installed in the muon endcap. The primary purpose was to attain the GEM operational experience and look for critical GEM electronic chain issues. It was observed that VFAT3 input channels could be destroyed by GEM discharge propagation towards readout strips. Many design improvements have been made in the VFAT3 hybrids to sustain the high voltage discharges produced in the GEM detectors. This channel loss investigation resulted in the reduction of damage probability from 93% to just only 3% after the addition of series protection resistors. Implementing the VFAT3 hybrid in the GEMs also revealed observation of bitflips in the device e-fuse. The e-fuses are used to assign a unique chip_ID to every hybrid. It is used to distinguish and load correct configuration data for the device's proper functioning in the GEM detector. A multi-bit encoding scheme named as Reed-Muller (RM) encoding was implemented to correct the e-fuse bit-flipping. A maximum of three bits was corrected by Reed-Muller encoding scheme, which proved to be sufficient to mitigate the issue.

A production worthy VFAT3 hybrid is designed and fabricated. The chip-on-board choice made the fabrication of hybrid PCB difficult. Several design improvements were made to facilitate the wire-bonding of the hybrid easier. The reduction of bond-wire thickness from 25 μm to 18 μm made the wire-bonding process robust and production worthy. A mass-scale production of VFAT3 hybrids was done to produce 5000 hybrids. These hybrids have been integrated in the 144 GE1/1 detectors covering both muon endcaps. All these hybrids were fully characterized and qualified on a fast and efficient production test bench, designed using Xilinx Kintex-7 FPGA and Microblaze soft processor. The complete production testing of one hybrid just took two minutes, which is highly efficient compared to 30 minutes of test time achieved with the characterization test bench. An extensive configuration and calibration data is generated during hybrid testing. The hybrid's proper operation is not possible until correct configuration parameters are loaded to corresponding hybrids from the database. A CERN Database on Demand (DBoD) central database engine was integrated with the VFAT3 database to retrieve all the tested hybrids' data during the CMS's device operation. The mass production was completed with a net yield of 89.4 %, including die and bonding losses.

Several lessons were learned from GE1/1 electronics design and implementation. Several recommendations were provided for the future GEM stations, GE2/1 and ME0. The critical change is the packaging of VFAT3 for the next GEM detectors to improve the robustness and noise performance of the next generations of plugin cards. Robust discharge protections were implemented with the help of a Sandwich board R&D, explicitly designed for GE2/1 and ME0 discharge protection campaign. The new GE2/1 plugin cards' size is increased more than twice compared to the existing GE1/1 hybrid to host HV surface mount components. The GE1/1 production test bench is being ported to test the prototype GE2/1 plugin cards. A total of 110 GE2/1 plugin cards have been tested initially with a mean noise of 0.2 fC with the existing GE1/1 test bench. The Reed-Muller multi-bit encoding is adopted for future GEM plugin card chip_ID encoding scheme. Several design recommendations were also provided to adjust future electronics' power rails for better noise performance concerning front-end channels.

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Glossary

ADC Analog to Digital Converter. 66

BSM Physics beyond the Standard Model (BSM) refers to the theoretical concepts required to explain the limitations of the Standard Model. 14

CBM Calibration, Bias, and Monitoring block in the VFAT3 to configure the analog front-end.. 56

CSC Cathode Strip Chambers are used in the muon endcap disks where the magnetic field is uneven with high particle rates. 24

DAC Digital to Analog Converter. 76

DT The Drift Tube detector measures muon positions in the barrel region of CMS detector. 24

DUT Device Under Test. 114

EYETS Extended Year-End technical Stop. 175

FPGA Field Programmable Gate Array. 76

HDLC High-Level Data Link Control. 71

HL-LHC The High Luminosity Large Hadron Collider is an upgrade to the LHC.It is started in June 2018 and will increase the accelerator's potential for new discoveries in physics, starting in 2027. 21

RPC Resistive Plate Chambers are muon detectors used for the muon trigger and transverse momentum measurements, both in barrel and endcap regions . 24

SEE Single Event Effects. 104

SEU Single Event Upset. 114

SLVS Scalable Low Voltage Signaling . 82

SPS The Super Proton Synchrotron (SPS) is the second-largest machine in CERN's accelerator complex, with 7 km in circumference, it takes particles from the Proton Synchrotron and accelerates them to provide beams for the Large Hadron Collider. 15

TID Total Ionizing Dose. 104

Appendix A

Radiation tolerance of HGCAL LDO

A.1 Introduction

This work describes a major contribution of the author in radiation characterization of a low dropout (LDO) linear regulator chip designed for the front-end electronics of CMS endcap calorimetry HL-LHC upgrades. The main motivation behind this work begins form the fact that Dr. Aspell joined the calorimetry project as an electronic co-ordinator and he decided to explore the radiation characterization experience of the author (learnt in GEM project) to the new project.

A.2 Introduction to HGCAL

After the third long shutdown (LS3) the HL-LHC operational phase will be started somewhere in last quarter of 2026. The instantaneous luminosity will then be increased to 5 x 10^{34} cm^2 s^{-1} with the aim to integrate 3000 fb^{-1} by the mid-2030s. The corresponding pileup per bunch crossing will be increased to 140. The integration of ten times more luminosity during HL-LHC poses significant challenges for radiation tolerance and event pileup on endcap calorimetry in the forward region. The CMS collaboration has decided to build and instrument a new high granularity calorimeter (HGCAL) for the CMS endcaps region.

The primary objective of the calorimeter is to measure the energy of the charged and neutral particles accurately. In addition, the calorimeter also measures the angle, position, and time of arrival of incidence particles. The core function of the calorimeter is to slow down the incoming particles until they stop. During this slowdown, showers of less energetic particles are generated inside the calorimeter. Different incoming particles interact with the calorimeter in mainly two different ways, namely electromagnetic and hadronic interactions. The electrons, positrons, and photons interact with nuclei and electrons electromagnetically. In contrast, hadrons and other particles, made of quarks, interact primarily through the strong nuclear force and produce complex hadronic showers.

The HGCAL calorimeter is also segmented into electromagnetic (CE-E) and hadronic (CE-H) compartments. A large number of Hexagonal modules based on Si sensors will be used in CE-E, and high-radiation regions of CE-H are shown in green color (see Figure A.1). In the blue part of the CE-H region with low-radiation, scintillating tiles with SiPM readout will be used. A combination of lead, copper and sintered copper tungsten will be used as absorbing material in the CE-E compartment, while stainless steel plates will be used in the CE-H compartment. The HGCAL will cover the pseudo-rapidity region of $1.5 \leq |\eta| \leq 3.0$ and comprises a total weight of 215 tons per endcap. A total of 6 Million Si

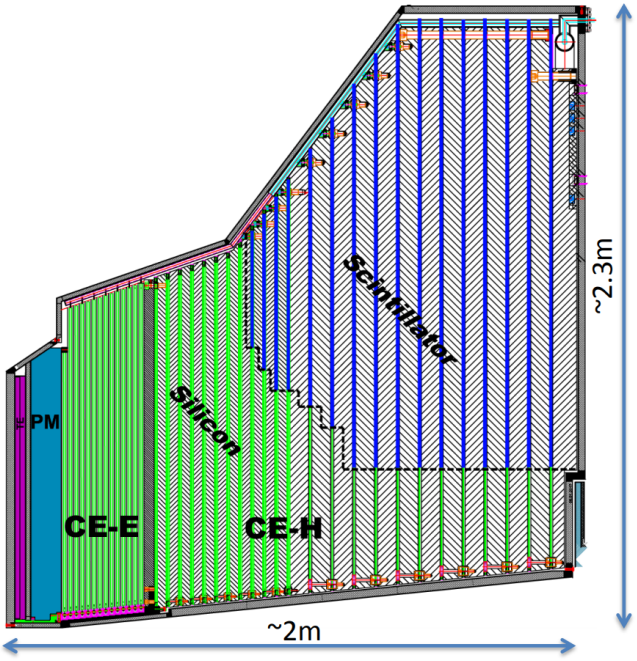


Figure A.1: Schematic view of CMS HGCAL calorimeter showing Electromagnetic calorimeter (CE-E) with Si sensors and Hadronic calorimeter (CE-H) compartments with both Si and scintillator detectors.

channels will be used having 0.5 or 1 cm^2 cell size with smaller cell size sensors placed at higher fluence regions. This totals to 620 m^2 of silicon sensors in 30,000 Hex-Modules. A total of 400 m^2 of scintillators will be deployed in 4000 boards totaling 240,000 scintillator channels, having 4-30 cm^2 cell size. The complete calorimeter detection system will be operated at -30°C to reduce the dark currents produced by sensors. In the HGCAL region of the CMS, the highest dose is around 2 MGy (200 Mrad). Such high radiation levels will be encountered at the inner levels of the detector. Figure A.2 shows ionizing radiation dose accumulated in HGCAL after an integrated luminosity of 3000 fb^{-1}. Using phase-2 geometry of CMS, the new calorimeter must have the ability to tolerate integrated radiation levels, which are ten times higher than anticipated in the baseline CMS design. The FLUKA simulations indicated highest fluence can cross 1 x 10^{16} $n_{eq}cm^{-2}$ as shown in Figure A.3.

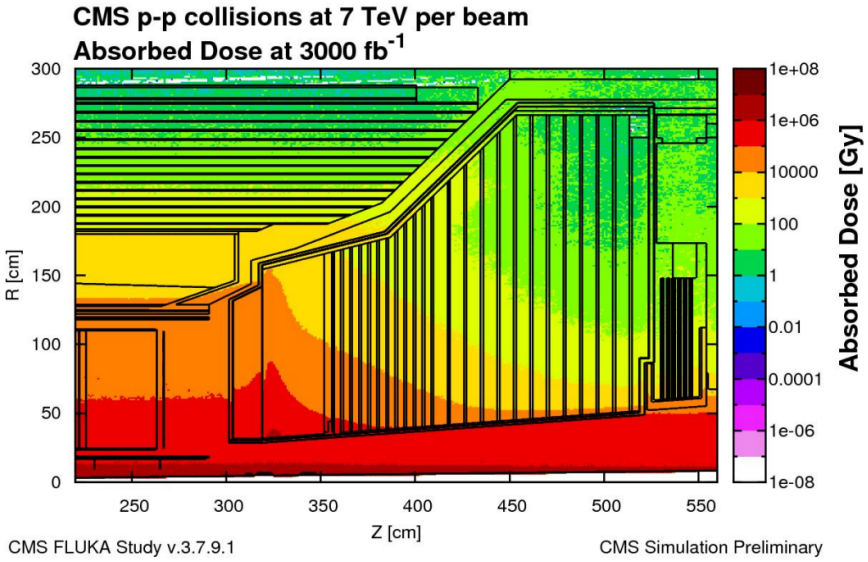


Figure A.2: Ionizing radiation dose accumulated in HGCAL after an integrated luminosity of 3000 fb^{-1}. Simulated using the FLUKA program. The two dimensional map shows absoebed dose both in radial and longitudinal coordinates, r and z [112].

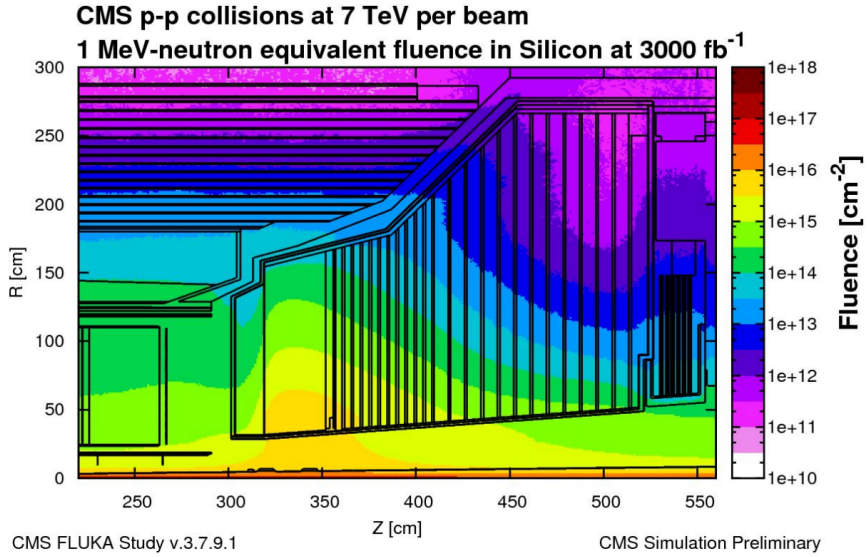
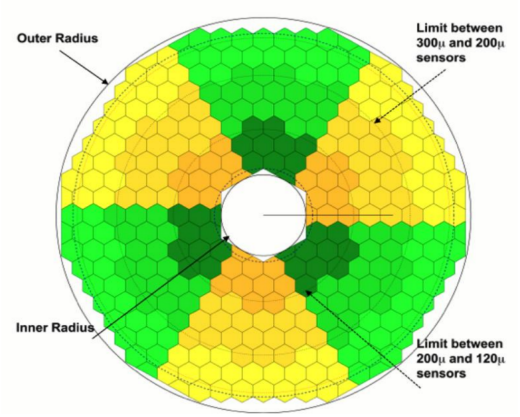


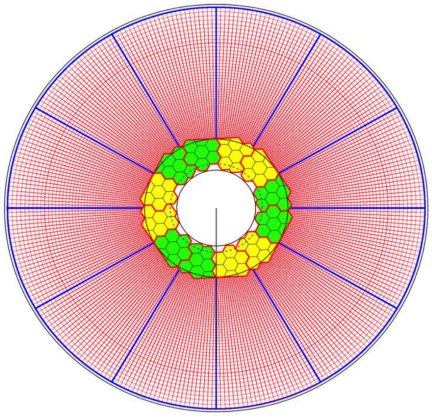
Figure A.3: Accumulated neutron fluence in HGCAL after an integrated luminosity of 3000 fb^{-1} [112].

HGCAL detector is arranged into large cassettes made of a cooling plate with silicon and scintillator modules mounted on it (see Figure A.4). The Front-end electronics located on the Hex-modules, with readout and control through the engine and wagon motherboard system. The wagons are passive PCBs with various shapes and sizes and will be used for connectivity of the front-end Hex-Modules to the engines. The engines (shown in red) are the PCBs with always same size and contain LpGBT chips and communicates with multiple Hex-modules through wagons. The detector arrangement inside a cassette is shown in Figure A.5

A hexagonal silicon module is shown in Figure A.6. Silicon sensors are the first use



(a) Silicon-only HGCAL layer in CE-E region, showing cassettes and variation of proposed silicon sensor thicknesses



(b) Mixed layer ring of sensor in CE-H region. Silicon sensors are used at higher particle flux regions and scintillators will be used in relatively low particle rate region.

Figure A.4: Wedge-shaped cassettes are visible both in CE-E and CE-H regions of the HGCAL. Six cassettes constitute one full disc of CE-E (left), and 12 cassettes cover a full CE-H region (right). (drawings not to the same scale!)

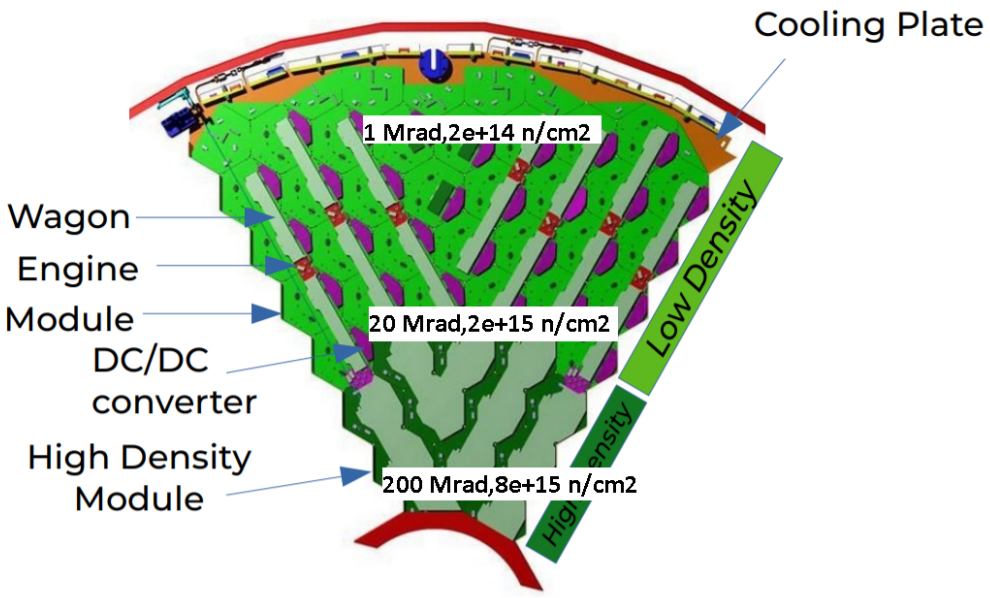


Figure A.5: The cassette arrangement for CMS HGCAL system. Six cassettes will cover one slice of disc for CE-E region and twelve cassettes will cover one disc in CE-H regions.

of 8" technology for large-scale HEP sensors. The hexagonal geometry has been chosen to maximize the use of the wafer area.

A Si-module is assembled as a glued stack of the baseplate, Kapton, Si sensor, and PCB. Because both the inner and outer boundaries of HGCAL detectors are circular, partial hexagon modules are proposed to fill the gap to make practical geometry close to the circular disc. In the case of Si-sensor only, a common mask is produced, which allowed us to produce different partial sensors from the same production of wafers by dicing the

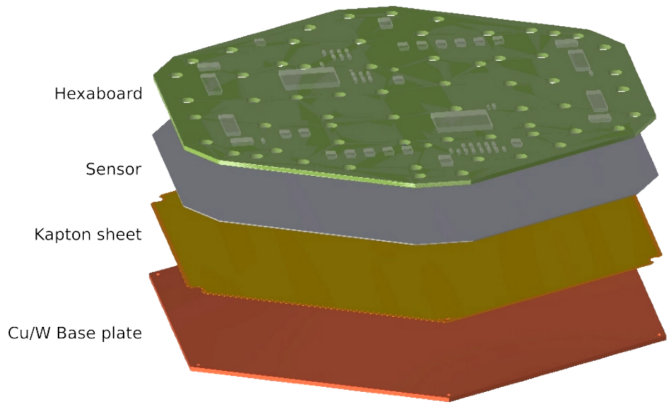


Figure A.6: A stacked view of CE-E silicon module.

wafer along with different appropriate positions.

A.3 HGCAL electronics powering scheme

A two-stage local supply scheme was proposed to power the HGCROC3 chips. The first stage is DC-DC, and the second stage is linear regulation (LDO). A block diagram of proposed powering scheme is shown in Figure A.7. In addition to the HGCROC3 chip,

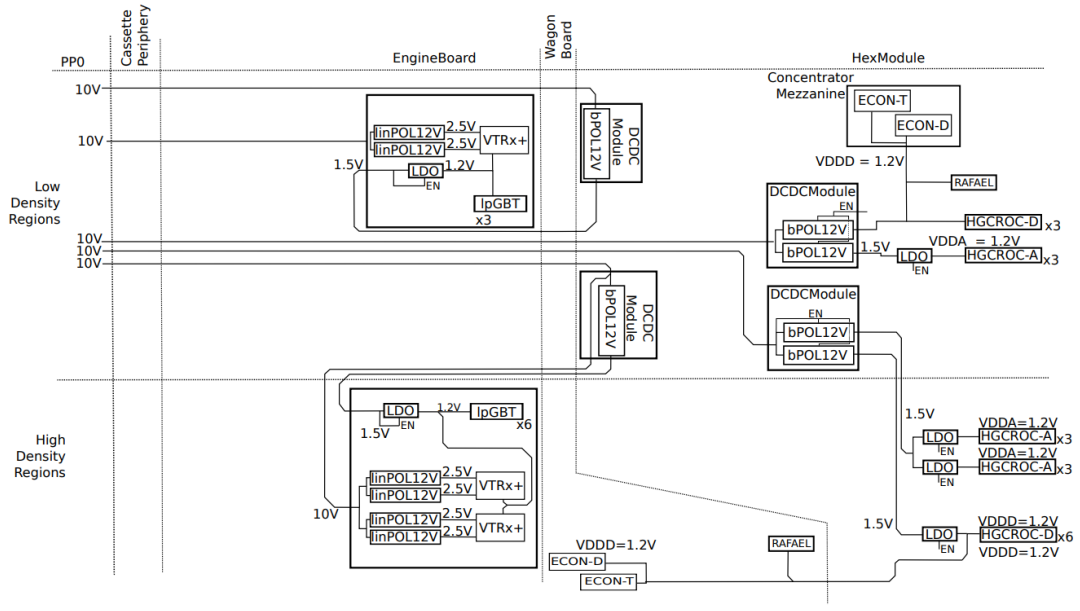


Figure A.7: Simplified HGCAL cassette powering scheme. SGC773000 will be used to power the HGCROC chips. For low density regions, LDO will be used for Analog power only. For High density region, LDO will be used for both Analog and digital power domains of HGCROC.

the LDO will also power the lpGBT chips on Engineboards. In the Hexmodule region and for high-density Hexa modules, the HGCROC3 powering in the HD region of the HGCAL will be powered totally by LDO, both for analog and digital domains. In the LD region of the HGCAL, the digital power will be supplied directly through DC-DC

converters, while LDO will supply the analog power domain of the front-end ASICs. The enable pins of the LDOs will be controlled by lpGBTs, and HGCROC3 chips could control the output voltage adjustment pins. The output voltage adjustment feature is intended to be used later in the project after years of operation. The primary purpose of this feature is to compensate for the LDO outputs deterioration by TID effects in the system.

In the EngineBoard region, both in the LD and HD regions of the system, lpGBTs will be powered by LDO chips. LDOs will be used in a self-enabled mode in this region and will always be "on" until the DC-DC module provides input power.

A.4 Introduction to SGC773000_CRN01 LDO

The SGC773000_CRN01 is a custom-designed LDO primarily for use in the HGCAL project. The chip design was subcontracted to a European-based company named as SiliconGate. The SGC773000_CRN01 is a low-dropout (LDO) high current, fast response, low quiescent current linear voltage regulator manufactured in CMOS 130 TSMC technology. RPHRIPOLY poly resistors and Enclosed MOSFETs helped the IP achieve low noise and high radiation robustness, respectively.

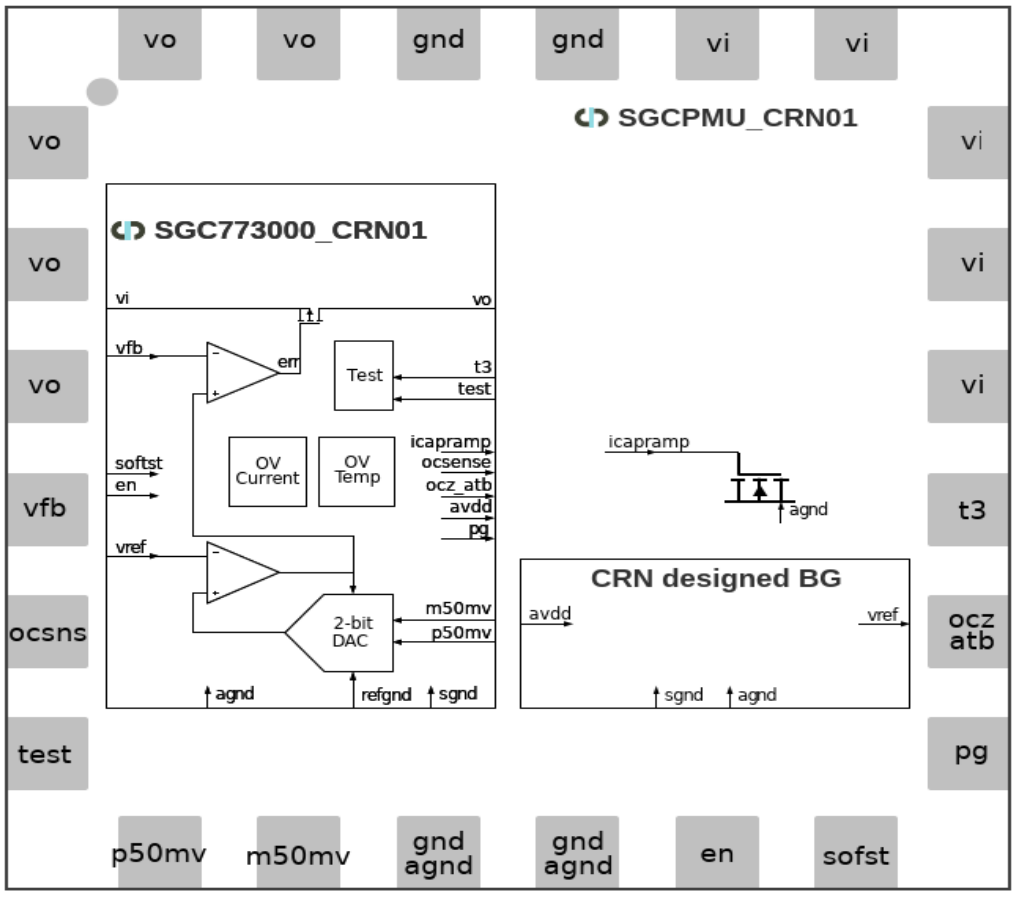


Figure A.8: SGC773000_CRN01 block diagram encapsulated in a 24 pin QFN package

The LDO uses proprietary multi-loop control techniques to achieve the excellent transient response and maintain low dropout and quiescent conditions. The SGC773000_-CRN01 includes error amplifiers, a PMOS power device, an internal programmable feed-

back resistor divider (2-bit DAC), an over-temperature detector, an overcurrent detector, and self-test capability as shown in Figure A.8. The output capacitor voltage goes through the external resistive divider and is fed back to an error amplifier through the "vfb" pin. The internal current feedback loop limits inrush currents during startup and protects the power device against over-current situations. The LDO shuts down when excess current is detected to protect the core from excessive power dissipation during a short circuit. The LDO also shuts down if the excess temperature is detected. After a shutdown, to start it, one needs to disable the LDO (en pin 'low') and enable it again (en pin 'high'). The LDO operation is controlled via the en pin. When disabled, the core is in power-down mode, and the output pin is pulled low via an internal 100Ω resistor. The SGC773000_CRN01 provides a Power Good (PG) flag with hysteresis. The PG comparator will return a 'good' signal only when the output voltage has reached 95% (rising) and will return a 'not good' signal when the output voltage falls below 90% of the regulated voltage. A summary of key specifications of the LDO is listed below:

- ☐ `Technology` : 130nm CMOS
- ☐ I_{max} : $3\ A$
- ☐ $V_{in_{max}}$: $2\ V$
- ☐ `Adjustable` V_{out} : $1.0 - 1.5V$
- ☐ `Max voltage dropout` V_o-V_{in} : $200\ mV$ @ I_{max}
- ☐ `Digital Adjust` : $\pm 50\ mV$ `steps`
- ☐ `Max. dissipation` : $500\ mW$
- ☐ `Stable with` $33\mu F$ `to` $62\mu F$ `ceramic output capacitors`

A.4.1 Typical LDO schematic & pinout table

A typical LDO application schematic is shown in figure A.9. An offset of plus/minus 50 mV can be added/subtracted from the output voltage, normally set via the feedback resistors network, by applying a digital code to the pins M50 and P50. All digital inputs to the LDO are driven between GND and VEXT. The maximum voltage on VEXT is 1.2V and should not be exceeded.

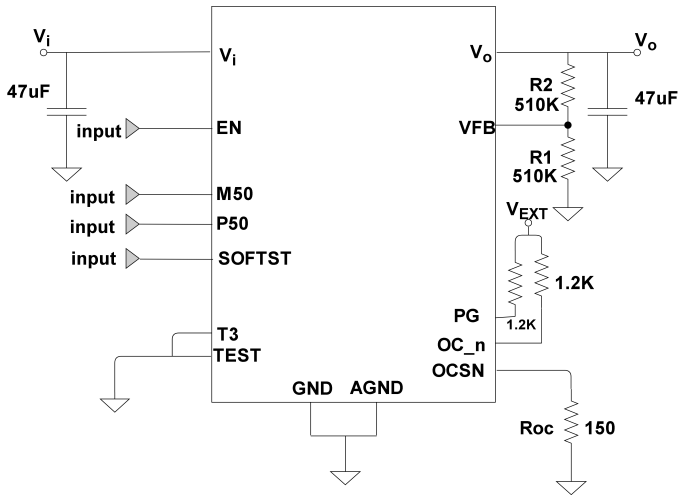


Figure A.9: Simplified schematic for LDO powering. $V_{EXT} = +1.2V$. V_i is 1.5 V and V_0 with $M_{50} = P_{50} = 0$ is 1.20 V.

The PG and OCZ are open-drain outputs pulled up with $1.2k\Omega$ resistors. A high PG signal indicates a regulated-output voltage condition. In contrast, a low OCn pin shows

an over-current or over-temperature state. The over-current limit is configured through the resistor Roc for a maximum of 5A current. Beyond this value, the LDO shuts down its output. A re-assert of Enable signal is required to restart the LDO.

A detailed pin list and pin functions are tabulated in the following table A.1.

PIN	TYPE	DIR	DESCRIPTION
V_O	Power	O	LDO regulated output.
VFB	Analog	I	LDO feedback sense.
OCSN	Analog	O	Over current sense input for the over current triggering value definition. Should connect to GND through a resistor defining the max. allowed current
TEST	Analog	I	Activates the LDO special test mode. Never used in user application. This pin must normally be grounded.
M50, P50	Digital	I	LDO 2-bit output voltage programming [M50,P50] / V_O [Volts] 10 / $V_O - 50$ mV 00 / V_O 01 / $V_O + 50$ mV 11 / $V_O + 100$ mV
GND_AGND	Power	I	Ground supply.
EN	Digital	I	LDO Enable pin active high. EN pin is also internally pulled up with a $47k$ resistor.
SOFTST	Digital	I	LDO soft start active high. If SOFTST is high then V_O will raise in about 12 ms.If SOFTST is low, V_O will raise in about 50 μs.
PG	Digital	O	Power good flag. When high indicates a well-regulated output voltage. This is an open drain output and can withstand 8mA.
OCZ	Digital	O	In normal mode, this is the overcurrent indicator. It is active low. This is an open-drain output and can sink 8 mA.
T3	Digital	I	Test and internal block characterization test control pin. Not used in operation, must be grounded.
V_I	Power	I	Unregulated positive supply.
GND	Power	I	Analog substrate ground supply.

Table A.1: LDO pinout table

A.4.2 Recommended Operating Conditions

The recommended operating conditions of LDO are depicted in the table A.2.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_i	Input Voltage	Full spec	1.20	-	2.0	V
V_{EXT}	Interface Voltage		-	1.20	-	V
V_o	Output Voltage	Fully validated	1.150	1.200	1.300	V
T_s	Startup time	No load, C_o, V_o : $typ.$, $softst$: 0 No load, C_o, V_o : $typ.$, $softst$: 1	- 10	0.05		ms
I_{V_O}	Output Current		0.001	-	3	A
OC_z	Over-current detection limit	Normal operation	-	5	-	A
OT_D	Over temperature detection limit		65	85	105	°C
V_{IH}	Digital Input High Level		80%	-	-	V_{EXT}
V_{IL}	Digital Input Low Level		-	-	20%	V_{EXT}
V_{OH}	Digital Output High Level		90%	-	-	V_{EXT}
V_{OL}	Digital Output Low Level			-	10%	V_{EXT}

Table A.2: Recommended operating conditions for the LDO operation

A.5 LDO Radiation campaign

A low noise uninterrupted supply is vital for the front-end ASIC to detect small, fast signals produced by incoming particles and measure their Time of Arrival (ToA). The LDO plays an essential role in achieving this task by post-filtering noisy input DC-DC supply. The operation of LDO under high radiation levels (see section A.2) need to be validated. The HGCAL environment will be a mixture of high-energy particle streams, which continuously deteriorate the performance of the electronics. So both aging effects and single-particle events are likely to occur during the operation of the device. A series of different radiation tests, including TID tests, SEU tets, neutron irradiation, have been planned to validate the radiation robustness of the LDO. The test setups and their outcomes are discussed in detail in the following sections.

A.5.1 LDO Neutron Irradiation

We irradiated the LDOs at IJS nuclear reactor, Ljubljana, Slovenia, in May 2021. Two fluence checkpoints were selected first 1×10^{16} $n.eq./cm^2$ and second up to 2×10^{16} $n.eq./cm^2$. Due to the relatively high fluence levels chosen for the LDO, the irradiation was performed in the so-called central channel (CC), where the highest neutron flux is available. The exposition times of 1500 and 3000 sec were used to achieve the desired checkpoints. During the neutron exposure, LDOs also received a small TID doses of gamma rays reaching up to TID of 13.6 and 27.2 Mrad for first and second checkpoints, respectively. Figure A.10 shows both the typical F19 and CC radiation channels which are normally used for small silicon devices irradiation.

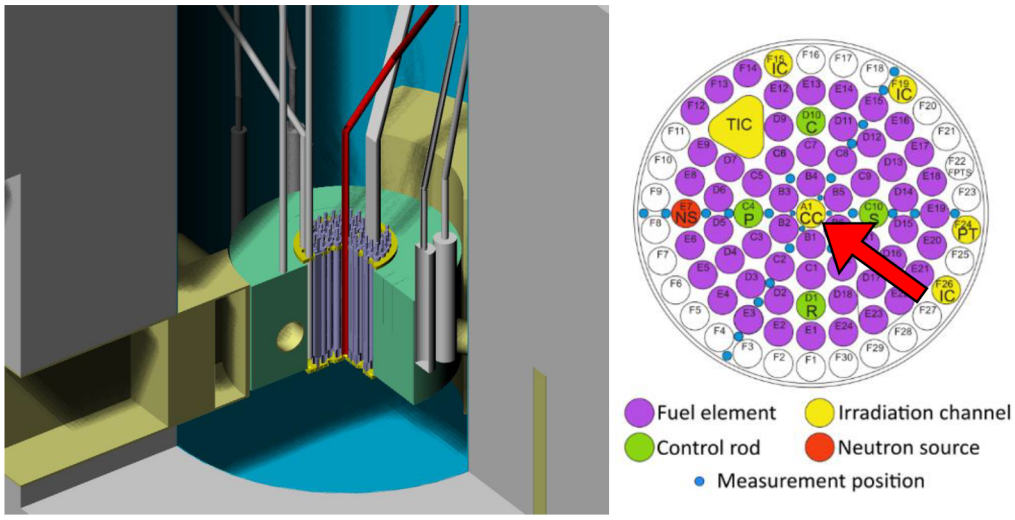


Figure A.10: LDO neutron irradiation central and F19 channels

Both F-19 and CC channels have the same dimensions. The constraints imposed on the maximum sizes of the samples were 2.5 cm diameter with the 12 cm height. The standard tubes at IJS are usually drilled at the top section and tied to the fishing line for easy handling (see Figure A.11).

Figure A.11: Real photograph of neutron irradiation. F19 channel is shown with red arrow. Three dies at 1×10^{16} $n.eq./cm^2$ and two dies at 2×10^{16} $n.eq./cm^2$ were irradiated. Due to high neutron dose requirement for LDOs, a similar central channel (CC) is used for LDO irradiation.

The measurements showed that after the neutron irradiation, LDO showed an average increase in the output voltage (Vout). An increase of 30 mV (2.5%) was recorded to the Vout for the LDOs which were irradiated to a less dose of 1×10^{16} $n.eq./cm^2$, while an average increase of 40 mV (3.3 %) was recorded to the Vout of LDOs which were irradiated to 2×10^{16} $n.eq./cm^2$. This deviation is well under acceptable limits of the LDO.

A.5.2 TID-only of LDO

We performed a TID test for the LDO to irradiate it up to 1-Grad TID. The LDO chips were irradiated in the CERN microelectronics X-ray irradiation facility, Obelix. The details about the X-ray machine are previously mentioned in Chapter 5. Figures A.12 and A.13 show LDO test setup and connectivity of the system. It includes Power supplies, multimeters, electronic loads, and a Linux computer for data storage.

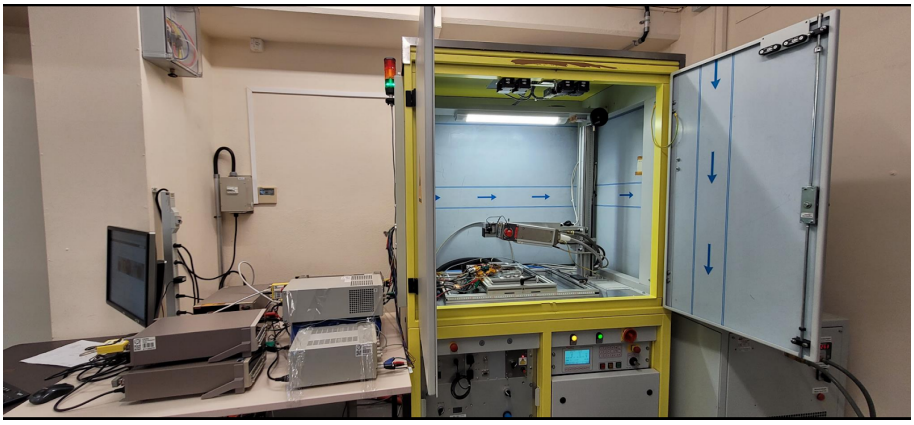


Figure A.12: LDO TID Irradiation facility at CERN

An input voltage of 1.6 V was applied to the LDO through a source meter. The enable, P50, and M50 inputs were controlled through PC software running python scripts. A 5V compatible DB-9 I/O connector was available in the source meter, connected to the LDO control inputs via a 1.2 V level translator. The PC indirectly controlled the LDO inputs via the source meter. At the output side of the LDO, a programmable DC load was used for varying different loads during the irradiation test. Three digital multimeters monitor the output voltage, PG, and OCZ status flags. A temperature sensor was also attached to monitor the chip temperature at the bottom side of LDO. All the equipment was connected through a shared ethernet network which was controlled by the main Linux computer. Since the test was running for eight days round the clock, a live web monitoring of test status and error conditions was devised using CERN cloud processing infrastructures. Live plots were accessible through a web browser hosted on CERN servers. It is essential to mention that data acquisition scripts were running independently from the data monitoring scripts. It was aiming to protect the primary TID system from any external interventions. The data monitoring script was only running after 30-second intervals.

The important test conditions and parameters are listed in Table A.3 below:

Figure A.14 shows the main acquisition flow chart for the TID test. A complete test loop takes around 32 minutes. The loop started with a high load of 3A and grabbed 300 samples of Vout and status flags with the sampling frequency of 3 Hz. Then the load was switched to a low value of 1.5A for the next 15 minutes, and outputs were recorded. After that, short-duration measurements of enable disable functionality, output voltage adjustment, and overload protection functionalities were tested, and LDO response was recorded on the computer. This loop was running for the actual test until desired TID was achieved.

The LDO was placed inside the shielded box during the test, and a laser cross-hair was used to align it with the X-ray beam. A pre-rad data was taken without beam for comparison purposes in the same conditions to exclude the environmental effects such as wire resistance and noise coupling due to the proximity of all power and signal lines in the feed-through channel. Once data taking was started, the device was never switched

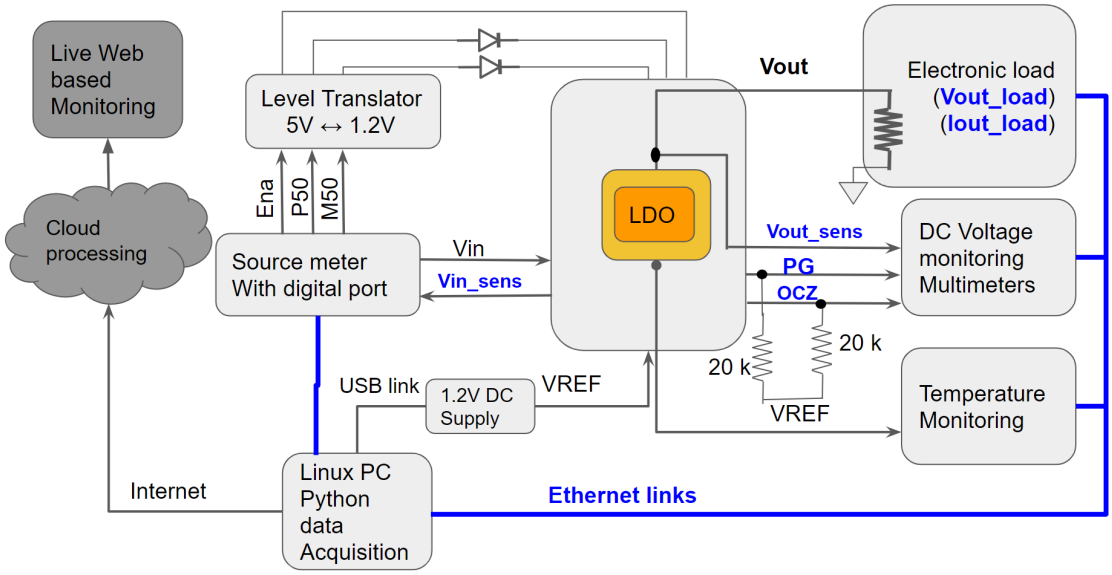


Figure A.13: LDO TID setup connection diagram

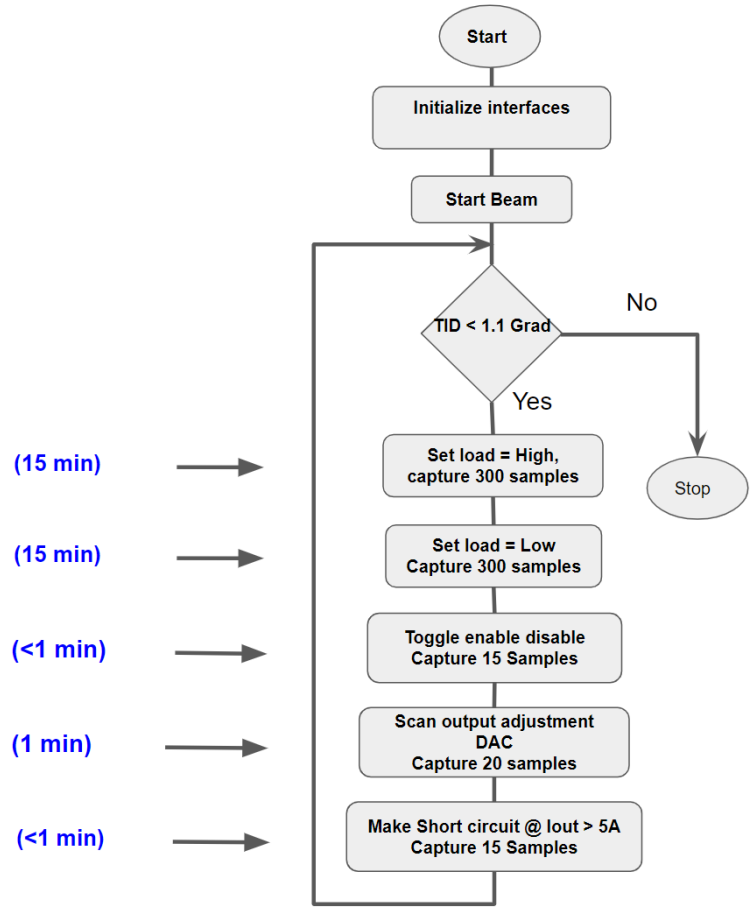


Figure A.14: LDO TID test loop. It was repeated round the clock for full test started from pre-rad conditions to short annealing phase. One complete test loop takes around 33 minutes.

off. Firstly, the beam turned on at a low rate of 388 krad/hr. The purpose of starting with

Parameter	Operating conditions
Vin	1.6V (with 4-wire sense correction)
Sampling rate	∼3Hz
High load	0.35 Ω (∼ 3.4A)
Low load	0.6 Ω (∼ 2A)
Over load	0.18 Ω(>5A)
Load mode	Constant Resistance
Chip Temperature	-16.5 to -19°C
Thermal chuck temp	-27.5 °C

Table A.3: Parameters used during TID test of LDO

a low rate was that devices manufactured in 130nm had shown sensitivity towards low dose rates up to 1 Mrad. So a total of 4.5 Mrad was achieved at a low dose rate in 12 hrs. Later on, the machine was switched to a higher rate of 9.7 Mrad/hr for the next five days. All the outputs, including PG, OC, and output voltage of LDO, were recorded with a sample rate of ∼ 3s. The Vout variation versus time and TID is shown in Figures A.15 and A.16.

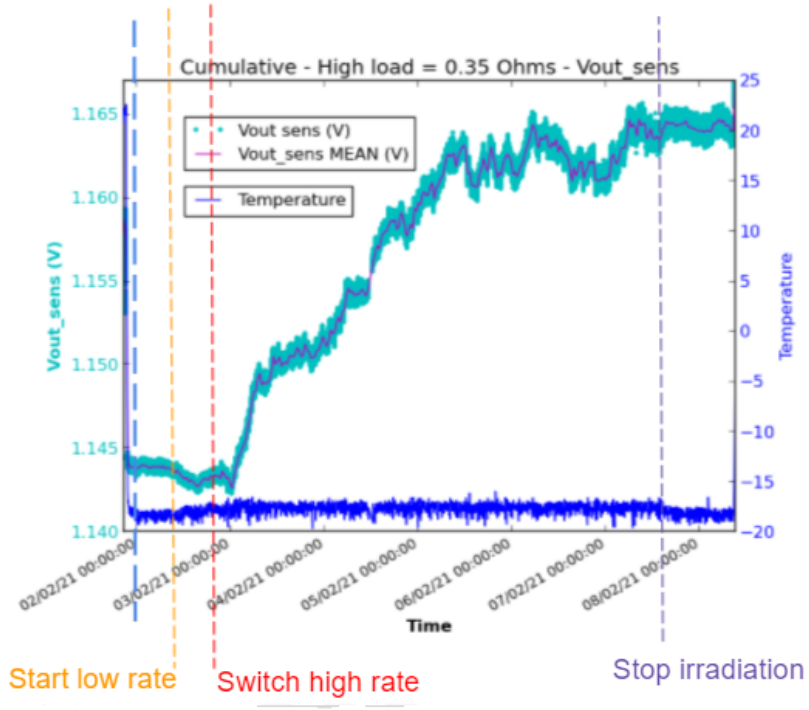


Figure A.15: Vout plot of the LDO versus time at high load conditions. the plot shows data accumumuated over eight days of monitoring. The bottom blue plot showing die temperature measured at metal ground pad underneath the chip.

A stable Vout (1.14 V) was recorded until a slow dose rate. Then a slightly fast rise was started with a high dose for the next three days, saturating during the last two days of irradiation. The overall Vout rise was not significant, and a 20 mV mean increase was observed after 1 Grad of TID. This indicates merely a 2% increase in the Vout after 1 Grad of TID. It is essential to mention here that a total of four 50 mV Vout adjustment steps are provided in the LDO to compensate for radiation damage effects. It leads to the fact

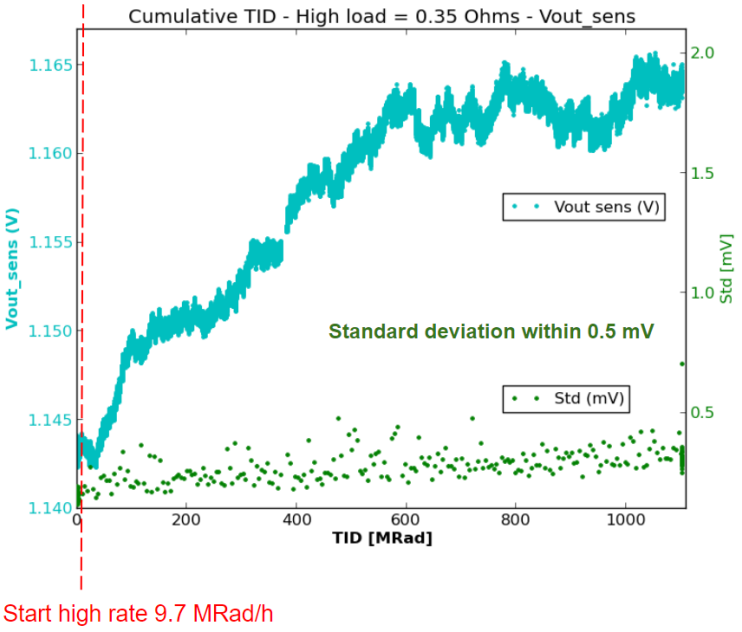


Figure A.16: Vout plot of the LDO versus TID, showing mainly high dose effect

that if we start with [M50, P50] = 01 in the CMS, which corresponds to 1.25 V Vout at no-load conditions, then after 10 HL-LHC years of operation, a maximum of one step down adjustment could be required to keep Vout constant.

In addition to output voltage monitoring, enable-disable functionality, short circuit protection, and output voltage adjustment functionalities were monitored. All these functionalities have been working as usual during and after the test. The output voltage variation after full TID is tabulated in the table A.4.

Code	Vout Pre rad (V)	Vout post 1-Grad (V)	Difference (mV) (post -pre)	Slope (μV/Mrad)
0	1.14052	1.16404	23.52	21.4
1	1.18920	1.21063	21.43	20.39
2	1.23841	1.25925	20.84	19.66
3	1.28711	1.30834	21.23	20.56

Table A.4: LDO Vout (V) with different {P50, M50 } combinations.

All the combinations produced similar variation, and the average drift in the output voltage was 20 mV after 1-Grad of TID. Figure A.17 also shows output voltage plots with different input codes.

It shows that P50, M50 path is robust against TID effects, and a common drift for all combinations shows that the bandgap variation is responsible for the observed drift. This drift of output voltage was well under specifications and can be compensated later in the experiment after several years of LDO operation if needed.

A.5.3 TID of neutron-irradiated LDOs

A TID test of neutron-exposed LDOs (discussed in section A.5.1) was done in the same CERN X-ray facility in which we tested normal LDOs (discussed in section A.5.2). A con-

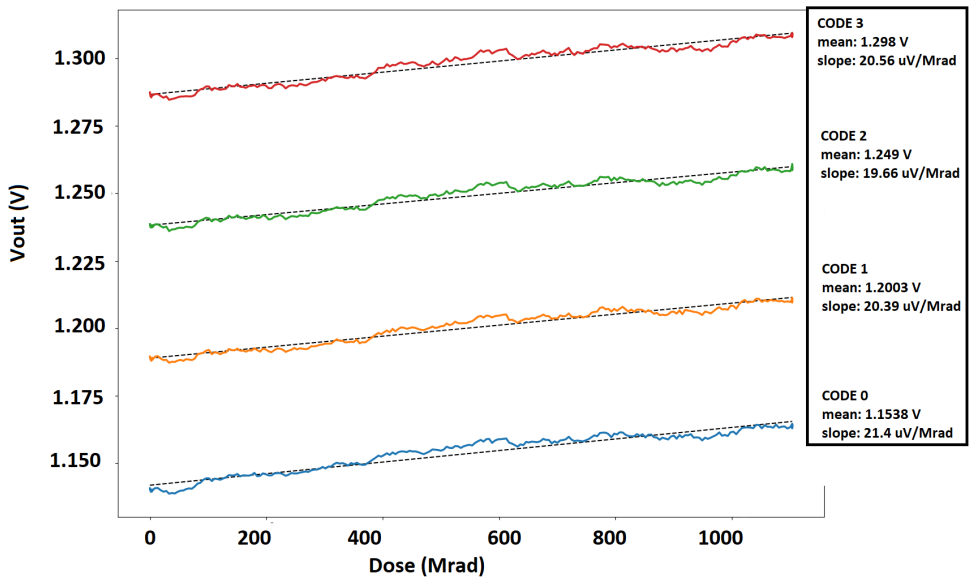
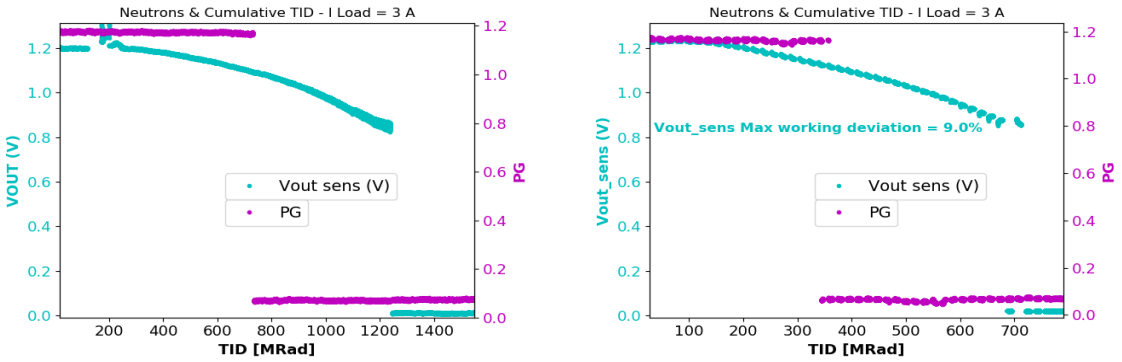


Figure A.17: Vout plots for all M50,P50 codes. Plots show similar vout variation for all the chosen input combinations of codes.

tinuous decrease in the output voltage at maximum load conditions (3A output current) was recorded. Figure A.18 shows a comparison of TID effect on LDO output voltage of two neutron-exposed LDOs (exposed at two different checkpoints). The LDO exposed



(a) Vout drop versus TID for first neutron irradiated LDO sample (checkpoint-1)

(b) Vout drop versus TID for second neutron irradiated LDO sample (checkpoint-2)

Figure A.18: LDO Vout variation of pre-exposed with neutron fluence checkpoint-1 & 2 comparison

up to checkpoint-1 (shown in Figure A.18a) asserted PG after 737 Mrad of TID. Although PG was asserted to indicate 'no good' condition, yet LDO continued to provide maximum current of 3 A until 1300 Mrad of TID with a gradual Vout drop, after which LDO stopped working completely. Similarly, the LDO exposed up to checkpoint-2 (shown in Figure A.18b) asserted PG after 340 Mrad of TID. Although PG was asserted to indicate 'no good' condition, yet LDO continued to provide maximum current of 3 A until ~700 Mrad of TID with a gradual drop in Vout, after which LDO stopped working completely.

Table A.5 shows a comparison of LDO performance degradation with different TID and neutron irradiation campaigns.

The TID-only test showed radiation tolerance up to 1.1 Grad; afterward, we stopped

the test due to time constraints. The two high fluence neutron-exposed LDOs named P2_1 and P2_2 showed radiation tolerances up to a 340 Mrad and 370 Mrad respectively.

Test Type	Fluence reached (neq.cm-2)	Dose reached (Mrad)	Measured Vout (@ 3A load)	Change in Vout
Pre-rad LDO (no radiation)	-	-	1.20 V	0
TID Only	-	>1100	1.225 V	+25 mV (2%)
Neutron Check point-1	1 x 10^{16}	13.6	1.23 V	+30 mV (2.5%)
Neutron Check point-2	2 x 10^{16}	27.2	1.24 V	+40 mV (3.3%)
Neutron (Check point 1) + TID	1 x 10^{16}	>737	1.12 V	-120 mV (10%)
Neutron (Check point 2) + TID	2 x 10^{16}	> 340	1.12 V	- 120 mV (9.6%)

Table A.5: LDO TID and neutron tests summary

A.5.4 LDO SEU test

An SEU test was planned to evaluate the device operation under heavy ion beams of different stopping powers. Figure A.19 shows a simplified block diagram for the LDO SEU test setup explaining the test principle.

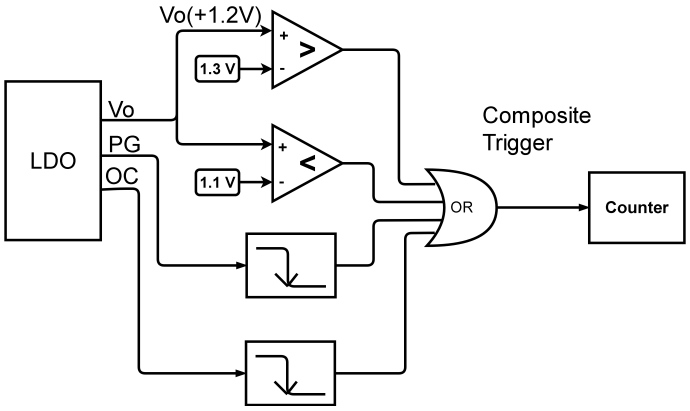


Figure A.19: Simplified LDO SEU test principal

The nominal output of LDO is +1.2 V with $M_{50}, P_{50} = 00$. The PG active low indicates Power malfunction, and OC active low indicates over current/ temperature condition. A composite trigger was generated if any of the following four conditions occured:

1. V_o crosses the upper threshold of 1.3 V
2. V_o crosses the lower threshold of 1.1 V
3. A falling edge of PG signal
4. A falling edge of OC signal

The composite signal triggered an oscilloscope, and waveforms were recorded. The total number of trigger events were fed to CPLD for counting purpose.

Figures A.20 and A.21 show the connection diagram and picture of the SEU test setup used in Louvain La Neuve. LDO was wire bonded on a test board and mounted on a metal fixture within the vacuum chamber. High current banana and DB-25 cables were used for the power and control signals routing, respectively. Two sealed feed-throughs were used, one for DB-25 and the other for banana cables. An interface card was placed outside the vacuum chamber, which hosts an analog comparator circuit for over and Undervoltage condition generations. The interface card also routed all the signals to the oscilloscope for live observations and trigger purposes. All the four signals shown in Figure A.19 are injected into the CPLD board for a composite trigger generation. The CPLD card sends back the composite signal to the interface card, then routes it to a LEMO connector. For simplicity, the oscilloscope was connected only to the LEMO connectors of the interface card. The CPLD card was also used to count the composite trigger signal events and individual PG, OC, and voltage transient events. The trigger counting data and waveforms are finally transferred to a Linux control computer.

A.5.4.1 SEU observations & cross-sections

Several ion species were used to irradiate the chip, and LDO outputs were recorded. We got some surprises, and a large number of transients were observed during heavy-ion beam irradiation. These were later categorized into two kinds of transients based on

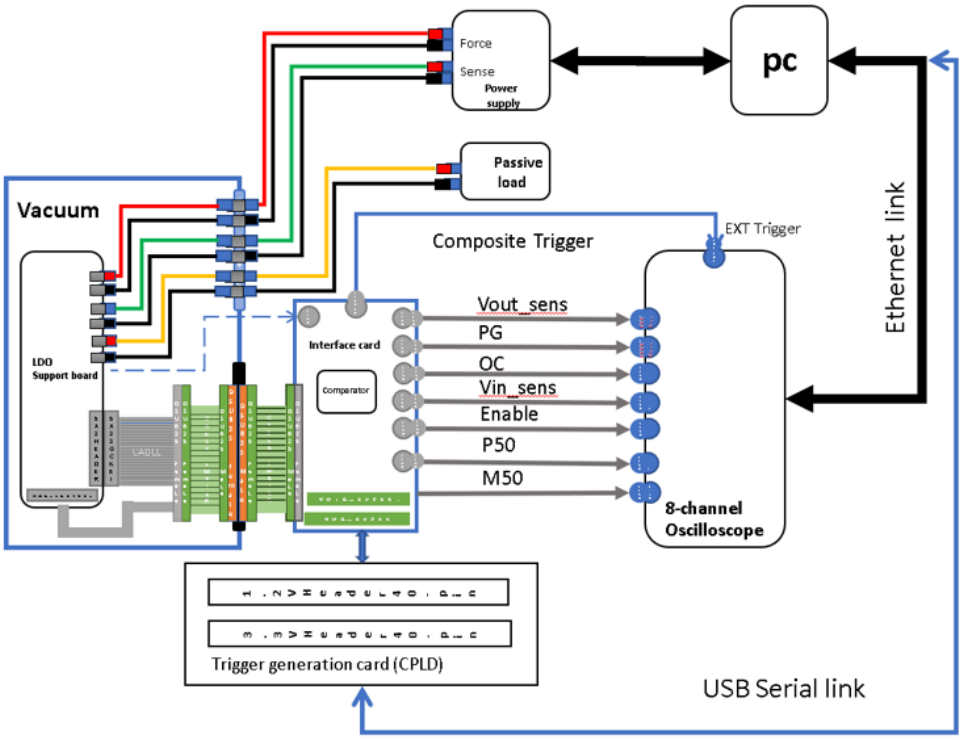


Figure A.20: SEU test setup at Louvain-La-Neuve Cyclotron HIF facility

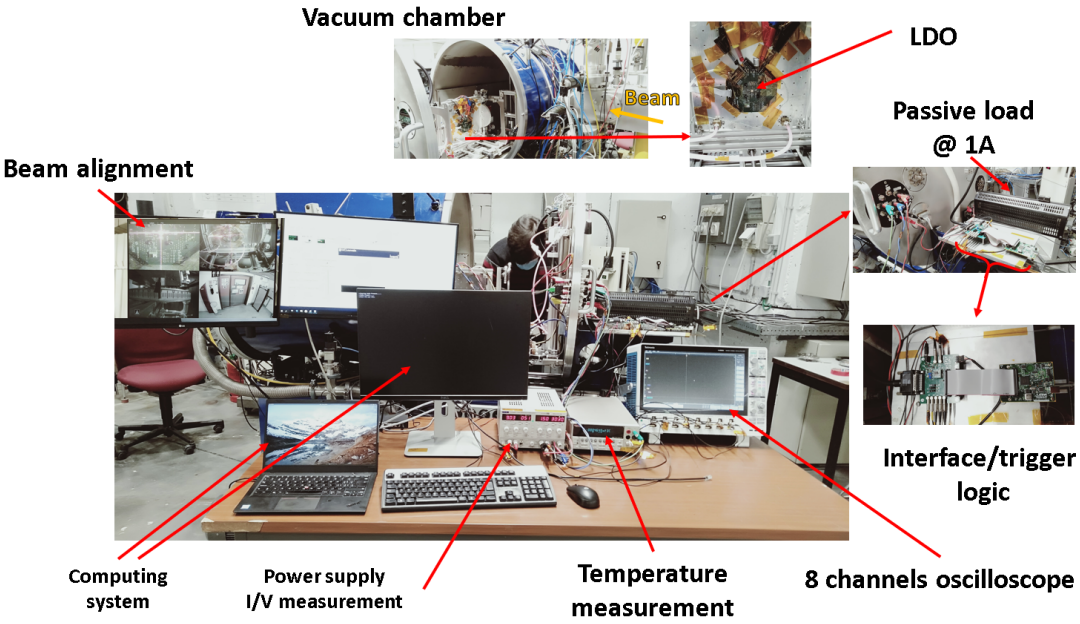


Figure A.21: SEU test setup at Louvain-La-Neuve Cyclotron HIF facility

the wave shape, timing, and polarity of the Vout signal. The first positive going faster transients were observed with a relatively higher frequency of occurrence as shown in Figure A.22. These transients were fast occurring with a maximum of 40μs duration and positive amplitudes up to 150 mV. Secondly, Table A.6 shows that with higher LET starting from "Cr," a large negative transient seems to appear at the Vout with a relatively low probability of occurrence. An oscilloscope snapshot of a large transient is shown in

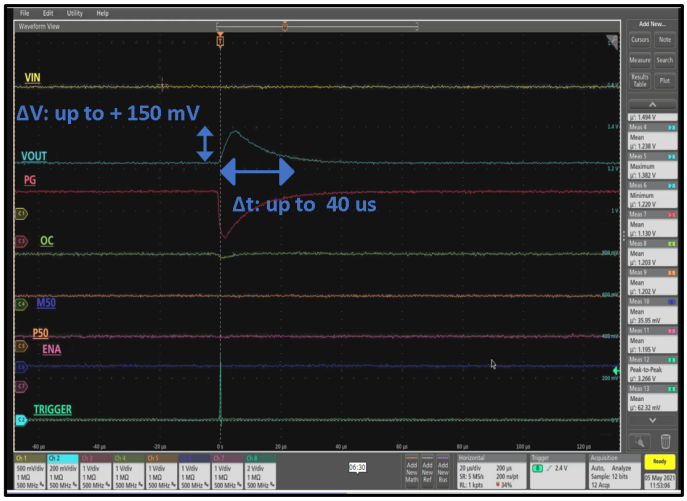


Figure A.22: Small transients observed on Vout signal. The frequency of small transients was higher.

Figure A.23.

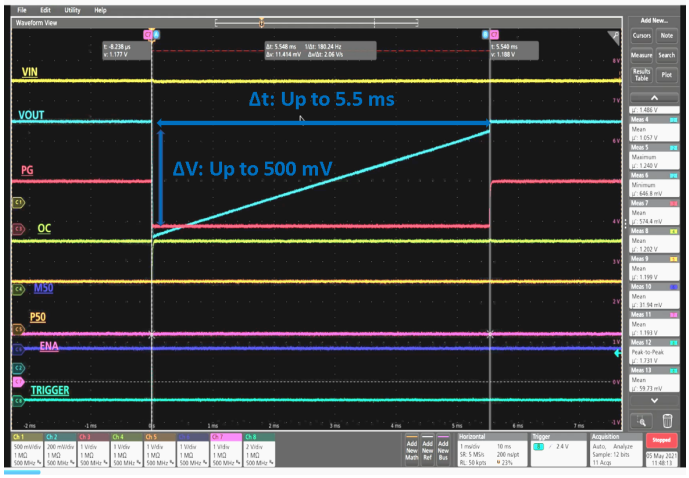


Figure A.23: Large and wide transients observed on Vout signal. The frequency of large transients was low compared to small transients.

This transient had a unique shape and negative going amplitude shift was up to 500 mV with the 5.5 ms time duration.

Ion	LET effective. $[MeV/(mg/cm^2)]$	Tilt θ°	Flux ions/(cm2.s)	Total Fluence ions/(cm2)	Elapsed time (sec)	Total transients count	Long transients count	Short transients count
Al	5.7	0	15201	30093272	3729	0	0	0
Al	7.44	40	12059	27036968	1791	0	0	0
Ar	9.9	0	14990	30111776	2003	193	0	193
Cr	16.1	0	15436	30082777	1943	412	4	408
Ni	20.4	0	14740	23472410	1575	417	7	410
Kr	32.4	0	15056	23773256	1574	735	197	538
Rh	46.1	0	15838	13604382	853	515	133	382
Xe	62.5	0	15179	13584771	889	548	152	396

Table A.6: SEU ions and transient counts

The HL-LHC cross-section estimate was performed using the same method described

in chapter 5 for VFAT3 synchronization lost cross-section estimates. As a reminder, a block diagram showing all the steps done for LDO HL-LHC estimates is shown in Figure A.24.

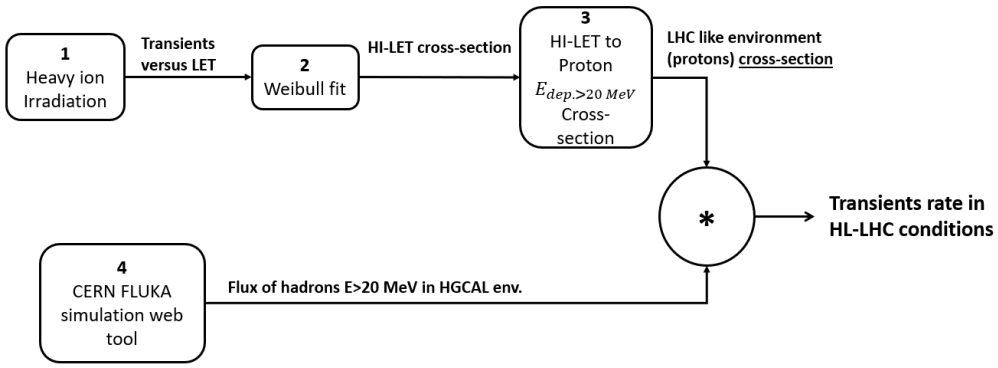
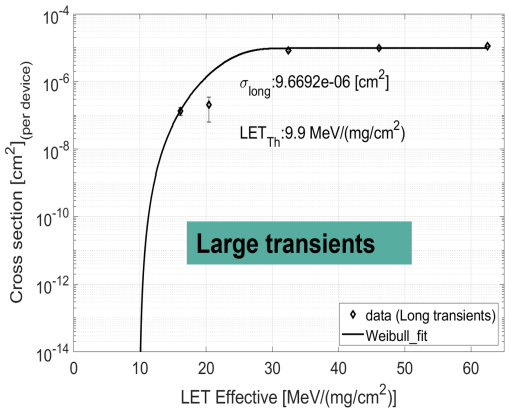
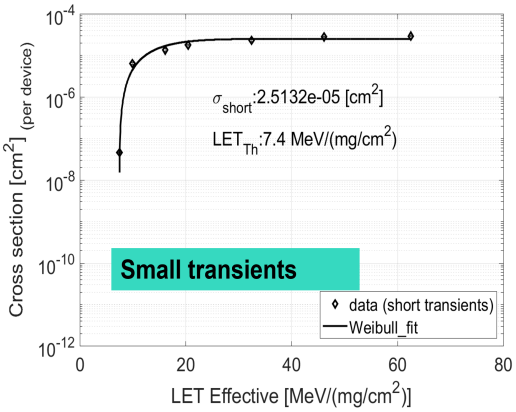


Figure A.24: LDO HL-LHC cross-section calculation steps as already explained in Chapter 5

Using the heavy ion irradiation data from table A.6 and Weibull fit function as used in Chapter 5 section 5.7.3, the HI-LET cross-section for small and large transients were calculated separately. Figure A.25 shows HI-LET cross-section for small and large transients observed on the output voltage signal of LDO. For large transients, the value of parameter threshold LET for upset was chosen between the last LET for which no error was detected and the first one for which errors were observed, which was between 9.9 and 16.1. This was indeed a threshold below which the energy was insufficient to trigger the event. The LET threshold was set to 9.9, and we also need to add a limit cross-sections for LET below 16. The limit cross-section was the one obtained, setting the number of errors to 1 (rather than the observed 0) and dividing this number by the integrated flux to obtain the cross-section shown in Figure A.25a. With the large transient Weibull fit, we



(a) Large transients HI-LET cross-section



(b) Small transients HI-LET cross-section

Figure A.25: HI-LET cross-sections for small and large transients observed during SEU irradiation with various ion beams. These plots are generated by using data from table A.6.

calculated a cross-section of $\mathbf{5 \times 10^{-15} cm^2}$ in the HGCAL-like environment of the LHC by using the computational method [96].

Similarly, for the smaller type of rising transients, the LET threshold was set to 7.4 and adjusted the other parameters were to fit the curve shown in Figure A.25b. In this case, the first point at 7.4 was the limit cross-section we estimated from the data(table A.6). (about 200 transients at a LET of 9.9, and none at 7.4, the limit cross-section at 7.4 was 200 times smaller than cross-section at 9.9). Using the parameters of this fit, we estimated a cross-section of about $\mathbf{3 \times 10^{-12} cm^2}$ in an HGCAL-like environment. We then multiplied these HL-LHC cross-sections by the flux of hadrons above 20MeV in an HGCAL radiation environment to estimate an error rate per chip.

Using the phase-2 HGCAL geometry defined in the TDR [112], the FLUKA spectrum for the flux of hadrons $> 20\ MeV$ is shown in Figure A.26

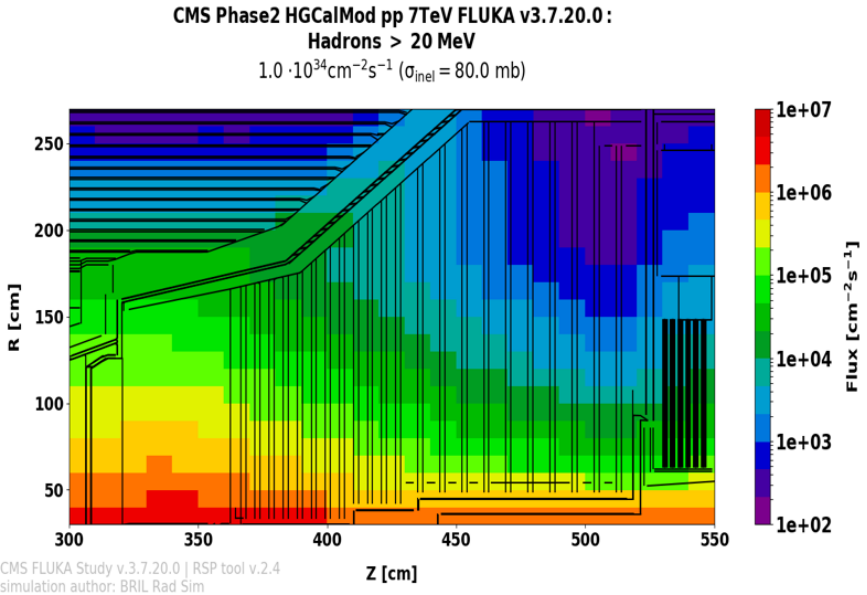


Figure A.26: Hadron (p > 20 MeV) flux, calculated by FLUKA Webtool with the Phase-2 HGCAL geometry.

The expected mean hadron flux is 3.5×10^6 particles cm^{-2} s^{-1} In HGCAL, the LD and HD regions will receive different levels of particle rates. The critical is the HD region. The rates of larger and smaller transients in HGCAL environment can be computed by multiplying HL-LHC cross-sections computed by computaional method and the mean flux in the HGCAL region, so we can write:

$$Rate_{large\ transients} = 1.75 \times 10^{-8} \quad \text{transients} \quad \text{(per LDO)} \tag{A.1}$$

$$Rate_{small\ transients} = 1.05 \times 10^{-5} \quad \text{transients} \quad \text{(per LDO)} \tag{A.2}$$

Expanding these transient rates over full HD region consisting of 16,776 LDOs, we can write:

$$Rate_{large\ transients} = 1 \text{ transient per hour} \quad \text{(HD region)} \tag{A.3}$$

$$Rate_{small\ transients} = 10 \text{ transients per minute} \quad \text{(HD region)} \tag{A.4}$$

The rate of smaller transients was significantly high compared to large transients. However, the smaller transients can be ignored as these will not impact the operation of the electronics, and transients can be minimized by increasing the LDO output capacitance. The main concern for the experiment is the large transient with the frequency of 1 tran-

sient per hour per HD region. This transient rate does not look significant and can be compensated, but keeping in mind the importance and role of LDOs in the experiment, even the small frequency of this large transient is not acceptable. Next, a post-SEU debugging campaign was launched to locate and mitigate these large transients.

A.6 LDO post SEU debugging

The large transients observed during the SEU test were a concern for the device operation in the CMS HGCAL environment. A thorough debugging of the source of transients was required to mitigate the problem completely. As a first step toward debugging, several fast digital pulses were injected to the enabling, P_{50},M_{50} and Test inputs of the LDO. The laboratory experiments highlighted the responsible circuit for large transients. This marking of the sensitive path was used further to investigate the problematic nodes in the device simulations. We will discuss in detail the laboratory experiments and simulation findings in the following subsections.

A.6.1 Laboratory regeneration of SEU signals

The idea was to reproduce SEU-like transients in the laboratory by injecting external pulses at various inputs of the LDO. The purpose was to find sensitive nodes in the LDO. The following three different possible pulse injection experiments were devised to initiate sensitive nodes in the LDO circuit:

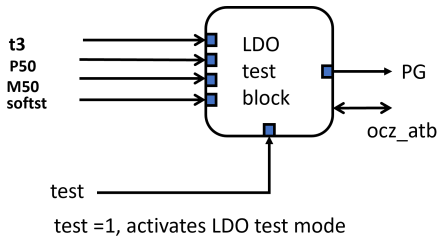
1. High to low pulses were injected into the enable pin.
2. $1 \rightarrow 0$ and $0 \rightarrow 1$ pulses were injected in the P50, M50 inputs
3. Low to high pulses were injected to the test pin of the LDO.

Firstly, short-duration high to low pulses were injected to the enable pin, which initiated the LDO re-initialization sequence. The LDO showed a similar waveform similar to SEU larger transients. It leads to the fact that the source of the larger transient is somewhere in the enable-disable signal chain of the LDO internal circuit. The

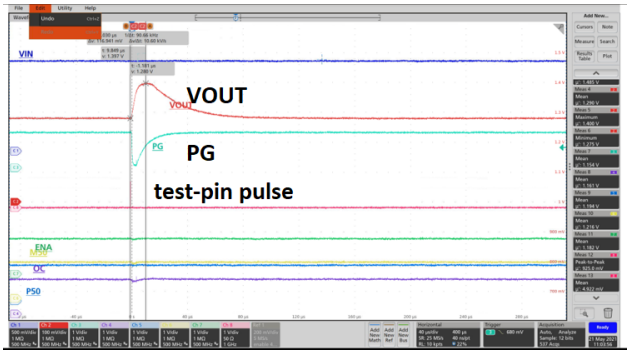
In the second experiment, we injected various combinations of P50, M50 short-duration pulses. The LDO performed typically, Vout showed expected response, and PG and OC flags were usual. This LDO response excludes the possibility of involvement of P50, M50 path in the transients generation, which were observed during the SEU test.

Lastly, low to high short pulses were injected into the test pin of the LDO. To facilitate the production and design debugging, LDO incorporates a test circuit which could be initiated by asserting the test pin as high. The fast switching of the test pin showed transient behavior not precisely similar to what was observed as short transients. However, it indicated that the possibility of involvement of test circuit in the shorter transients. This could be easily corrected by increasing/or adding the capacitance to the sensitive nodes of the built-in test-circuit path. Adding extra capacitance will reduce the sensitivity of switching the LDO state from normal to test mode.

In test mode, a 4-bit bus is used to apply 15 different test vectors to monitor different vital voltages of the LDO circuit, such as bandgap reference. PG is used as digital comparator output, and OCZ is used as analog input and output. During test mode in specific tests, OCZ is used to inject reference DC input voltage to compare some internal nodes, and PG becomes an output of the comparator. This is an indirect method to measure LDO internal voltages, helpful to remove measurement errors. PG and OC are



(a) LDO builtin test circuit pin diagram.



(b) A short pulse is applied to test pin of the LDO and Vout and PG are recorded.

Figure A.27: LDO test block diagram.

multiplexed pins used for the test circuit outputs. A 4-bit bus is used to apply 15 different test vectors to monitor different internal voltages of the LDO circuit, such as bandgap reference.

The transients observed showed the response with a maximum of 80 μs pulse width. The output transients have smoother peaks compared to SEU short transients. The direct correlation was not established, but the involvement of the test path could not be ignored. Simulations propose the addition of capacitance at sensitive nodes.

A.6.2 SEU simulation of LDO schematic

The SEU test findings and laboratory signal injection experiments were used as starting seeds for LDO simulations. A summary of SEU findings and laboratory tests done at CERN are:

- 1st issue:
  - V_O output voltage drops significantly: up to ~500mV
  - PG goes low and stays low until the output voltage recovers
  - OCZ goes low
  - V_O takes a long time to recover: ~ 5.5ms but, it is dependent on the V_o voltage drop
- 2nd issue:
  - V_O output voltage has an overshoot up to 150 mV
  - After the overshoot, the V_O goes back to its previous voltage level in about 40 us
  - PG goes low and quickly rises back to high
- 3rd issue:
  - Pulse injection in TEST pin causes PG to change state and some V_O overshoot

A typical SEU is translated to a triangular-shaped current pulse having 50ps rise time, 50ps fall time with an mA peak current of LET/10 as shown in Figure A.28.

From Louvain SEU data, the highest ion beam LET used was 62.5 $MeV/(mg/cm^2)$, which means the peak current should be around 6.25 mA. The chosen rise time was 50

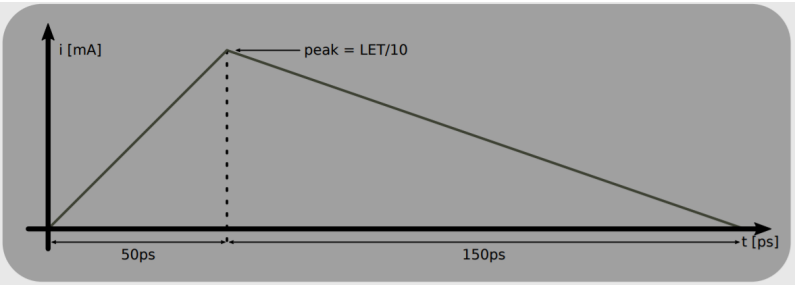


Figure A.28: Large and wide transients observed on Vout signal. The frequency of large transients was low compared to small transients.

ps, and the fall time was 150 ps. The choice of a larger fall time of 150 ps was made instead of 50 ps since later is the most conservative one. Every net tested was submitted to positive and negative SEU pulses. Positive and negative SE on a net were spaced 50μs apart. The device simulations also found the issue on the enable-disable path of the LDO circuit. During the first attempt to understand the issue, four critical nets were marked as the root cause that could cause a similar behavior as shown in Figure A.29.

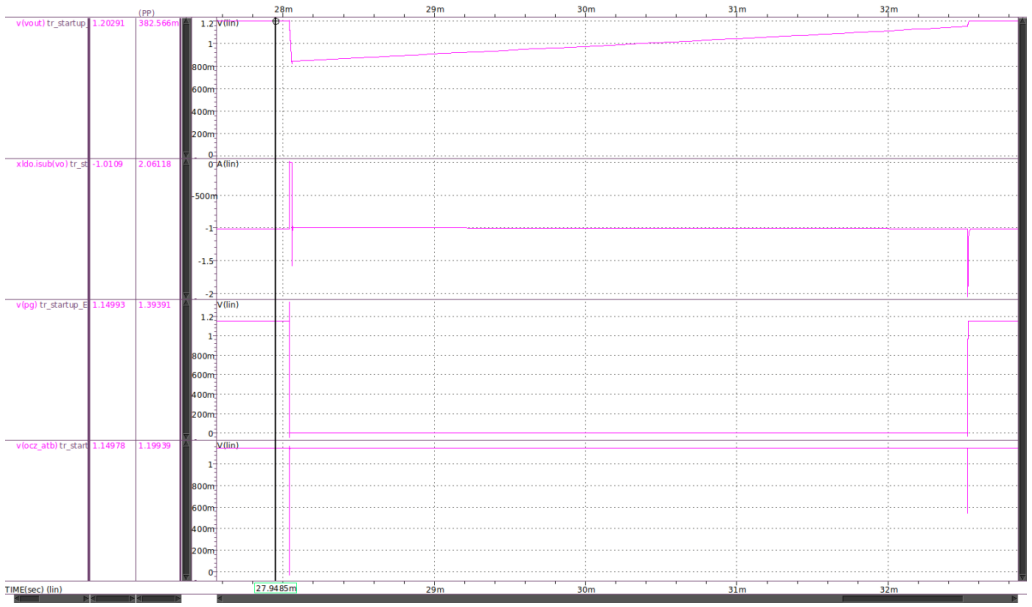


Figure A.29: The image above shows the same issue in simulation after a net was subjected to a SE with typical energy.

Although the output voltage V_O drop was observed in the simulation, it was not as much as in laboratory measurements. This dropout in the V_O depends not only on the SE itself but also on the discharge state of an internal node, which is connected to the capacitance responsible for the 10 ms output voltage rise at startup. Therefore, the drop in V_O will change depending on the PVT conditions, which is difficult to achieve in simulation accurately.

However, all initial four nets needed more than 10 times of energy than a typical SEU. This amount of energy is unlikely to happen. With a deeper probing of the enable path, five additional critical nets were located. One of them only needed a typical SE energy to trigger the issue. Therefore, this was selected as the root cause of the issue; the other four need at least five times more energy. Figure A.30 shows Vout dropping when a typical SEU energy equivalent waveform is injected at internal circuit net "vrefokzvcasn."

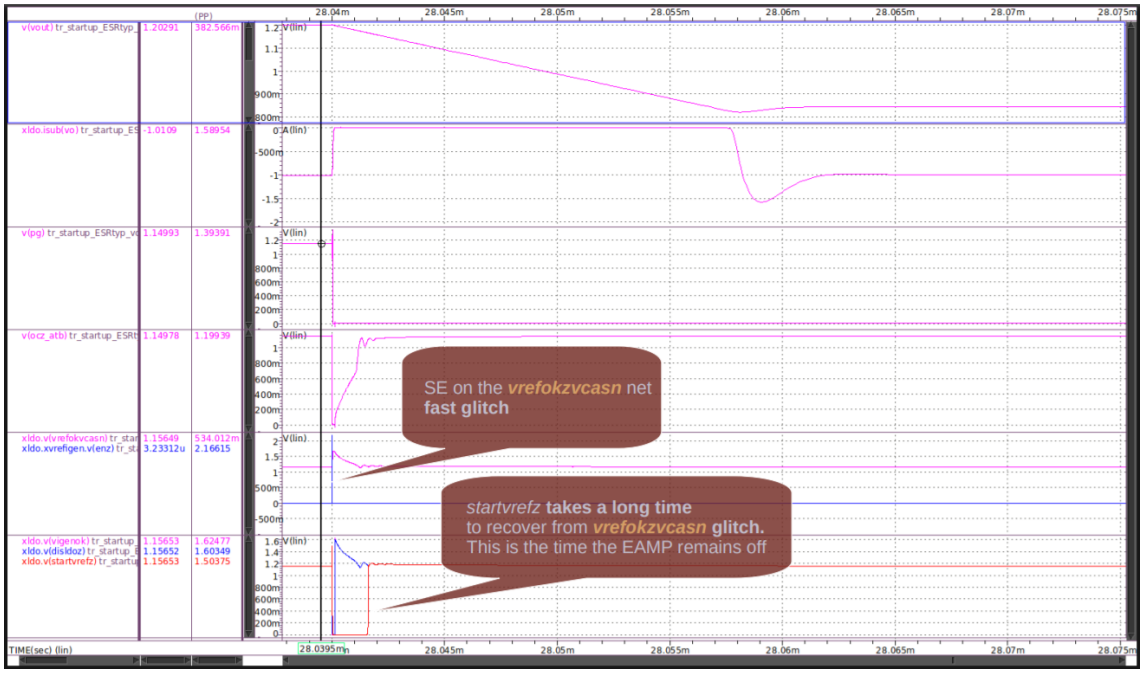


Figure A.30: The image above shows the simulation when the net vrefokzvcasn (xldo.xvrefigen.v(enz)) suffers a SE

The signal "vrefokzvcasn" goes high due to a SE but quickly recovers since it is the output of an inverter. Two other internal signals, "vigenok" and "disldoz" change their status briefly. However, "startvrefz," the enable for the EAMP and PGCOMP, takes a long time to recover. PG stays low since V_O is already below 90% of the programmed value when "startvrefz" goes high again. V_O continues to drop since the output load is still 1A and the SGC773000 stopped supplying current.

A.6.3 LDO laser testing

Although sensitive nodes of the LDO have been identified with high confidence yet, we planned to do a high-power laser scan of the LDO to locate individual sensitive nodes with high precision. A laser test energizes individual nodes of the chip with micro-beam entering from the bottom of the chip. Unlike the SEU test, where the entire chip is exposed to a beam size of 25 mm, the laser beam diameter is a few microns to probe the individual sensitive nodes with more spatial precision. Moreover, this test will eliminate the possibility of any other sensitive node in the system which the SEU test and the simulations might not identify. The entire chip view of the LDO version 1v0 is shown in Figure A.31.

For simplicity, only the two top layers are visible (layers AP and Metal 7). On the right side of LDO, we have the startup capacitor; the bottom has a bandgap (BG), the LDO core logic sits above BG. The LDO is composed of an analog/control section and a power device. The area of interest (AOI) for Laser testing is the analog/control section. The AOI has dimensions of ~610 µm × 385 µm. The pad arrangement helps quickly identify the top and bottom of the chip. The left and right of the chip can be identified by the different structures such as a capacitor, AOI, and bandgap.

A PULSCAN laser system provides the instrumentation for failure analysis of semiconductor devices. It is helpful in quickly debugging the chip design, which might take a lot of time and effort. The defect localization accuracy is high, which improves the final yield of the system. Figures A.32 shows a PULSCAN system that will be used for LDO

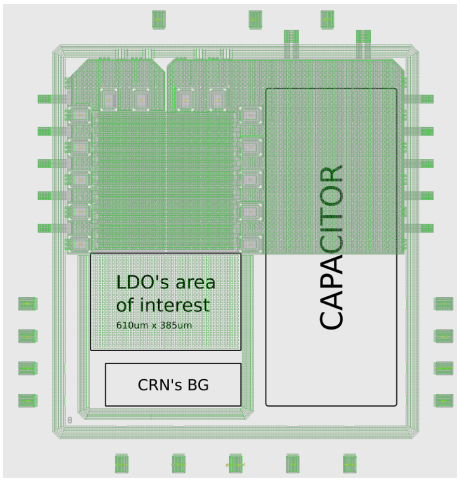


Figure A.31: Full chip view of the LDO

debugging.

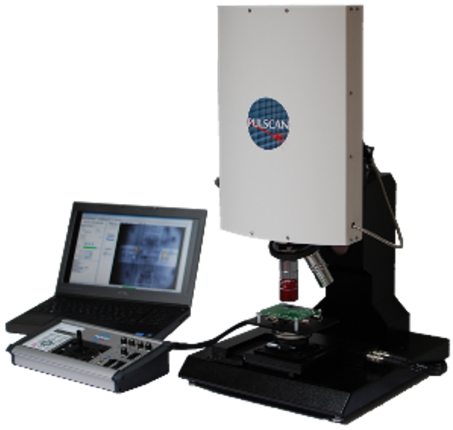


Figure A.32: Pulscan laser scanning system

Figure A.33 shows how the PULSCAN system scans a typical chip from the bottom side. A minimum of 10 mm height clearance is required for laser head movement. There is also a requirement of 45° clearance to avoid cutting the laser beam path.

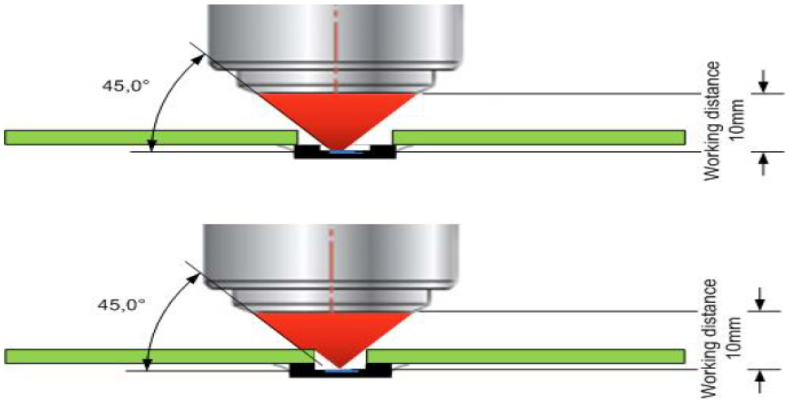
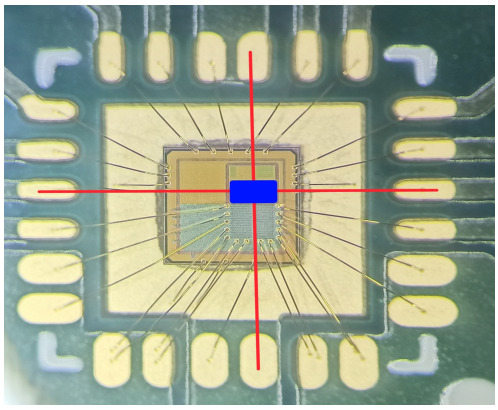
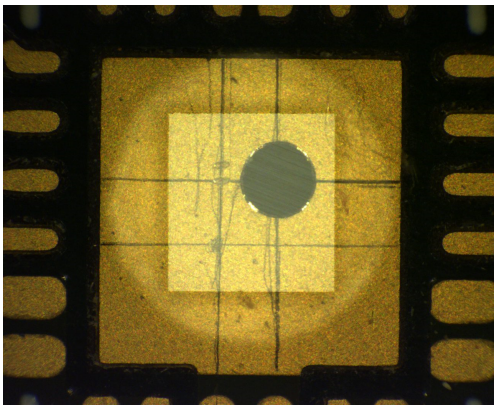


Figure A.33: PCB cut size requirements for proper Laser scan

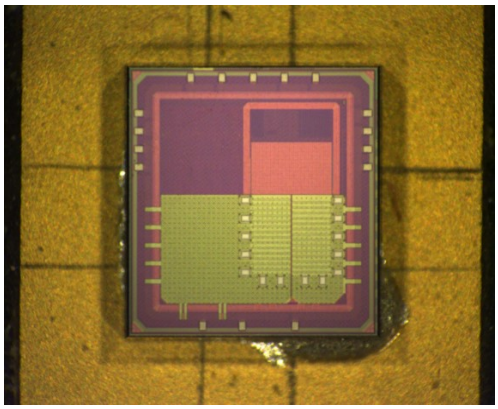
Due to the presence of bond wires and metal layers on the top side of the chip, laser scanning is only feasible from the bottom side of the chip. A small hole of 800 μm is drilled precisely by micro-drilling. The hole was made by taking two x and y-axis references on PCB landing pads to make the AOI of the die be placed on the center mark of chosen references. The chip is also placed by taking the same x and y-axis reference marks to ensure precise alignment. The hole is made of a beveled shape with an angle of 45° from the backside to allow the incidence of laser energy onto the AOI fully. Figure A.34 shows the intermediate steps for LDO alignment over the drilled hole on PCB. Figure A.34a shows marking of AOI of the chip and reference lines on an existing bonded LDO chip. These references were drawn on a new PCB for precise drilling of the hole underneath AOI, as shown in Figure A.34b. Then a new chip is placed in position over the drilled hole shown in Figure A.34c. Finally, the laser test will be done during the last week of November, 2021. The test results will be compared with simulation findings, and any additional revealed sensitive nodes will be modified before the mass production of the final version of the LDO chip.



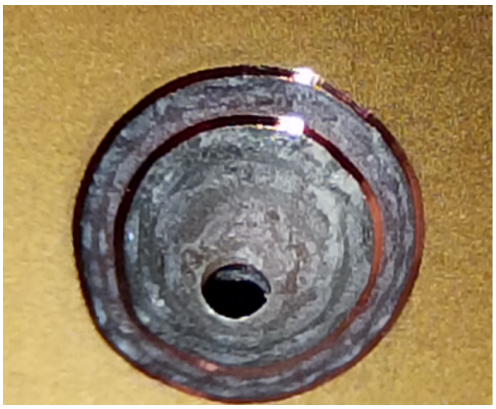
(a) step 1: A pre-aligned and bonded chip is taken as a baseline. Four landing pads on the PCB were used to reference the centre of the area of interest (AOI)



(b) step 2: A 800μm diameter hole is drilled at the centre of AOI location



(c) step 3: Aligning of the LDO over the hole with respect to the same reference pads on the PCB.



(d) Bottom view of the drilled hole to show back of AOI of the LDO. The hole is made 45° bevel to avoid laser beam obstruction, while entering the PCB.

Figure A.34: Preparation of LDO board for LASER beam irradiation. Pictures showing drilling of a hole and precise placement of the LDO over the hole to expose the area of interest (AOI) for the laser beam.

A.6.4 LDO design improvements

After LDO simulations, several design improvements were considered, and a few were implemented in the updated LDO version 3v0. Extra caution was done in design upgrades, considering that new upgrades should not compromise achieved device functionality and radiation robustness.

The first most straightforward modifications were the addition or increase of capacitance with critical nets. Secondly, the removal of regeneration inverters was done to reduce the number of sensitive nets. Finally, the power-down nets were made slower in order to make the system more robust to SEEs.

The simulations of upcoming LDO 3v0 showed that the problem of LDO output voltage drop, then enters again in startup mode, and prolonged recovery time has now been solved. The simulation applied five times more SE energy than the expected maximum (30mA peak current and 250ps of duration), and LDO worked without issues. Regarding the PG and OCZ LDO outputs, the small observed glitches on version 1v0 were also improved, but some glitches still can occur. These glitches were deemed as not critical.

A.7 LDO mass production planning

Mass production of packaged LDO (100k LDOs) is expected to begin at the beginning of 2022. Most of the commercial companies usually use IC testers to qualify the bulk production lots. The production test specifications are written to keep in mind commercial testers, overall test time, and low-cost testing strategies. A proposed list of LDO production tests is as follows:

- **IDDQ test**: Detects total chip current (I_{DD}) in quiescent state. This corresponds to no activity in the chip.
- **LDO Disable test**: Detects the Disable functionality of LDO and verifies if EN pin is correctly wire-bonded inside the package
- **Normal Start test**: Verifies the usual start of LDO at three different output currents of 1, 2, and 3A.
- **Soft Start test**: Verifies the soft start functionality of the chip.
- **Over Current test**: Verifies the overcurrent protection capability of the LDO.
- **M50, P50 test**: Verifies LDO output voltage adjustment functionality.

The applied inputs and expected outputs for each test are discussed in table A.7.

A.7.1 LDO binning

The LDO binning could result in the following two categories:

1. ***Green***: The performance of LDO is within the specified range and according to table A.7.
2. ***Red***: LDO does not conform to table A.7, leads to rejection of the LDO.

The result of each test vector will be appended in a ***.csv*** file, including associated bin color. The production data will be beneficial to visualize common modes of failure and voltage accuracy of LDO lots. Histograms of output data can distinguish different LDO bins, which could be used to set the initial LDO voltage settings.

		INPUTS						OUTPUTS				Comment
Vector	Duration	EN	SOFTST	M_{50}	P_{50}	V_i	I_{load}	PG	OC_z	V_o	$I_{V_{in}}$	
1	@ 1 ms	0	0	0	0	1.5 V	0 A	0	0	$< 50\ mV$	$< 5\ mA$	IDDQ test
2	@ 1 ms	0	0	0	0	2.2 V	0 A	0	0	$< 50\ mV$	$< 5\ mA$	
3	@ 1 ms	0	0	0	0	2 V	1 A	0	0	$< 5mV$	$\times$	LDO Disabled test
4	@ 100 μs	0	0	0	0	2 V	1 A	0	1	$< 5\ mV$	$\times$	Normal start test
5	@ 100 μs	1	0	0	0	2 V	1 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	
6	@ 100 μs	0	0	0	0	1.6 V	2 A	0	1	$< 5\ mV$	$\times$	
7	@ 100 μs	1	0	0	0	1.6 V	2 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	
8	@ 100 μs	0	0	0	0	1.4 V	3 A	0	1	$< 5\ mV$	$\times$	
9	@ 100 μs	1	0	0	0	1.4 V	3 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	
10	-	0	0	0	0	2 V	1 A	0	0	$< 50\ mV$	$\times$	Soft Start test
11	-	0	1	0	0	2 V	1 A	0	0	$< 50\ mV$	$\times$	
12	@ 5 ms	1	1	0	0	2 V	1 A	$\times$	$\times$	$< 0.6\ V$	$\times$	
13	@ 15 ms	1	1	0	0	2 V	1 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	
14	@ 100 μs	1	0	0	0	2 V	1 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	Over current test
15	@ 100 μs	1	0	0	0	1.5 V	5 A	0	0	$< 50\ mV$	$\times$	
16	@ 100 μs	1	0	0	0	2 V	1 A	0	0	$< 50\ mV$	$\times$	
17	@ 100 μs	0	0	0	0	2 V	1 A	0	0	$< 50\ mV$	$\times$	
18	@ 100 μs	1	0	0	0	2 V	1 A	1	1	$1.180V \leq Vo \leq 1.220V$	$\times$	
19	@ 100 μs	1	0	1	0	2 V	1 A	1	1	$1.130V \leq Vo \leq 1.170V$	$\times$	M_{50}, P_{50} test
20	@ 100 μs	1	0	0	1	2 V	1 A	1	1	$1.230V \leq Vo \leq 1.270V$	$\times$	
21	@ 100 μs	1	0	1	1	2 V	1 A	1	1	$1.280V \leq Vo \leq 1.320V$	$\times$	

Table A.7: LDO production test vectors and output table

A.8 Summary

A thorough radiation characterization campaign to qualify a high current low voltage LDO designed for CMS HGCAL upgrades was performed. Firstly, TID tests were performed up to 1-Grad, and all the internal functions of the LDO were monitored during the test. LDO performed extremely well even under full load conditions. However, a slight slow rise of 20 mV, after 1-Grad of dose, in the output voltage of the LDO was observed. This rise is well accountable for the output adjustment option available in the LDO. Secondly, Five LDOs were irradiated with neutrons at the IJS reactor. Three LDOs were irradiated at 1×10^{16} $n_{eq}cm^2$ and two were irradiated at 2×10^{16} $n_{eq}cm^2$. The LDOs showed an average increase of 30mV after checkpoint-1 and an increase of 40 mV after checkpoint-2.

The heavy-ion SEU testing was done to observe transient produced at the outputs of the LDO due to sensitive region upsets by energy transfer from single high energy heavy ions. A large transient pulse was observed during heavy ion irradiation. Both laboratory investigations and device simulations confirmed regeneration of transients by injection of short pulses in the enable path of the LDO. The sensitive nodes were identified with more

precision in the simulation, and a correlation with the actual SEU energy was established. Lastly, as a part of the SEU debugging campaign, a laser scanning of the LDO is also planned, and dedicated PCB modifications has been done. The laser test is important to verify precisely the sensitive nodes of the LDO which were identified with the device simulation. In addition, it will remove the chance of any hidden sensitive node which might could might not be identified during device simulations.

An improved version of the LDO has been submitted for fabrication and will be available for testing in December 2021. Finally, the specifications for the mass production of the LDO were prepared, keeping in mind the industrial testing constraints and procedures.

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